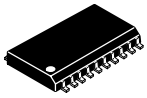
MC100LVEL37

3.3V ECL 1:4 ÷1/÷2 Clock Fanout Buffer

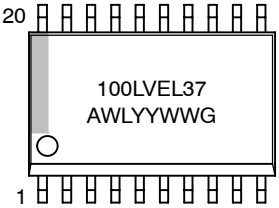
ON Semiconductor®

http://onsemi.com



SO−20 WB
DW SUFFIX
CASE 751D

MARKING DIAGRAM*



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Description

The MC100LVEL37 is a fully differential 1:4 fanout buffer. The device offers two outputs at ÷1 of the input frequency, and two outputs at ÷2 of the input frequency. The Low Output−Output Skew of the device makes it ideal for distributing 1x and 1/2x frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the CLKn input will pull down to V_{EE}, The $\overline{CLKn}$ input will bias around $V_{CC}/2$ and the Qn output will go LOW.

Features

- 700 ps Typical Propagation Delays
- 50 ps Maximum Output−Output Skews
- ESD Protection: >2 kV Human Body Model, >200 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −3.8 V
- Internal Input Pulldown Resistors
- Qn Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V−0 @ 0.125 in, Oxygen Index 28 to 34
- Transistor Count = 256 devices
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

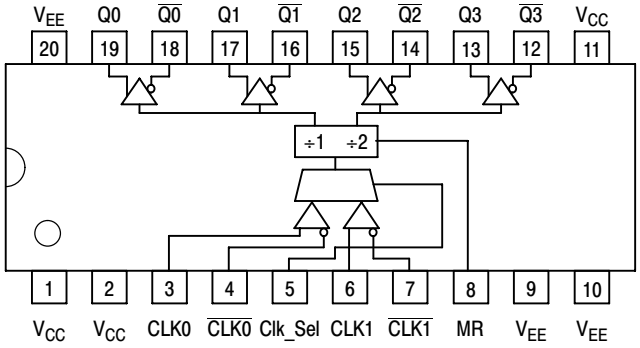


Figure 1. 20−Lead Pinout (Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Table 1. TRUTH TABLE

Clk_Sel	MR	Q0, 1	Q2, 3
L	L	CLK0/÷1	CLK0/÷2
H	L	CLK1/÷1	CLK1/÷2
X	H	L	L

X = Don't Care

Table 2. PIN DESCRIPTION

PIN	FUNCTION
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Differential Clock ÷1 Outputs
Q2, $\overline{Q2}$; Q3, $\overline{Q3}$	ECL Differential Clock ÷2 Outputs
CLKn, $\overline{CLKn}$	ECL Differential Clock Inputs
Clk_Sel	ECL Input Clock Selection
MR	ECL Asynchronous Master Reset
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 −6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 lfpm 500 lfpm	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	Standard Board	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder Pb Pb−Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0.0 V (Note 1)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		38	50		38	55		38	55	mA
V_{OH}	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)										
	V_{PP} < 500 mV	1.3		2.9	1.2		2.9	1.2		2.9	V
	V_{PP} ≧ 500 mV	1.5		2.9	1.4		2.9	1.4		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLKn	0.5			0.5			0.5			μA
	$\overline{CLKn}$	−300			−300			−300			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 5. LVNECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 4)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		38	50		38	55		38	55	mA
V_{OH}	Output HIGH Voltage (Note 5)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
V_{OL}	Output LOW Voltage (Note 5)	−1830	−1695	−1555	−1810	−1705	−1620	−1810	−1705	−1620	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)										
	V_{PP} < 500 mV	−2.0		−0.4	−2.1		−0.4	−2.1		−0.4	V
	V_{PP} ≧ 500 mV	−1.8		−0.4	−1.9		−0.4	−1.9		−0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLKn	0.5			0.5			0.5			μA
	$\overline{CLKn}$	−300			−300			−300			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
5. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
6. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 6. AC CHARACTERISTICS V_{CC} = 3.3 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = −3.3 V (Note 7)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
fmax	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay										ps
	CLK to Q/$\overline{Q}$ (Diff)	640		940	680	700	920	720		980	
	CLK to Q/$\overline{Q}$	620		920	680	700	940	720		970	
	MR to Q	640		920	680	700	920	720		980	
t_{SKEW}	Within-Device Skew (Note 8) Duty Cycle Skew (Differential Configuration) (Note 9)			50 50			50 50			50 50	ps
t_{JITTER}	Cycle−to−Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 10)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% − 80%)	280		550	280		550	280		550	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. V_{EE} can vary ±0.3 V.
8. Within-device skew defined as identical transitions on similar paths through a device.
9. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
10. V_{PP}(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

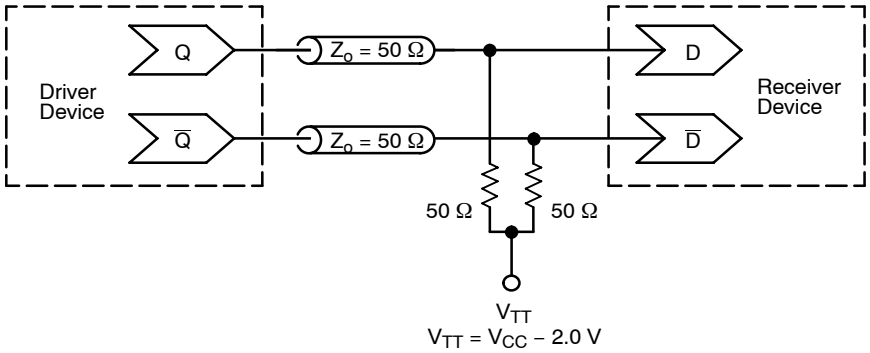


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVEL37DW	SO−20 WB	38 Units / Rail
MC100LVEL37DWG	SO−20 WB (Pb−Free)	38 Units / Rail
MC100LVEL37DWR2	SO−20 WB	1000 / Tape & Reel
MC100LVEL37DWR2G	SO−20 WB (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

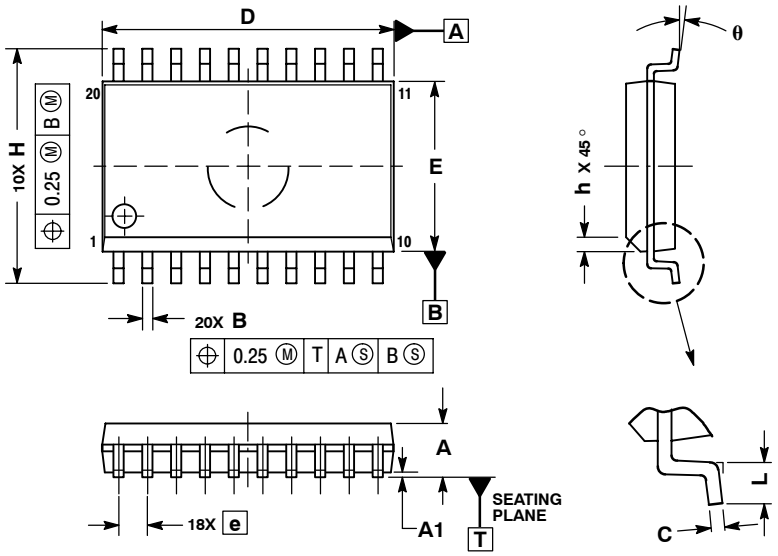
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

SO−20 WB
DW SUFFIX
CASE 751D−05
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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