

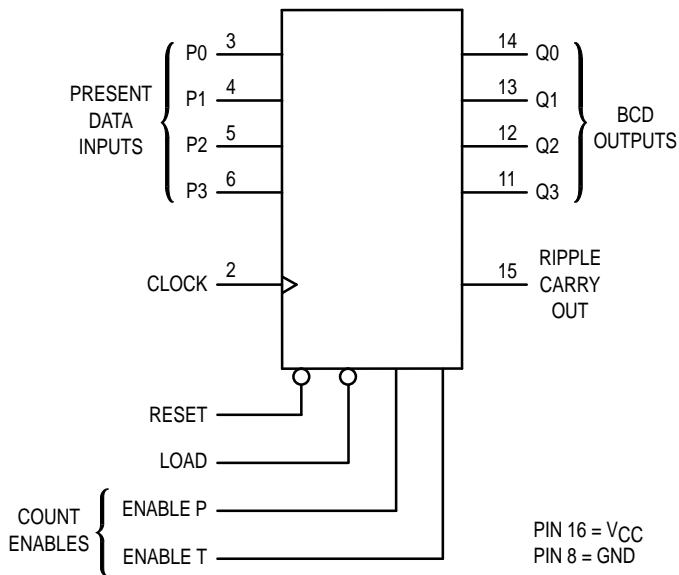
Product Preview
Pre-settable Counters
High-Performance Silicon-Gate CMOS

The MC54/74HC160A and HC162A are identical in pinout to the LS160 and LS162, respectively. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC160A and HC162A are programmable BCD counters with asynchronous and synchronous Reset inputs, respectively.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates

LOGIC DIAGRAM



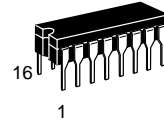
Device	Count Mode	Reset Mode
HC160	BCD	Asynchronous
HC162	BCD	Synchronous

FUNCTION TABLE

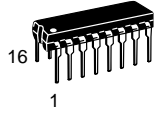
Inputs					Output
Clock	Reset*	Load	Enable P	Enable T	Q
	L	X	X	X	Reset
	H	L	X	X	Load Preset Data
	H	H	H	H	Count
	H	H	L	X	No Count
	H	H	X	L	No Count

* HC162A only. HC160A is an Asynchronous Reset Device
H = high level
L = low level
X = don't care

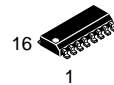
MC54/74HC160A
MC54/74HC162A



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08

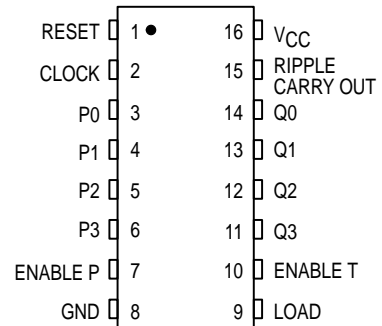


D SUFFIX
SOIC PACKAGE
CASE 751B-05

ORDERING INFORMATION

MC54HCXXXAJ Ceramic
MC74HCXXXAN Plastic
MC74HCXXXAD SOIC

PIN ASSIGNMENT



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MC54/74HC160A MC54/74HC162A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
Ceramic DIP: - 10 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	- 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)			ns
	$V_{CC} = 2.0 \text{ V}$	0	1000	
	$V_{CC} = 4.5 \text{ V}$	0	500	
	$V_{CC} = 6.0 \text{ V}$	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

MC54/74HC160A MC54/74HC162A

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle)* (Figures 1 and 7)	2.0	6.0	4.8	4.0	MHz
		3.0	TBD	TBD	TBD	
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 7)	2.0	170	215	255	ns
		3.0	TBD	TBD	TBD	
		4.5	34	43	51	
		6.0	29	37	43	
t _{PHL}		2.0	205	255	310	
		3.0	TBD	TBD	TBD	
		4.5	41	51	62	
		6.0	35	43	53	
t _{PHL}	Maximum Propagation Delay, Reset to Q (HC160A Only) (Figures 2 and 7)	2.0	210	265	315	ns
		3.0	TBD	TBD	TBD	
		4.5	42	53	63	
		6.0	36	45	54	
t _{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 3 and 7)	2.0	160	200	240	ns
		3.0	TBD	TBD	TBD	
		4.5	32	40	48	
		6.0	27	34	41	
t _{PHL}		2.0	195	245	295	
		3.0	TBD	TBD	TBD	
		4.5	39	49	59	
		6.0	33	42	50	
t _{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 1 and 7)	2.0	175	220	265	ns
		3.0	TBD	TBD	TBD	
		4.5	35	44	53	
		6.0	30	37	45	
t _{PHL}		2.0	215	270	325	
		3.0	TBD	TBD	TBD	
		4.5	43	54	65	
		6.0	37	46	55	
t _{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160A Only) (Figures 2 and 7)	2.0	220	275	330	ns
		3.0	TBD	TBD	TBD	
		4.5	44	55	66	
		6.0	37	47	56	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 7)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

* Applies to noncascaded/nonsynchronously clocked configurations only. With synchronously cascaded counters, (1) Clock to Ripple Carry Out propagation delays, (2) Enable T or Enable P to Clock setup times, and (3) Clock to Enable T or Enable P hold times determine f_{max}. However, if Ripple Carry Out of each stage is tied to the Clock of the next stage (nonsynchronously clocked), the f_{max} in the table above is applicable. See Applications Information in this data sheet.

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	
		60	
			pF

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock (Figure 5)	2.0	150	190	225	ns
		3.0	TBD	TBD	TBD	
		4.5	30	38	45	
		6.0	26	33	38	
t_{su}	Minimum Setup Time, Load to Clock (Figure 5)	2.0	135	170	205	ns
		3.0	TBD	TBD	TBD	
		4.5	27	34	41	
		6.0	23	29	35	
t_{su}	Minimum Setup Time, Reset to Clock (HC162A only) (Figure 4)	2.0	160	200	240	ns
		3.0	TBD	TBD	TBD	
		4.5	32	40	48	
		6.0	27	34	41	
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock (Figure 6)	2.0	200	250	300	ns
		3.0	TBD	TBD	TBD	
		4.5	40	50	60	
		6.0	34	43	51	
t_h	Minimum Hold Time, Clock to Preset Data Inputs (Figure 5)	2.0	50	65	75	ns
		3.0	TBD	TBD	TBD	
		4.5	10	13	15	
		6.0	9	11	13	
t_h	Minimum Hold Time, Clock to Load (Figure 5)	2.0	3	3	3	ns
		3.0	TBD	TBD	TBD	
		4.5	3	3	3	
		6.0	3	3	3	
t_h	Minimum Hold Time, Clock to Reset (HC162A only) (Figure 4)	2.0	3	3	3	ns
		3.0	TBD	TBD	TBD	
		4.5	3	3	3	
		6.0	3	3	3	
t_h	Minimum Hold Time, Clock to Enable T or Enable P (Figure 6)	2.0	3	3	3	ns
		3.0	TBD	TBD	TBD	
		4.5	3	3	3	
		6.0	3	3	3	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (HC160A only) (Figure 2)	2.0	125	155	190	ns
		3.0	TBD	TBD	TBD	
		4.5	25	31	38	
		6.0	21	26	32	
t_{rec}	Minimum Recovery Time, Load Inactive to Clock (Figure 5)	2.0	125	155	190	ns
		3.0	TBD	TBD	TBD	
		4.5	25	31	38	
		6.0	21	26	32	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		3.0	TBD	TBD	TBD	
		4.5	16	20	24	
		6.0	14	17	20	
t_w	Minimum Pulse Width, Reset (HC160A only) (Figure 2)	2.0	80	100	120	ns
		3.0	TBD	TBD	TBD	
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

FUNCTION DESCRIPTION

The HC160A/162A are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls.

The HC160A and HC162A are BCD counters with asynchronous Reset, and synchronous Reset, respectively.

INPUTS

Clock (Pin 2)

The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting (HC162A) and loading occur with the rising edge of the Clock input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (pin 3) is the least-significant bit and P3 (pin 6) is the most-significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs (BCD or binary). Q0 (pin 14) is the least-significant bit and Q3 (pin 11) is the most-significant bit.

Ripple Carry Out (Pin 15)

When the counter is in its maximum state (1001 for the BCD counters or 1111 for the binary counters), this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

$$\text{Ripple Carry Out} = \text{Enable T} \cdot \text{Q0} \cdot \overline{\text{Q1}} \cdot \overline{\text{Q2}} \cdot \text{Q3}$$

for BCD counters HC160A and HC162A

CONTROL FUNCTIONS

Resetting

A low level on the Reset pin (pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HC160A resets asynchronously and the HC162A resets with the rising edge of the Clock input (synchronous reset).

Loading

With the rising edge of the Clock, a low level on Load (pin 9) loads the data from the Preset Data Input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Although the HC160A and HC162A are BCD counters, they may be programmed to any state. If they are loaded with a state disallowed in BCD code, they will return to their normal count sequence within two clock pulses (see the Output State Diagram).

Count Enable/Disable

These devices have two count-enable control pins: Enable P (pin 7) and Enable T (pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \cdot \text{Enable T} \cdot \text{Load}$$

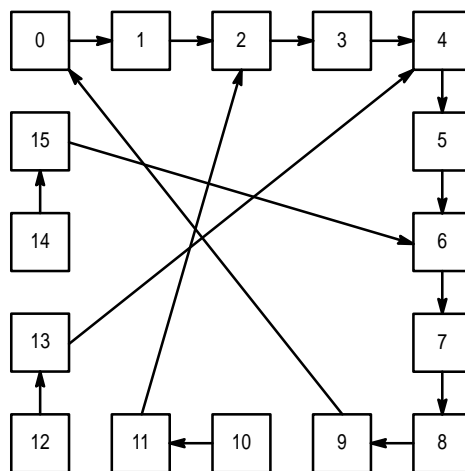
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control; Enable T is both a count-enable and a Ripple-Carry Output control.

Table 1. Count Enable/Disable

Control Inputs		Result at Outputs		
Load	Enable P	Enable T	Q0 – Q3	Ripple Carry Out
H	H	H	Count	High when Q0–Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0–Q3 are maximum*
X	X	L	No Count	L

* Q0 through Q3 are maximum for the HC160A and HC162A when Q3 Q2 Q1 Q0 = 1001.

**OUTPUT STATE DIAGRAMS
HC160A and HC162A BCD Counters**



SWITCHING WAVEFORMS

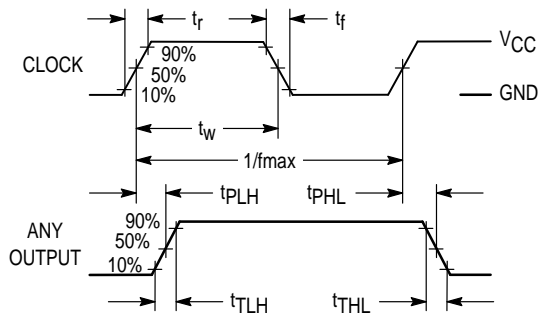


Figure 1.

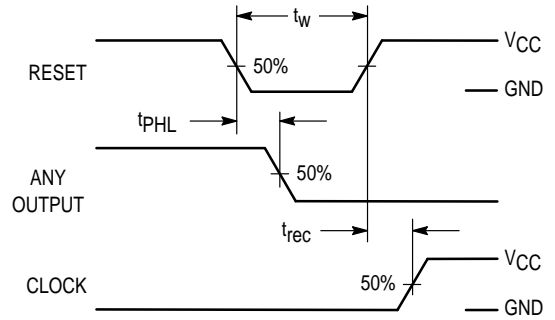


Figure 2.

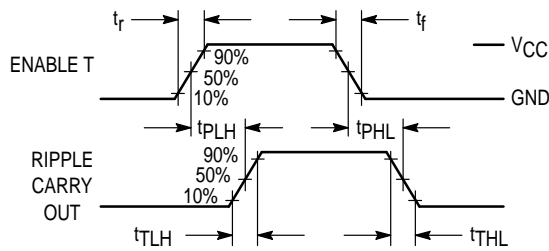


Figure 3.

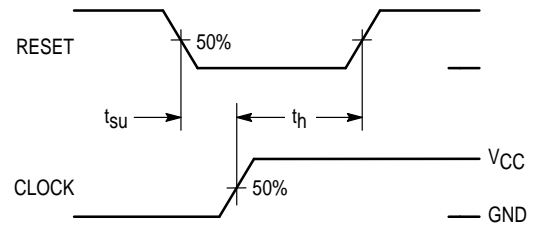


Figure 4. HC162A Only

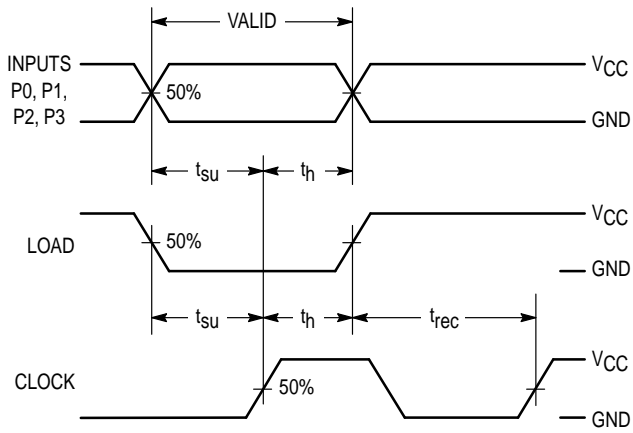


Figure 5.

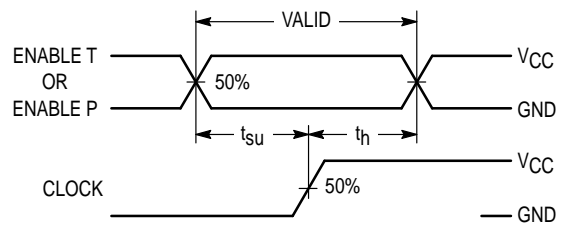
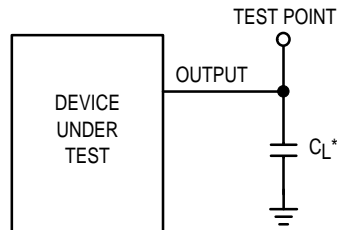


Figure 6.

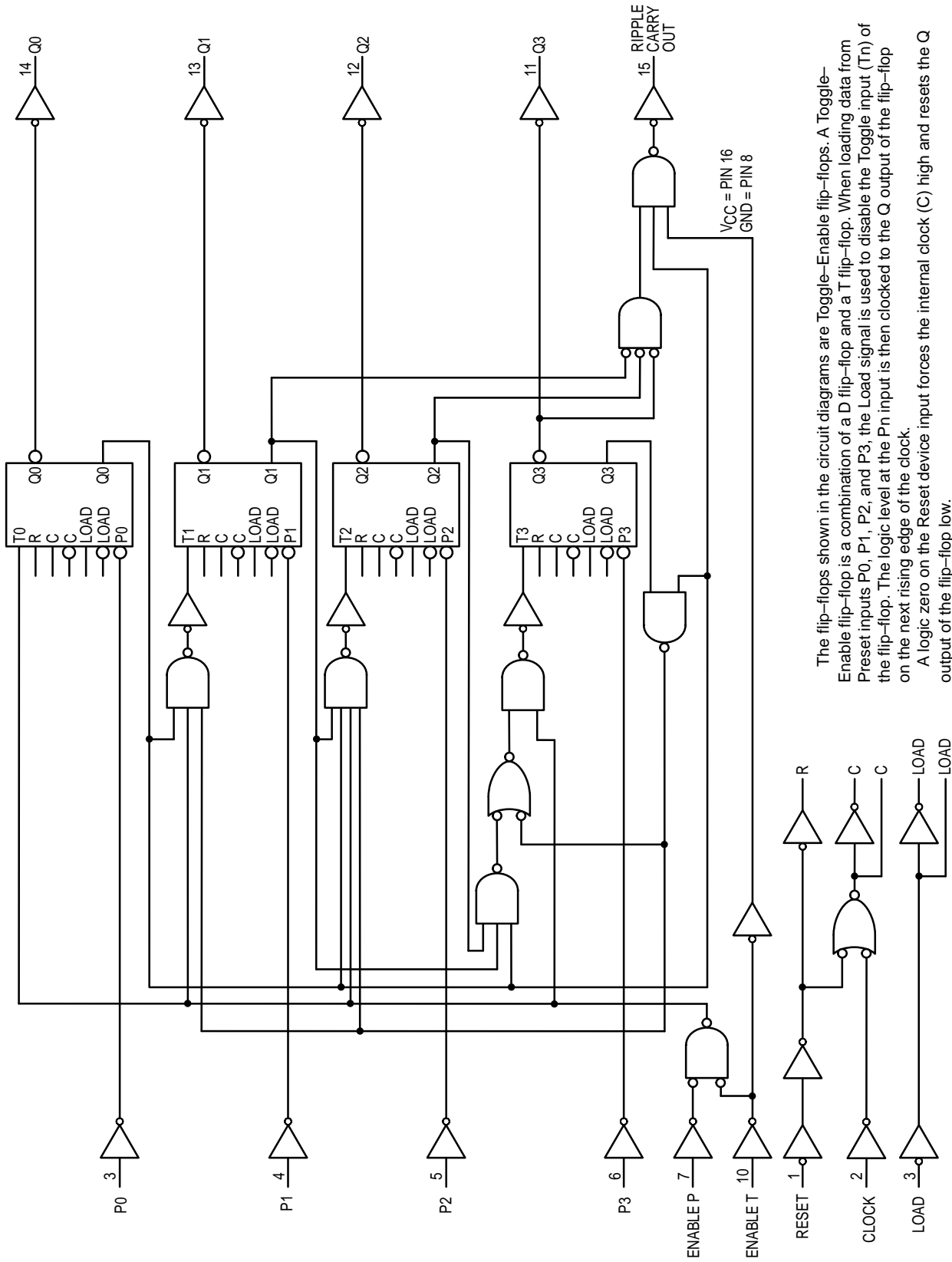
TEST CIRCUIT



* Includes all probe and jig capacitance

Figure 7.

MC54HC160A • MC74HC160A
BCD Counter with Asynchronous Reset

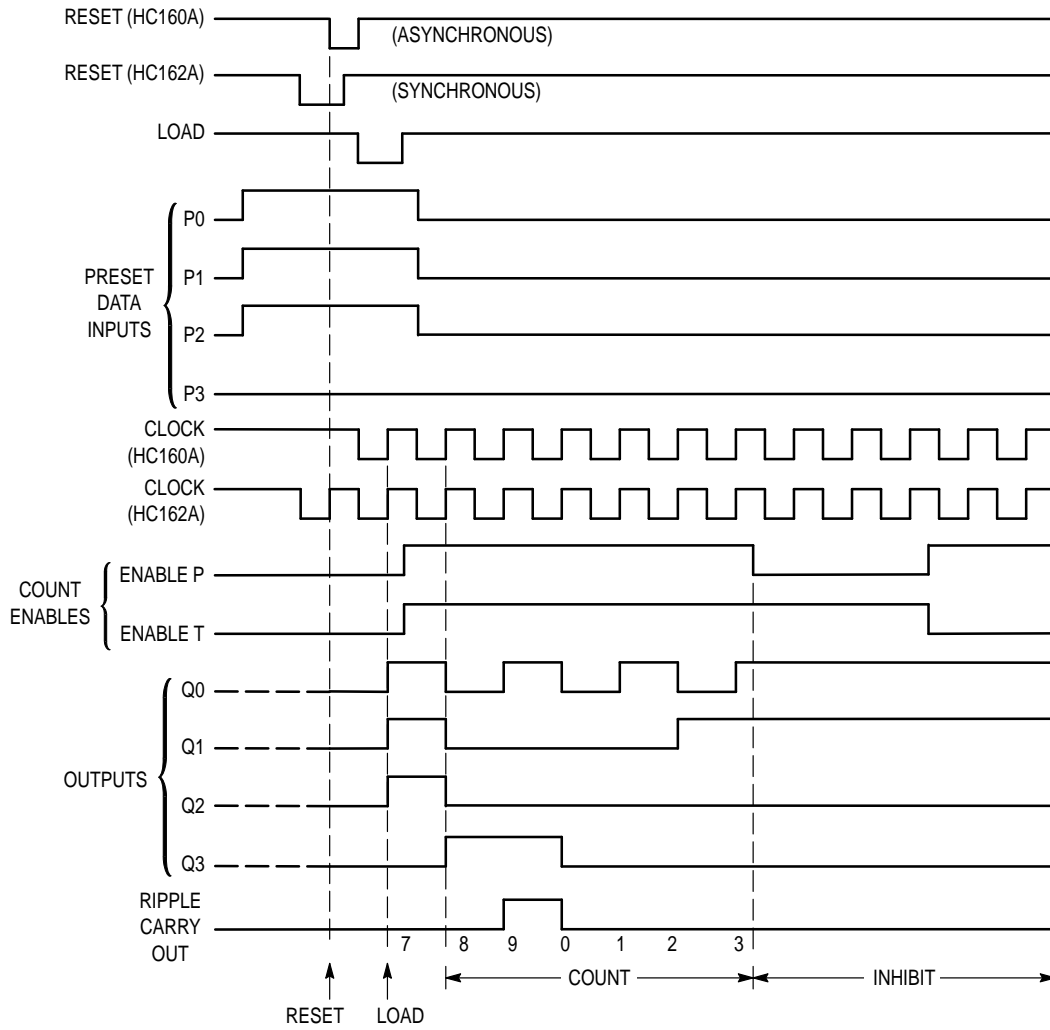


The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.
 A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

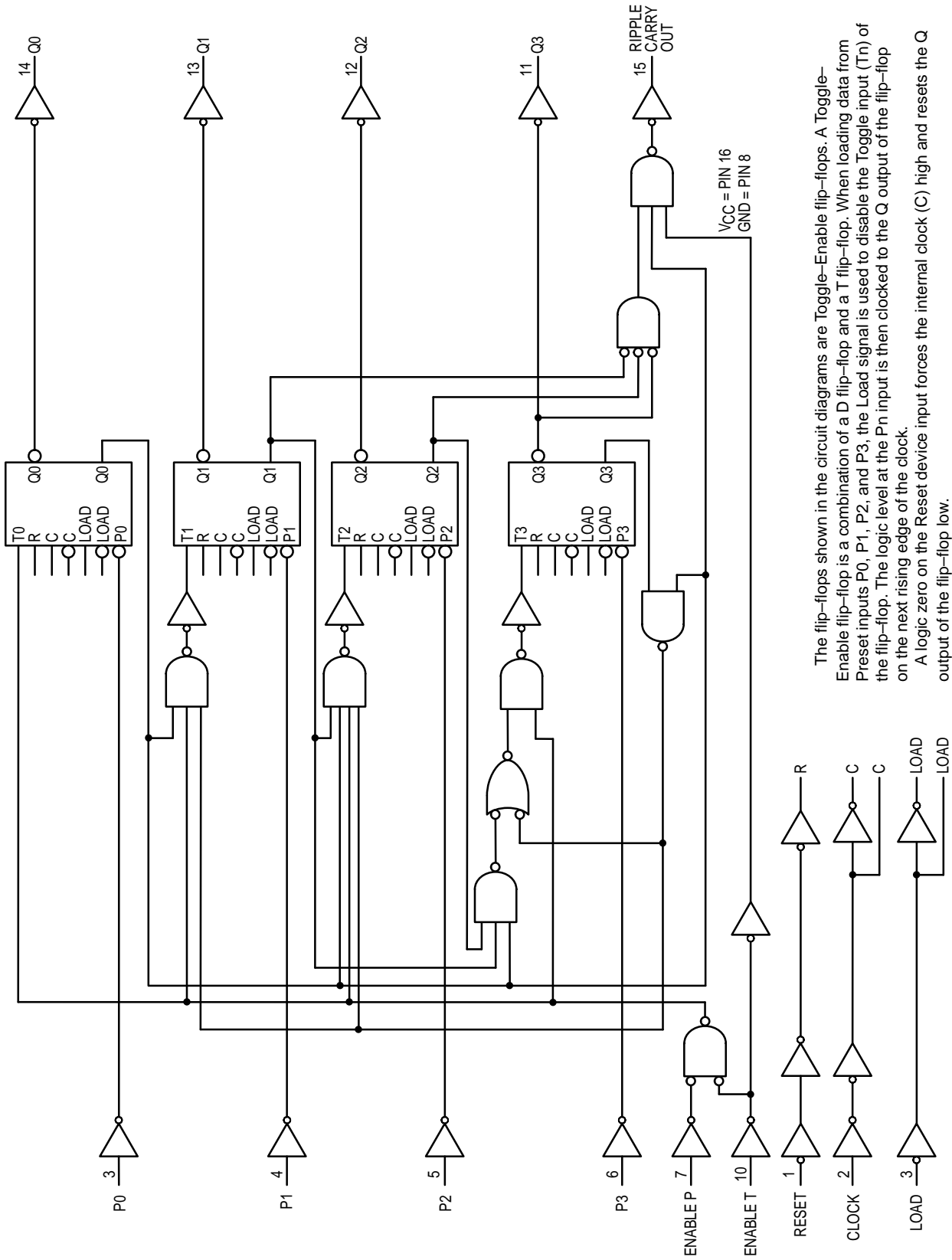
HC160A, HC162A TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



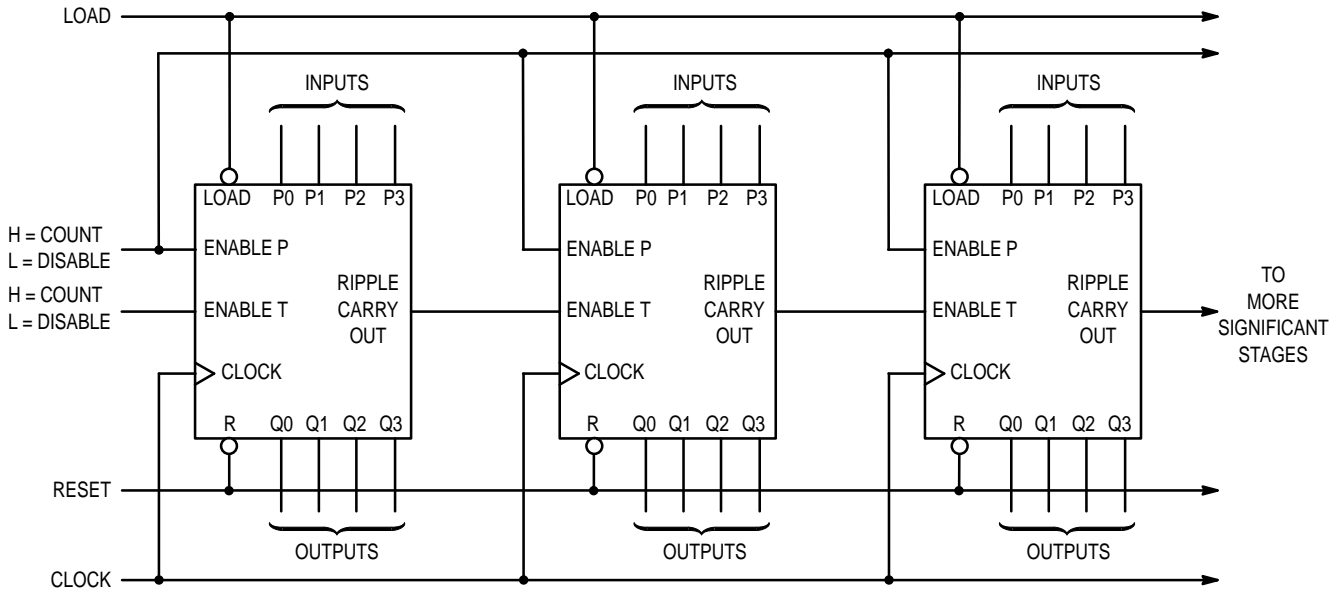
MC54HC160A • MC74HC160A
BCD Counter with Synchronous Reset



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.
A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

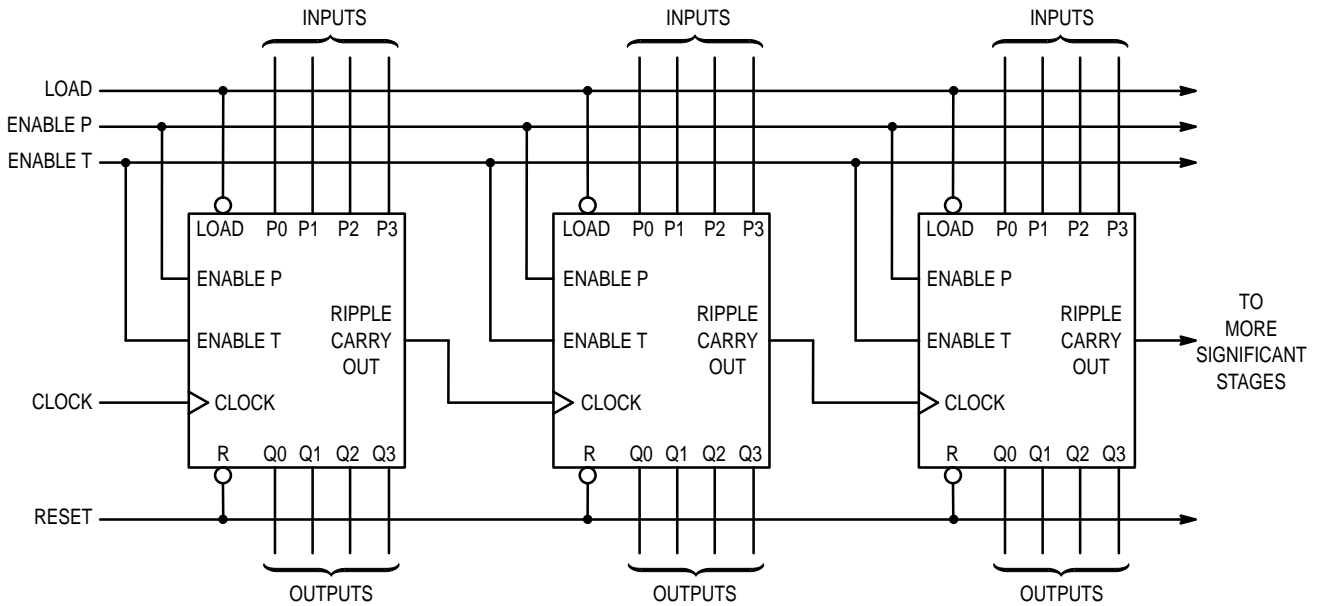
TYPICAL APPLICATIONS
CASCADING

N-Bit Synchronous Counters

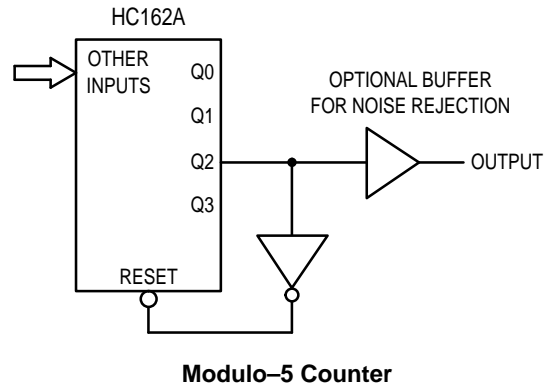


NOTE: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.


Nibble Ripple Counter



TYPICAL APPLICATION



The HC162A facilitates designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous Reset.

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