Micro Linear

PRELIMINARY

ML2712 2.4GHz RF Transceiver

GENERAL DESCRIPTION

The ML2712 combined with the ML2713 form a FSK (Frequency Shift Keying) 2.4 GHz radio chipset. The ML2712 contains the RF and PLL circuits for a half duplex radio transceiver solution for IEEE802.11 and other wireless communication protocols using the 2.4 GHz ISM band.

The ML2712 is controlled using a three-wire programming interface and three control lines. The transmit circuits feature an RF down converter for a transmit frequency translation loop and a Wideband Phase Detector for a directly modulated VCO transmitter. An RF down converter mixer is provided for receive. All frequency generation circuits are integrated for the RF conversion, the 1LO VCO and PLL plus a 2LO VCO and PLL for use in dual conversion radios. In addition the ML2712 contains an 8 bit D/A & Comparator that may be used together as a tracking A/D for Received Signal Strength Indication measurement (RSSI).

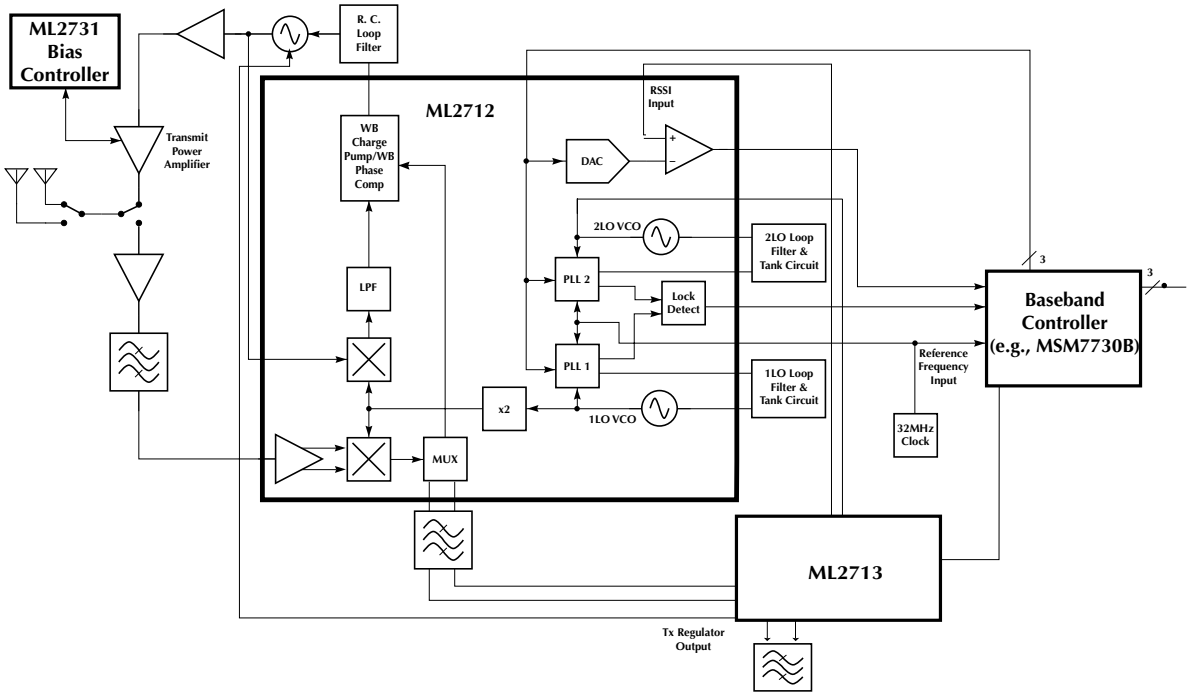
FEATURES

- 2.4GHz RF Down Converter
- Programmable 2.2GHz and 236MHz Frequency Synthesizers
- External VCO tank circuits for flexibility
- Compatibility with the OKI MSM7730 and similar baseband controllers
- Transmit Wideband Phase Comparator for closed loop transmitter with >5MHz loop bandwidth
- PLLs Programmable via 3 wire interface
- 48 pin TQFP 7mm body
- 3.0V to 5.5V operation

APPLICATIONS

- 2.4GHz Frequency Shift Key modulated radios
- PC Card & Flashcard Wireless Transceivers
- IEEE802.11FHSS Compatible 1 and 2Mbps Standard

SIMPLIFIED BLOCK DIAGRAM



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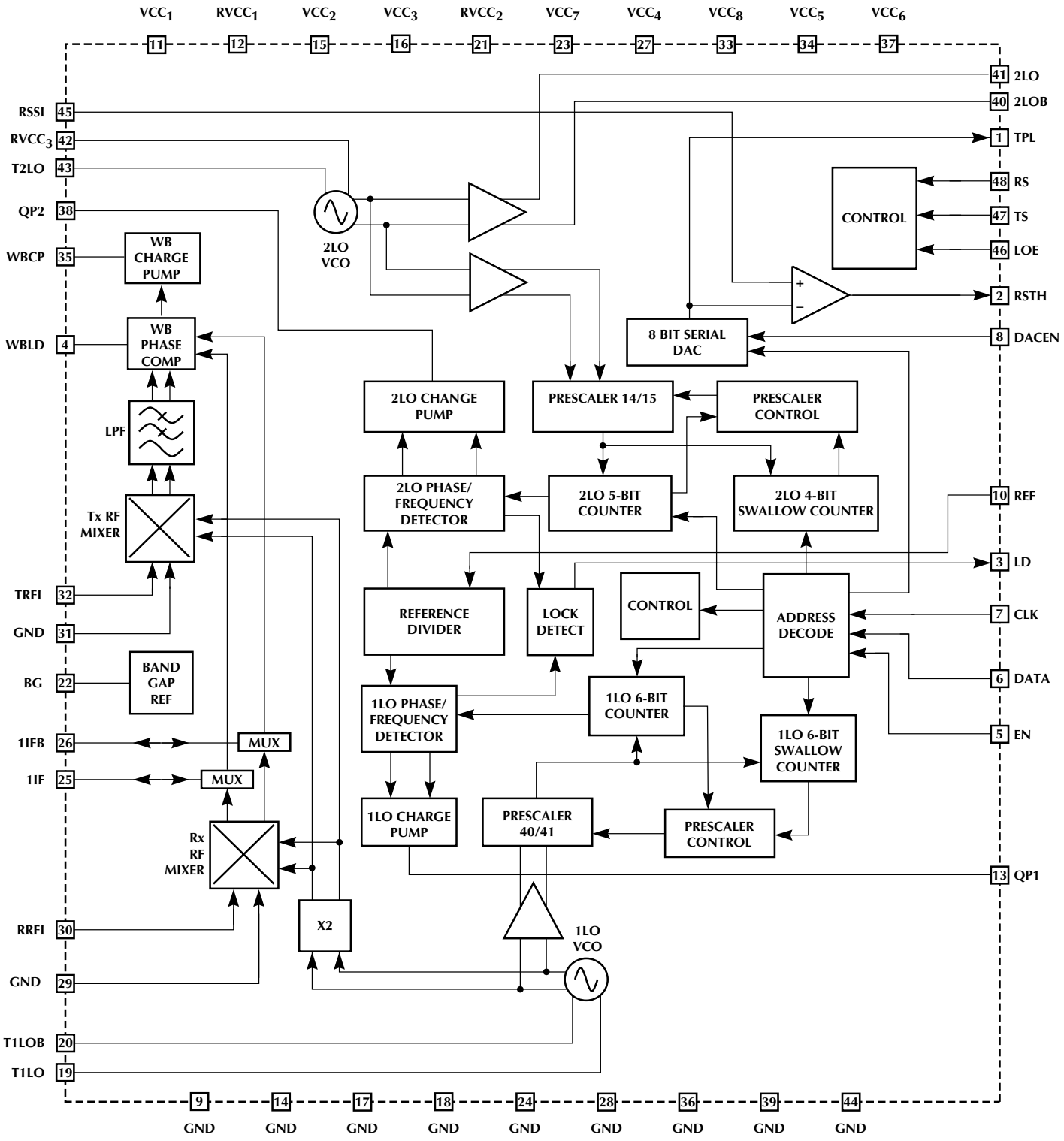
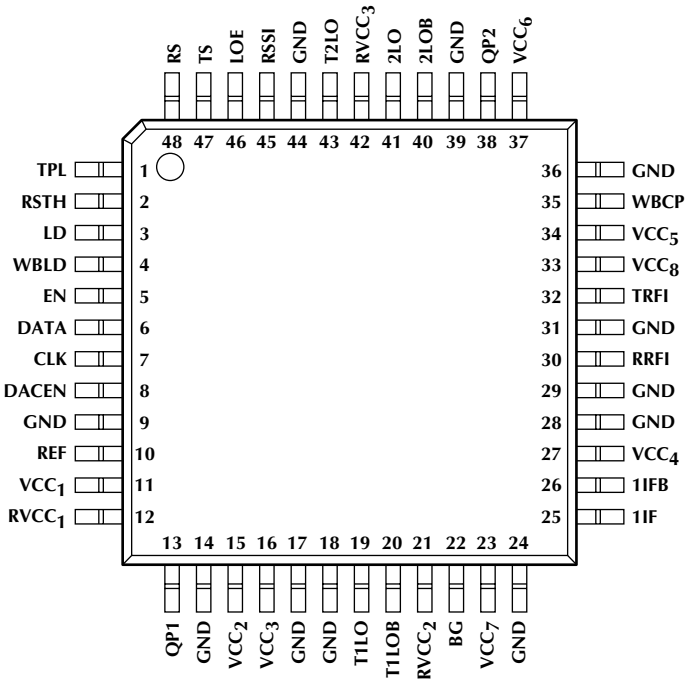
Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

BLOCK DIAGRAM



PIN CONFIGURATION

ML2712
48-Pin TQFP (H48-7)



TOP VIEW

PIN DESCRIPTIONS

Pin #	Signal Name	I/O Type	Description
Power and Ground			
11	VCC_1		Supply Voltage for CMOS Logic. A bypass capacitor connected with minimum trace lengths from VCC_1 to PCB ground is recommended
9	GND		Ground for CMOS Logic
15	VCC_2		Supply voltage for Digital/Analog Converter and Comparator. A bypass capacitor connected with minimum trace lengths from VCC_2 to PCB ground is recommended
16	VCC_3		Supply Voltage for 1LO Prescaler and Phase Detector. A bypass capacitor connected with minimum trace lengths from VCC_3 to PCB ground is recommended
17	GND		Ground for 1LO Prescaler and Phase Detector
27	VCC_4		Supply Voltage for RF Amplifier. A bypass capacitor connected with minimum trace lengths from VCC_4 to PCB ground is recommended
28	GND		Ground for RF Low Noise Amplifier
34	VCC_5		Supply Voltage for Wideband Transmit PLL Charge Pump. A bypass capacitor connected with minimum trace lengths from VCC_5 to PCB ground is recommended
36	GND		Ground for Wideband Transmit PLL Charge Pump. Minimizing the lead trace length from this GND to PCB ground to reduce inductance and resistance is recommended
37	VCC_6		Supply Voltage for 2LO Charge Pump. A bypass capacitor connected with minimum trace lengths from VCC_6 to PCB ground is recommended
39	GND		Ground for 2LO Charge Pump
23	VCC_7		Power Supply for 2LO Prescaler and Phase Detector. A bypass capacitor connected with minimum trace lengths from VCC_7 to PCB ground is recommended

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	I/O Type	Description
24	GND		Ground for 2LO Prescaler and Phase Detector
33	VCC_8		Supply Voltage for Mixers, 1LO Frequency Doubler, and Transmit PLL. A bypass capacitor connected with minimum trace lengths from VCC_8 to PCB ground is recommended
29	GND		Ground for Mixers, 1LO Frequency Doubler, and Transmit PLL
Regulated Power and Ground			
12	$RVCC_1$		Regulated Bypass Output Supply Voltage for 1LO PLL Charge Pump. A bypass capacitor connected with minimum trace lengths from $RVCC_1$ to PCB ground is recommended
14	GND		Ground for 1LO PLL Charge Pump
21	$RVCC_2$		Regulated Bypass Output Supply for 1LO Voltage Controlled Oscillator. A bypass capacitor connected with minimum trace lengths from $RVCC_2$ to PCB ground is recommended
18	GND		Ground for 1LO Voltage Controlled Oscillator
42	$RVCC_3$		Regulated Bypass Output Supply for 2LO Voltage Controlled Oscillator. A bypass capacitor connected with minimum trace lengths from $RVCC_3$ to PCB ground is recommended
44	GND		Ground for 2LO Voltage Controlled Oscillator
Transmitter Section			
32	TRFI	I	Transmit RF Input signal. This signal, input to the Transmit Down Converter Mixer should be AC coupled and matched to the nominal 50Ωinput impedance
31	GND		Transmit Signal Ground. Minimizing the lead trace length from this GND to PCB ground to reduce inductance and resistance is recommended
35	WBCP	O (Analog)	Wideband PLL Charge Pump output
10	REF	I	Reference frequency input to Phase Locked Loops. Requires square wave input
3	LD	O (CMOS)	Lock Detect output. Low output indicates this pin is in open drain. Two Phase Locked Loops are frequency locked and requires 10kΩ pull-up
4	WBLD	O (CMOS)	Wideband PLL Lock Detect open drain output and requires 10kΩ pull-up
41	2LO	O	2LO output. Together with 2LOB provides a balanced 2LO output port for input to Down Converter Mixer on ML2713. Requires 5KΩ external pull-up resistor to VCC3 if not connected to ML2713 In Standby Mode, 2LOB and 2LO provide a calibration tone used to calibrate the ML2713 IF Transceiver
40	2LOB	O	2LOI output. Together with 2LO provide a balanced 2LO output port for input to Down Converter Mixer on ML2713 Requires 5KΩ external pull-up resistor to VCC1 if not connected to ML2713 In Standby Mode, 2LO and 2LOB provide a calibration tone used to calibrate the ML2713 IF Transceiver
25	1IF	I/O	IF Input/Output. In RECEIVE Mode, functions with 1IFB to present a balanced first IF output port with 340Ω output impedance. Connection must be AC coupled. It is recommended that the signal trace connected to this pin be isolated from other signal or digital control lines to maintain receiver sensitivity In TRANSMIT Mode, functions with 1IFB to present a balanced first IF input port with 340Ω input impedance. Connection must be AC coupled. It is recommended that the signal trace connected to this pin be isolated from other signal or digital control lines to maintain receiver sensitivity

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	I/O Type	Description
26	1IFB	I/O	IF Input/Output Inverted. In RECEIVE Mode, functions with 1IF to present a balanced first IF output port with 340Ω output impedance. Connection must be AC coupled. It is recommended that the signal trace connected to this pin be isolated from other signal or digital control lines to maintain receiver sensitivity In TRANSMIT Mode, functions with 1IF to present a balanced first IF input port with 340Ω input impedance. Connection must be AC coupled. It is recommended that the signal trace connected to this pin be isolated from other signal or digital control lines to maintain receiver sensitivity
Receiver Section			
30	RRFI	I	Receive RF Input signal. It is recommended that the nominal input impedance of 20Ω on this pin be matched and be AC coupled
45	RSSI	I (Analog)	Received Signal Strength Indicator input
1	TPL	O	Digital to Analog Converter high output voltage defined by contents of Control Register E
2	RSTH	O (CMOS)	RSSI Threshold output. High output indicates RSSI input is greater than TPL. Digital to Analog Converter output voltage
19	T1LO	(Tank Port)	First Local Oscillator Tank circuit. T1LO and T1LOB provide a balanced pair for connection to an external parallel inductor/capacitor tank circuit that determines the frequency of oscillation
20	T1LOB	(Tank Port)	Inverted First Local Oscillator Tank circuit. T1LOTB and T1LO provide a balanced pair for connection to an external parallel inductor/capacitor tank circuit that determines the frequency of oscillation
13	QP1	O	Charge Pump output of 1LO Phase Locked Loop. Analog output switches between VCC_2 and ground
38	QP2	O (Analog)	Charge Pump output of 2LO Phase Locked Loop charge pump output. Analog output switches between VCC_6 and ground as controlled by the phase detector in the 2LO PLL
43	T2LO	O (Analog)	Second Local Oscillator Tank circuit. T2LO and GND (pin 44) provide an unbalanced pair for a connection to an external parallel inductor/capacitor tank circuit that determines the frequency of oscillation
22	BG	I/O (Analog)	Bandgap voltage output. Connection available for bypass capacitor recommended for noise decoupling from Bandgap voltage reference. Recommended capacitance value is 10nF connected to ground
Mode Control			
46	LOE	I (CMOS)	Local Oscillator Enable
47	TS	I (CMOS)	Transmit Switch
48	RS	I (CMOS)	Receive Switch
Serial Interface			
5	EN	I (CMOS)	Enable serial data
8	DACEN	I (CMOS)	D/A Converter Enable
6	DATA	I (CMOS)	Serial Data
7	CLK	I (CMOS)	Clock input for serial data

FUNCTIONAL DESCRIPTION

INTRODUCTION

The ML2712 2.4GHZ RF Transceiver contains all the RF circuitry, including the phase lock loop (PLL), and the active VCO circuits, for a half duplex transceiver. When combined with the ML2713 it enables the design of a high performance 2.4GHz half duplex radio with a fast switching time between transmit and receive modes. This is ideal for applications such as frequency hopping radio for the IEEE 802.11 FH standard.

The ML2712 Transceiver has four modes of operation; 1) Standby 2) Transmit 3) Receive and 4) Sleep. The operating modes of the ML2712 can be programmed through a parallel control interface or through a serial interface. Two serial control interfaces are utilized for programming the PLLs and on chip A/D.

In STANDBY mode all the PLL and VCO circuits are enabled while all the transmitter and receiver circuits are disabled. The use of STANDBY mode is recommended when the PLLs are locking, after the PLL frequencies have been reprogrammed, or after the IC has been transferred out of SLEEP mode.

The transmit circuits include a 2.4GHz RF down converter for transmit frequency translation and a Wideband Phase Detector that implements a directly modulated VCO transmitter radio architecture. The receive section of the ML2712 inlcudes a 2.4GHz RF mixer that down converts the received RF frequency to the first IF frequency; nominally 260MHz. All required frequency generation circuits are integrated on-chip for the RF conversion including the 1LO VCO and the PLL and 1LO frequency doubler. Additionally, a second VCO and PLL provide a 2LO output useable in IF circuits in a dual conversion radio. An 8 bit D/A & Comparator for an RSSI tracking A/D are also integrated on-chip.

The two local oscillator signals generated in the ML2712 are the 1LO with at a typical frequency in the region of 2.2GHz and the 2LO, with a typical frequency of 236MHz. Both signals are phase locked by the independently programmable PLLs to a common external reference frequency. External tank circuits are required for the 1LO and 2LO VCOs to determine the operating frequency ranges. The 1LO signal, generated by doubling the frequency of the 1LO VCO, is used by both the transmit and receive mixer circuits to down convert the 2.4GHz RF signals. The half-frequency 1LO VCO eases tank circuit design and minimizes the VCO pulling when the the radio switches between transmit and receive modes. The differential output from the 2LO VCO is provided for use in radio IF circuits such as the ML2713. A lock detect output indicates when the PLLs are frequency locked. Programming of the PLL frequency is performed via a three wire serial interface.

The ML2712 implements a directly modulated VCO transmitter architecture. The elements of this architecture include a Power Amplifier, a transmitter VCO, a transmitter reference generation circuit and a 1IF Wideband PLL which locks the Transmitter VCO to this transmit reference signal. The ML2712 does not integrate the PA but does provide the Wideband PLL and an RF down-convert mixer, enabling the transmit reference signal to be generated at a lower frequency. In TRANSMIT mode the 2.2GHz (nominal) 1LO signal is used to down-convert the 2.4GHz external transmit VCO RF signal. The down converted signal is then phase locked by the on chip wideband phase detector to an externally modulated signal (Transmit reference IF) and output to pins 1IFB and 1IF. The output of the Wideband phase detector controls the transmit VCO frequency (Tx VCO external to IC) via an external loop filter. For a typical application, e.g., IEEE802.11 the symbol rate is 1Msymbol/sec. The lock up time is less than 2µsec. enabling a radio designed with the ML2712 to switch between transmit and receive modes in less than 2µsec.

The ML2712 receiver circuits perform the RF down conversion. A typical receiver design would include the ML2712, an external LNA and RF filter, an IF filter and the ML2713 IF Transceiver. In RECEIVE mode, the ML2712 uses the 1LO signal to down convert the received 2.4 GHz band signal to a nominal 260 MHz IF. The received IF signal is output on 1IF and 1IFO pins. By multiplexing both the transmit and receive signals on one set of pins, only a single Surface Acoustic Wave (SAW) IF channel filter is required in the radio design. A SAW filter with a nominal Gaussian impulse response can be used to provide modulation filtering of the transmit reference IF signal. When in receive mode the A/D and Comparator provide the analog circuits for a tracking A/D converter, intended for RSSI digitization or clear channel assessment for "listen before talk" radios.

In SLEEP mode all circuits, except for the central interface and programming registers, are powered down to minimize power consumption.

MODES OF OPERATION

STANDBY MODE

In STANDBY mode all the PLL and VCO circuits are enabled while all the transmitter and receiver circuits are disabled. (see Figigure 1) The use of STANDBY mode is recommended when the PLLs are locking, after the PLL frequencies have been reprogrammed, or after the IC has been transferred out of SLEEP mode. The VCO and PLL circuits are enabled and reach a locked state in 150 usec indicated by an active Lock Detect (LD) signal.The frequency divide ratio settings defined by Control Word C and D (see Table 4) define the frequencies of the 1LO PLL and 2LO PLL.

TRANSMIT MODE

The ML2712 uses a directly modulated VCO running at the transmitter frequency to generate the transmited signal. The VCO is then free of unwanted spurious signals and has the advantage of requiring no bandpass filtering for the transmitter signal prior to or after the Power Amplifier. The transmitter VCO is phase locked to the center frequency with the transmitter modulation applied. The modulated signal is applied directly to the VCO inside the loop bandwidth of a phase locked loop. To allow modulation rates in excess of 1Mbps requires a very wideband phase detector, capable of operating with loop bandwidths in excess of 5MHz. In this circuit the noise floor is set by the transmit VCO rather than by upconvert mixers. The circuits active in TRANSMIT Mode are shown in Figure 2.

DIRECTLY MODULATED TRANSMIT VCO

The transmitter is designed to enable a significant amount of power to be generated at the required frequency using a VCO, and is a technique for generating low noise, phase/frequency modulated transmitters without the need for bandpass filtering.

The ML2712 transmitter architecture is shown Figure 3. A tuning voltage applied to the transmit VCO, operating at the final transmission frequency, ensures the correct center frequency before modulation is applied. This closed loop system, uses a PLL with the Transmit VCO phase locked to a modulated reference signal (S_{MOD}). The modulated reference signal is generated at 260MHz. The signal from the Transmit VCO is down converted with the 1LO signal, then filtered through a bandpass filter. The output of the filter is fed to the very high-speed phase/ frequency detector Wideband PLL. This compares the down-converted transmit signal with the modulated reference signal S_{MOD}.

Any frequency or phase error between S_{MOD} and the down-converted signal is corrected by changing the tuning voltage of the transmit VCO. The down-conversion with the F1LO translates the reference signal S_{MOD} to the final transmitter frequency.

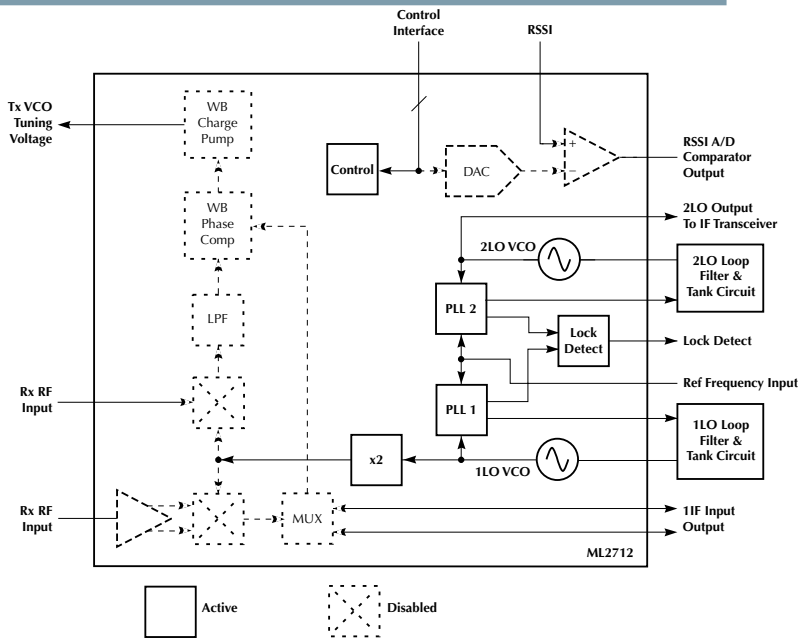


Figure 1. Standby Mode Active Circuits

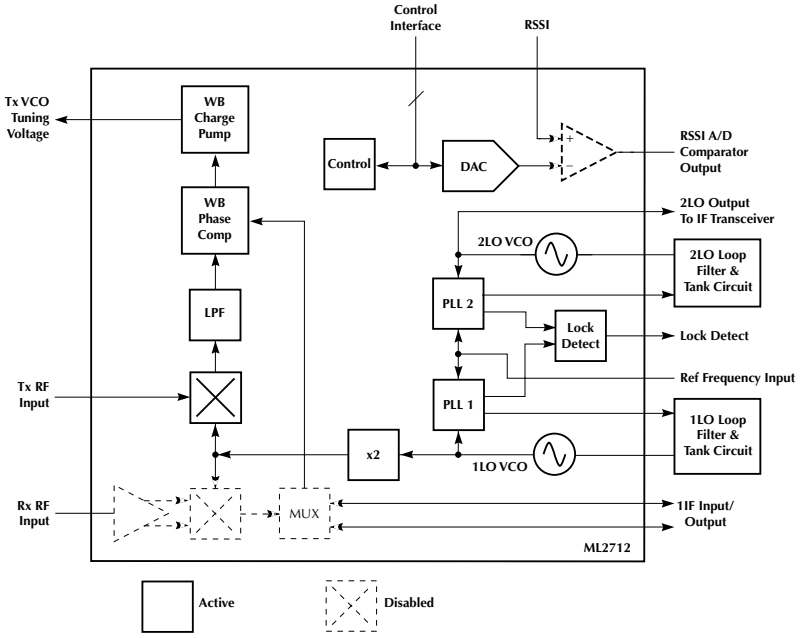


Figure 2. Transmit Mode Active Circuits

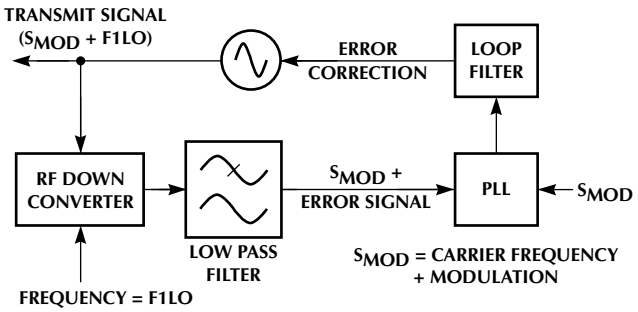


Figure 3. Directly Modulated VCO Transmitter

MODES OF OPERATION (CONTINUED)

Any modulation on S_{MOD} is duplicated at the final frequency, provided is it inside the control loop bandwidth. The spectrum of S_{MOD} and the final output frequency are shown in Figure 4.

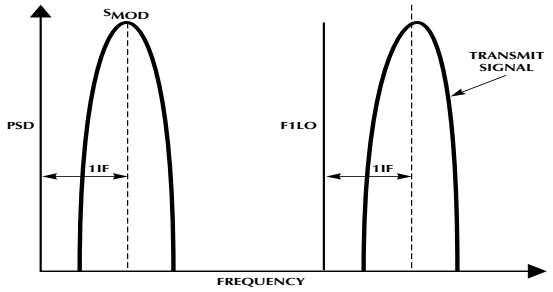


Figure 4. Simplified Spectrum of Directly Modulated VCO Transmitter

The PLL loop bandwidth is at least four times that of the modulation rate. Meeting the IEEE802.11 FHSS specification for 1Msymbol/sec requires a PLL control loop bandwidth greater than 4MHz. To achieve the Wideband PLL dynamics and the RF channel spacing requirements, the Transmit VCO is down converted with the 1LO signal (at Frequency F1LO). The RF channel spacing can be achieved by stepping the 1LO VCO. This allows the same VCOs and PLLs to be used in both Transmit and Receive Modes. For typical WLAN operation the receive frequency and transmit frequency are the same (between frequency hops). Therefore the 1LO (and 2LO) frequencies do not require re-tuning when switching from transmit to receive. As a result the transmit to receive turn-round time is very rapid. It is determined by the power on, settling, and lock up times of the Wideband PLL. For 802.11 FH systems the requirement is less than 2µsec.

TRANSMITTER PLL

The transmitter wideband PLL is shown in Figure 5. An external VCO provides a nominal 2.45GHz signal which is coupled to the Transmit RF mixer using a directional coupler or similar external circuit. The transmiter RF mixer is used to down-convert the transmiter VCO signal using the frequency doubled 1LO VCO to produce a 260MHz (nominal) signal. This signal is fed via a low pass filter to the Wideband Phase Comparator where is it compared to the Transmit IF reference signal, supplied by the ML2713. The Wideband Phase Comparator output controls the transmit VCO via an external loop filter. The bandwidth of the Wideband Phase Comparator is high enough to enable a relatively low tolerance Transmit VCO to be used.

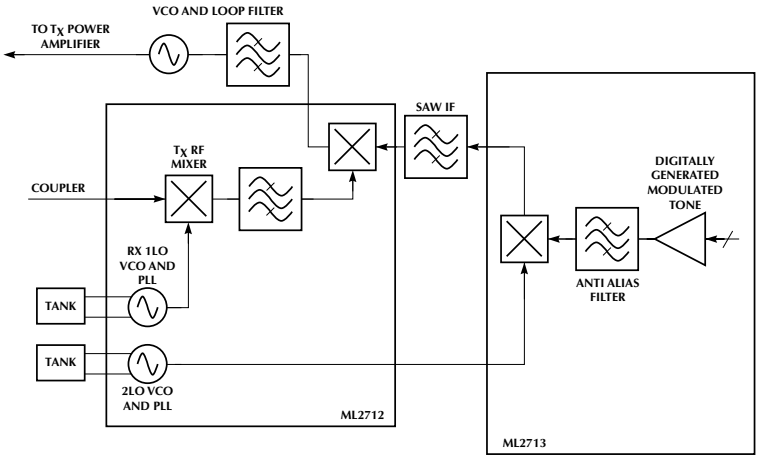


Figure 5. Wideband Phase Locked

The Transmit RF input is a single ended design with a nominal 50 ohms input impedance. The Transmit RF down-converter and Wideband PLL are only enabled in TRANSMIT Mode.

The Wideband PLL is designed to ensure the Transmit VCO is within the pull-in range of the Wideband PLL (so it will lock when transmitting), to achieve required lock up time, and to set the loop bandwidth. The Wideband PLL loop bandwidth requirement is 4 times the symbol rate at a minimum. The ML2712 is capable of loop bandwidth greater than 5MHz. Since the bandwidth of the Wideband PLL can be >4MHz, the lock up time for 802.11 applications is typically less than 2µsec. The maximum frequency pull-in range for the transmit VCO is 500MHz to ensure that the down-converted signal passes through the low pass filter.

Design of the ML2712 enables the large pull-in frequency in the Wideband PLL. When TS (Pin 47)is asserted the Wideband charge pump output is first clamped to mid-rail. A PFD detector is then used to ensure frequency lock. Finally the output switches to an XOR detector for accurate phase tracking. After TS is asserted WBCP is clamped to a nominal voltage of mid rail of VQWB (the charge pump supply voltage) for 0.25µsec for 16MHz and 32MHz at the reference input, or 0.2µsec for 20MHz or 40MHz. This pulls the VCO to mid range.

When the clamp is disabled a phase frequency detector (PFD) pulls the VCO to frequency lock for 1µsec with 16 MHz and 32MHz reference input, or 0.8µsec with 20MHz or 40MHz reference input. This rapidly pulls the VCO to frequency lock.

If the Wideband bit (Control Word B b11) is set low, the PFD is then disabled and an XOR phase detector is used until the TS signal is de-asserted. A factor of four difference between the PFD and XOR charge pump currents keeps KD, the phase detector gain, constant. The PFD charge pump current is nominally 2mA and the XOR charge pump current is nominally 0.25mA.

A lock detect output from the Wideband PLL indicates Frequency Lock. An indication of the transmitter not locked is required by some regulatory authorities.

MODES OF OPERATION (CONTINUED)

RECEIVE MODE

The circuits active in RECEIVE Mode are shown in Figure 6. All the transmitter circuits are normally disabled in this mode.

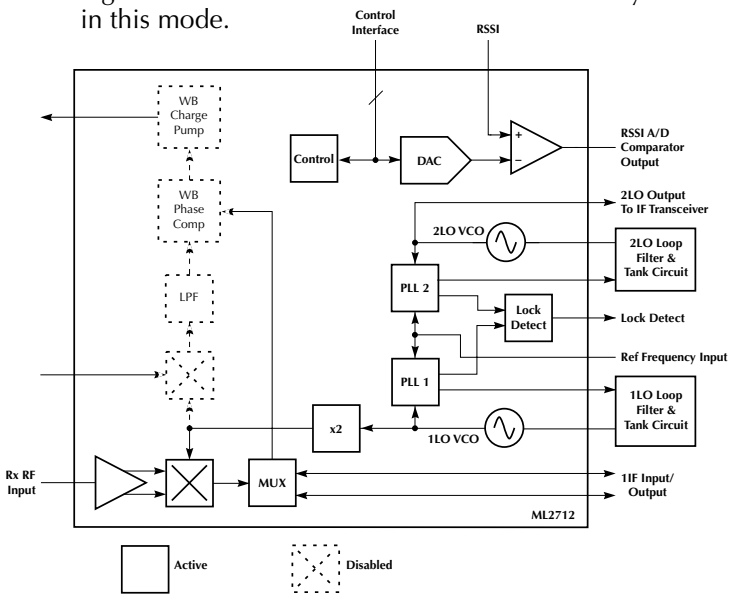


Figure 6. Receive Mode Active Circuits

RECEIVE RF DOWN-CONVERTER

The Receive RF input amplifier converts the single ended RF input to a differential signal which is then fed to a mixer. The amplifier and mixer combination down-converts the received RF signal to the receiver 1LO IF (1IF), which is optimized for 260MHz. The output of the down-converter is differential with 340Ω of output impedance suitable for low loss matching to an external SAW IF filter. The 1IF output ports are bidirectional and are multiplexed with the transmit reference IF input.

PLL & VCO CIRCUITS

Two independently programmable PLL circuits control the 1LO and 2LO VCO frequencies. These are programmed via the Serial Control Bus (DATA, CLK, and ENABLE). Program words are clocked into divider or control circuits when ENABLE is asserted. The programming is operational whether the ML2712 is in SLEEP, STANDBY, RECEIVE or TRANSMIT Mode.

The reference signal, REF (Pin 10) typically from an external crystal oscillator, is fed to a programmable reference divider with programmable division ratios of 40, 32, 20 and 16. The reference divider output is fed to both the 2LO and the 1LO phase/frequency detectors.

The polarity of the charge pump output current pulse is programmable to give a positive or negative frequency/ voltage control. The value of the current pulses is programmable via the Serial Control Bus. (See Table 7 and 10)

1LO VCO

The 1LO VCO operates at approximately 1.1GHz, and is doubled to a final frequency of 2.2GHz. The 1GHZ VCO signal is connected to the 1LO PLL circuits. The VCO requires an external differential tank circuit design to reduce the effects of frequency pulling due to signal coupling. The tank circuit is tuned by the charge pump output QP1(Pin 13) using a passive external loop filter.

The active circuitry for the 1LO VCO is a differential cross-coupled pair providing a negative resistance across the tank circuit to maintain oscillation. The tank circuit must provide a DC path to $RVCC_2$ (Pin 21). The layout of this circuit must be kept symmetric to minimize interference or coupling from other circuits in the radio.

2LO VCO

The 2LO VCO requires an external tank circuit and loop filter. The 2LO VCO is phase locked to provide a fixed frequency, nominally 236MHz. The differential pair 2LO (Pin41) and 2LOB (Pin 40) providedrive to the ML2713. The 2LO differential outputs are from the collectors of a differential pair that require a pull-up to a nominal 2.3V, normally provided by the ML2713.

A calibration tone added to the 2LO output in STANDBY Mode is intended for aligning filters and discriminators in the IF circuits of the ML2713. The calibration tone is an 8MHz square wave with a 16MHz or 32MHz reference input, or a 10MHz square wave with af 20MHz or 40MHz reference input.

The 2LO VCO is a cross-coupled pair, with one base connected to $RVCC_3$ (Pin 42) (2LO supply voltage). The other base is connected to an external tank circuit through T2LO (Pin 43). This design presents a negative impedance across the tank circuit. Since a dominant oscillation, due to bond wire inductance and parasitic capacitance on the PCB, can lead to high frequency oscillation (of the order of 1GHz), the circuit must be carefully laid out. The 2LO tank circuit must provide a DC path from T2LO to $RVCC_3$ (Pin 42).

MODES OF OPERATION (CONTINUED)

OVERVIEW OF PLLS

Control words programmed via the Serial Control Bus set the ML2712 PLL reference frequency divider,and the 2LO PLL and 1LO PLL signal dividers division ratios. For illustration a simple PLL is shown in Figure 7.

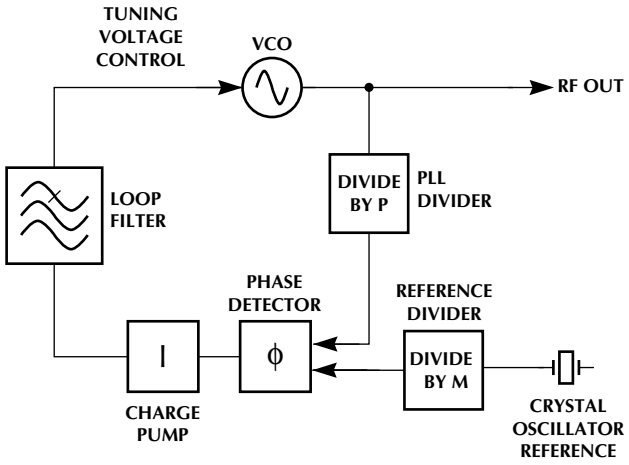


Figure 7. Simple PLL

The simplified signal divide by P (Figure 7) uses a dual modulus (or swallow pulse) prescaler system.

Figure 8 shows a dual modulus signal divider. This type of PLL is able to divide by two integers, N and N+1. ND & NS, are clocked in parallel by pulses from the prescaler, which is initially set to N+1. The ND & NS registers are programmed via the Serial Control Bus. The signal divider ratio achieved by this system is given by the equation:

$R_{SD} = N \times ND + NS$. ND must be greater than NS.

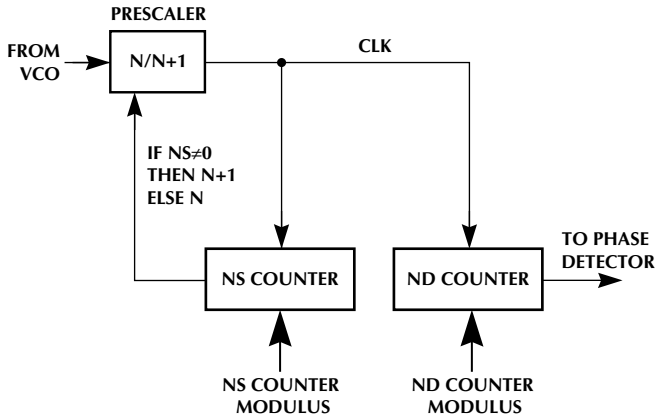


Figure 8. Dual Modulus Signal Divider

The output of the signal divider is compared with the 500 kHz comparison frequency from the reference divider in the phase detector. In the PLL (Fig. 8) the tuning voltage to the VCO is adjusted until phase locking occurs. At this point the VCO frequency in MHz will be given by the equation:

$f = (N \times ND + NS) \times (f_R/M)$.

Note that since both PLL signal divider and reference divider are subject to an extra divide by two stage, they may be neglected in the equations. However, it is important to note that the comparison frequency in MHz in both the 1LO and the 2LO PLL is given by $f_C = f_R/2M$.

DAC AND RSSI COMPARATOR

The DAC can be used to generate a voltage output to control the transmit power in an external power amplifier (PA). The DAC and Comparator can also be used to form an RSSI threshold circuit or an RSSI tracking A/D in conjunction with external baseband circuits. The DAC is programmed via the Serial Control Bus using either the DACEN or the EN control line. The DAC may be programmed at serial clock rates up to 16MHz.

SLEEP MODE

In SLEEP Mode only the control circuits are active. These circuits are static CMOS and consume minimal current when there is no interface activity.

CONTROL INTERFACES

OPERATING MODE CONTROL

A parallel control interface dynamically controls the four different Modes of operation. The control lines TS (Pin 47), RS (Pin 48) and LOE (Pin 46) enable the PLLs, VCOs, transmitter and receiver circuits. The relationship between this control interface, the Modes of operation and the functioning of the circuits are described in Table 1. The function of this control interface can be duplicated via the Serial Control Bus, and the circuits enabled in STANDBY, RECEIVE and TRANSMIT can be programmed via the Serial Control Bus.

RS	TS	LOE	Mode	IC Status
High	High	High	SLEEP	All radio circuits are off. Static CMOS control circuits are active, consuming minimal current but permitting the register settings to be changed via the baseband controller IC. Registers store power-up default or previously programmed values on serial control lines. The baseband IC may configure the radio, while the radio is neither transmitting nor receiving data, but the ML2712 will maintain the last programmed values. Note that in SLEEP Mode the operating Mode control may be overridden by the Serial Control Bus if parallel control interface is not required.
High	High	Low	STANDBY	Only the VCO and PLL circuits are enabled in this mode and will be locked within 150µsec. This will be flagged by an LD (lock detect) signal. The frequency divide ratio settings will cause the two PLLs to lock to the desired frequencies. In this mode the 2nd LO output signal can have a calibration signal added to the 2LO VCO signal. This calibration signal is used for discriminator alignment on the ML2713. The 8 bit DAC and associated comparator circuit are enabled.
Low	High	Low	RECEIVE	The Receive RF down-converter, 1LO PLL & VCO, 2LO PLL & VCO, RSSI DAC, and RSSI comparator are all enabled, although for maximum flexibility any of these circuits could be disabled via the Serial Control Bus.
High	Low	Low	TRANSMIT	The Transmit RF down-converter, Wideband PLL, 1LO PLL & VCO, 2LO PLL & VCO, and RSSI D/A are all enabled, although for maximum flexibility any of these circuits could be disabled via the Serial Control Bus

Table 1. Operating Mode ControlStates

CONTROL INTERFACES (CONTINUED)

SERIAL CONTROL BUS

The ML2712 contains two 3-wire serial control interfaces. They have common clock and data, but separate latch enable controls (EN & DACEN). The EN signal programs the registers that determine the operation of the PLLs, VCOs and DAC, and determines which circuits are active in STANDBY, RECEIVE and TRANSMIT Modes. The DACEN signal is dedicated to DAC programming only. Serial bus control is active in all operating Modes. The serial control interface overrides the parallel mode control interface. See Table 2 and Figure 9.

All DATA bits are clocked into the ML2712 while EN or DACEN is low and loaded into the addressed latch on the low to high trailing edge of the EN or DACEN pulse. The serial bus control register only retains the last 16 bits of data that follow either the EN or DACEN pulse. The data latches are fully static CMOS and use minimal power when the Serial Control Bus is inactive.

All Serial Control Bus words are entered data MSB first. The word is made up of data and address fields. The data field is the leading 13 bits and the last 3 bits are the address field (see Table 3). The address field determines the destination register for the data field. There are 5 control registers (CONTROL WORDs A, B, C, D, and E) defined in Table 4. When data is latched by a DACEN pulse the address field is ignored and the data field is always used to program the 8-bit DAC. In Tables 3 and 4 the left-most bit isalways the MSB.

EN or DACEN are enabled to latch data into the DAC register as determined by the DCE control bit, b4 in Control Word B. When DCE is set to 0, the default power up state, the EN latch enable pulse is active and the DACEN pulse is disabled. In this state a rising edge on EN will write data to the 8-bit DAC when the address field is correct. Other control words may be written using different address fields as shown in Table 4. When DCE is set to 1 both DACEN and EN pulses are active and either may be used to latch control words, although not simultaneously. In this mode DACEN will write data to the 8-bit DAC regardless of the address data. The EN pulse will continue to operate as described for DCE set to 0.

The ML2712 default power up condition is designed for normal operation. At power up the registers are programmed as in Table 4. The user may adjust the mode of operation for specific tasks by programming the control register settings immediately after power up, or at an appropriate time during operation. Note that address field 000 is reserved for test modes and should not be programmed in normal operation.

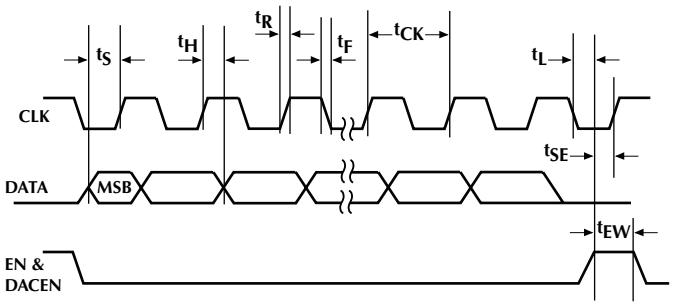


Figure 9. Control Bus Timing

	Parameter	Min	Typ	Max	Units
CLK					
t_R	Rise time			15	ns
t_F	Fall time			15	ns
t_{CK}	Period	50			ns
EN & DACEN					
t_{EW}	Pulse width	2			ns
t_L	Falling edge delay	15			ns
t_{SE}	Rising edge setup	15			ns
DATA					
t_S	Data-to-Clock Setup	15			ns
t_H	Data-to-Clock Hold	15			ns

Table 2. Three Wire Bus Interface Timing Characteristics

Field	DATA													ADDRESS		
bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Function	Data 12	Data 11	Data 10	Data 9	Data 8	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0	Add 3	Add 2	Add 1

Table 3. Format of Serial Control Bus data

CONTROL INTERFACES (CONTINUED)

Data	b0	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12	b13	b14	b15
Control Word A	VC1	VC2	PLL1	PLL2	CP1	CP2	PP1	PP2	LD1	LD2	PPW	PB	x			
Power Up Default	1	1	1	1	1	1	1	1	1	1	1	1	x	0	0	1
Control Word B	TX	RX	LBC	DAC	DCE	COM	CI1	CI2	CI3	CI4	CAL	WB	x			
Power Up Default	0	0	0	1	0	1	1	1	1	1	1	1	x	0	1	0
Control Word C	MSB 1LO ND1 Counter LSB						MSB 1LO NS1 Swallow Counter LSB						x	Address		
Power Up Default	1	1	0	1	1	0	0	1	0	1	0	0	x	0	1	1
Control Word D	MSB 2LO ND2 Counter					2LO NS2 Counter MSB LSB				Reference Div.			x	Address		
Power Up Default	1	0	0	0	0	1	1	0	0	0	0	1	x	1	0	0
Control Word E	x	x	x	x	MSB 8-bit DAC Voltage LSB								x	Address		
Power Up Default	x	x	x	x	0	0	0	0	0	0	0	0	x	1	0	1

Table 4. Control Word Settings on the Serial Control Bus

Control Bit in CONTROL WORD A						ML2712 Circuits Enabled					
VC1	**VC2**	**PLL1**	**PLL2**	**CP1**	**CP2**	**1LO VCO**	**2LO VCO**	**1LO PLL**	**2LO PLL**	**1LO Charge Pump**	**2LO Charge Pump**
0	0	0	0	0	0	ALL OFF					
1	x	x	x	x	x	ON	x	x	x	x	x
x	1	x	x	x	x	x	ON	x	x	x	x
x	x	1	x	x	x	x	x	ON	x	x	x
x	x	x	1	x	x	x	x	x	ON	x	x
x	x	x	x	1	x	x	x	x	x	ON	x
x	x	x	x	x	1	x	x	x	x	x	ON
1	1	1	1	1	1	ALL ON (DEFAULT POWER UP CONDITION)					

Table 5. VCO, PLL and Charge Pump Power Control Modes

CONTROL WORD A

Control Word A enables the VCOs, PLL dividers, PLL charge pumps and voltage reference circuits; programs the polarity of PLL charge pumps; and programs the function of the Lock Detect (LD) output.

Control Bits VC1, VC2, PLL1, PLL2, CP1, CP2

Two frequency synthesizers, 1LO and 2LO, each contain a VCO and a PLL. This dual conversion superheterodyne receiver uses the two local oscillators to down convert the 2450 MHz ISM Band RF signal. (Table 5).

All these circuit components are enabled individually using CONTROL WORD A as defined in Table 4. For the PLLs to operate, all control bits must be set to 1.

CONTROL INTERFACES (CONTINUED)

Control Bits LD1 & LD2

The PLLs indicate their lock status using the Lock Detect output (LD Pin 3). Control bits LD1 & LD2 program the indication of frequency lock on 1LO, 2LO, or both 1LO and 2LO, as shown in Table 6.

Control Mode		LO Status			
LD1	LD2	1LO	2LO	LD Pin output	Mode of Operation
0	0	x	x	1	Output disabled
0	1	unlocked	unlocked	0	1LO lock indication
0	1	locked	unlocked	0	
1	unlocked	locked	0	1	
locked	locked				
1	0	unlocked	unlocked	0	2LO lock indication
1	0	locked	unlocked	0	
1	0	unlocked	locked	1	
1	0	locked	locked	1	
1	1	unlocked	unlocked	0	2LO & 1LO lock indication
1	1	locked	unlocked	0	
1	1	unlocked	locked	0	
1	1	locked	locked	1	

Table 6. Lock Detect Mode

Control Bits PP1, PP2 & PPW

In each PLL a charge pump or switched current source either sinks or sources a current pulse depending on the error signal at the phase detector. Iif the divided VCO frequency at the phase detector is greater than the reference frequency, the charge pump will source a current pulse. The current pulse is fed to an external loop filter serving as an integrator or current reservoir. The result is the voltage across the loop filter and the tuning voltage to the VCO increasing or decreasing depending on the loop filter being referenced to ground or the power supply. The polarity of charge pumps within the PLL and transmit wideband PLL (WBPLL) may be programmed using CONTROL WORD A as shown in Table 7. The charge pump current settings in Table 10 assume that the external loop filter is reference to ground.

Control Bit PB

A band-gap voltage reference is used to control bias levels. Control Bit PB in CONTROL WORD A controls this internal voltage reference. For any circuits to operate, other than the control interfaces, this bit must equal 1.

CONTROL WORD B

Control Word B changes the control mode in which ML2712 operates. CONTROL WORD B may also be used to program charge pump current level and enable the DAC, Comparator & calibration circuits.

Control Bits TX, RX & LBC

The Mode of operation can be controlled via the serial interface (which disables the parallel operating mode interface). This option reduces the pin count requirement for a baseband controller. Individual circuit blocks may all be toggled on or off using control words. Extra control mode bits, TX & RX in CONTROL WORD B, are provided to enable transmit and receive switching via the Serial Control Bus interface. These control bits are enabled by the LBC control bit as shown in Table 8. Individual circuit blocks may be controlled by the Serial Control Bus control interface during LBC = 1 mode. When LBC = 1 the control lines TS (pin 47) and RS (pin 48), are ignored and the Mode of operation is determined by the TX and RX bit in Control Word D.

Control Bit in CONTROL WORD B			Control Status
TX	RX	LBC	
X	X	0	Parallel Control Interface (Default Power on condition)
0	0	1	Serial control - Tx & Rx circuits off
0	1	1	Serial control - Rx circuits on
1	0	1	Serial control - Tx circuits on
1	1	1	Serial control - Tx & Rx circuits off

Table 8. Parallel Control Over-Ride Using LBC Bit

Control Bit in CONTROL WORD A			ML2712 Charge Pump Polarity		
PP1	PP2	PPW	1LO Charge pump polarity	2LO Charge pump polarity	WBPLL Charge pump polarity
1	x	x	Frequency signal > Frequency ref. Pump high	x	x
0	x	x	Frequency signal > Frequency ref. Pump low	x	x
x	1	x	x	Frequency signal > Frequency ref. Pump high	x
x	0	x	x	Frequency signal > Frequency ref. Pump low	x
x	x	1	x	x	Frequency signal > Frequency ref. Pump high
x	x	0	x	x	Frequency signal > Frequency ref. Pump low

Table 7. Charge Pump Polarity

CONTROL INTERFACES (CONTINUED)

Control Bits DAC, COM & DCE

The DAC and comparator may be used as a tracking ADC circuit. In normal operation these circuits are available in TRANSMIT, RECEIVE & STANDBY operating Modes. However, independent control of the comparator and DAC is available via control bits as shown in Table 9. There are two other modes available to program the DAC. When DCE in CONTROL WORD B is set to 0, EN is active and DACEN is disabled. With DCE at 1 both the DACEN and EN pins are active. DACEN and EN cannot be simultaneously low. With DCE at 1 a rising edge on DACEN will write data to the 8-bit DAC regardless of the address data.

Control Bit in CONTROL WORD B		Circuits Enabled
DAC	COM	
1	1	DAC & Comparator on (Default power up state)
0	1	DAC off, Comparator on
1	0	DAC on, Comparator off
0	0	DAC & Comparator off

Table 9. Control of ML2712 DAC & Comparator

Control Bits CI1, CI2, CI3, CI4

The PLLs each contain a charge pump. The magnitude of the current in these pumps may be controlled as defined in Table 10. The recommended values for best phase detector performance are [CI1,CI2]=[1,0] or [1,1] and [CI3,CI4] = [1,0] or [1,1].

Control Bit CAL

The ML2713 companion to the ML2712 contains self-aligning filter and discriminator circuits. The alignment of these circuits is designed to take place when the ML2712/ ML2713 chipset is in STANDBY Mode (Table 1). Under power up default conditions in STANDBY Mode the ML2712 provides an 8 MHz calibration tone to the ML2713 via the 2LO output (pins 2LO & 2LOB). This will happen while the 1LO and 2LO local oscillators are phase locking. However, the CAL tone may be disabled using CONTROL WORD B (See Table 11).

Control Bit in CONTROL WORD B				Charge Pump Setting	
CI1	CI2	CI3	CI4	1LO Charge pump current (mA)	2LO Charge pump current (mA)
0	0	x	x	0.25	x
0	1	x	x	0.5	x
1	0	x	x	1	x
1	1	x	x	2	x
x	x	0	0	x	0.25
x	x	0	1	x	0.5
x	x	1	0	x	1
x	x	1	1	x	2

Table 10. Charge Pump Currents

CAL bit in CONTROL WORD B	Calibration Mode
0	Calibration output to 2LO disabled
1	Calibration tone to 2LO port enabled (Default power up mode)

Table 11. Control of Calibration Tone Generation

WB bit in CONTROL WORD B	Calibration Mode
1	Wideband PLL phase Dual PFD & XOR mode
0	Wideband PLL phase In XOR only mode

Table 12. Control of CalibrationTone Generation

CONTROL INTERFACES (CONTINUED)

CONTROL WORD C

2LO ND & NS counters are denoted as ND2 & NS2. The binary weighted modulus values are loaded using CONTROL WORD C as shown in Table 13. The prescaler used in the 2LO PLL is a 14/15 dual modulus type giving the 2LO frequency in MHz as $f_{2LO} = (14 \times ND2 + NS2) \times (f_{REF} /M)$.

The reference divider ratio M is also set in CONTROL WORD C (Table 4)

Control Bit CONTROL WORD C		Reference Division Ratio M	
b9	b10	b11	
0	0	0	16
0	0	1	32 (Power up Default)
0	1	0	20
0	1	1	40

Table 13. Reference Division Ratio

CONTROL WORD D

The 1LO PLL is a dual modulus type as described above. 1LO ND & NS counters are denoted in ML2712 as ND1 & NS1. Modulus values are binary weighted and are loaded using CONTROL WORD D as shown in Table 4. The prescaler used in the 1LO PLL is a 40/41 dual modulus type giving the 1LO frequency in MHz as

$f1LO = (40 \times ND1 + NS1) \times (f_{REF} /M)$.

CONTROL WORD E

The 8-bit DAC and Comparator form a tracking Analog-to-Digital converter (ADC) intended to connect to the RSSI (Receive Signal Strength Indicator) on the ML2713.

The tracking ADC is represented in Figure 10. CONTROL WORD E is used to program a voltage into the 8-bit DAC setting up a voltage on the inverting terminal of the Comparator. If the RSSI voltage exceeds that on the DAC then RSSITH signals logic high.

Typically, a baseband IC will be used to program RSSI values into the ML2712 corresponding to a known receive signal level. The RSTH value (high/low) is sensed by the baseband IC to determine if the signal strength threshold has been exceeded. By successively programming the 8-bit DAC using CONTROL WORD E the baseband IC can measure the RSSI voltage closely.

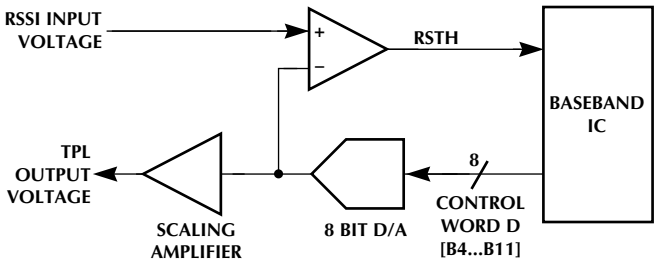


Figure 10. Charge Pump Polarity

Alternatively, the DAC may be programmed with a threshold value that when exceeded triggers the baseband IC into receive mode. In this mode the DAC and Comparator are used to provide the necessary circuits for Clear Channel Assessment (CCA) as defined in IEEE 802.11. Figure 11 shows the relationship between RSSI DAC code (in decimal) programmed into ML2712 via CONTROL WORD E and the DAC RSSI voltage threshold.

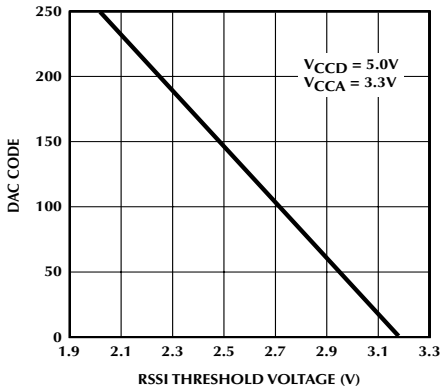


Figure 11. Parallel Control Over-Ride Using LBC Bit

The DAC also has a general purpose use. The DAC voltage programmed using CONTROL WORD E is fed to scaling circuit before appearing externally at TPL. While the DAC output is suitable for general use, a likely use for the voltage is for transmit power control. In this mode of operation the DAC voltage corresponding to the required transmitter output power can be programmed before transmit operation. The relationship between TPL voltage versus DAC programming is shown in Figure 12.

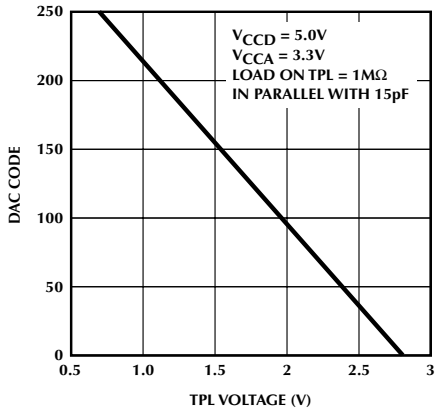


Figure 12. Control of ML2712 DAC Comparator

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

VCC_1 ..... 6.0V
VCC_2, $RVCC_1$, VCC_3, $RVCC_2$, VCC_4, VCC_8 , VCC_5 , VCC_6 , $RVCC_3$ ..... -0.3V to VCC_1 + 0.3V
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10s) ..... 260°C

OPERATING CONDITIONS

Commercial Temperature Range ..... 0°C to 70°C
Extended Temperature Range ..... -20°C to 70°C
VCC_1 Range ..... 3.0V to 5.5V
VCC_2Range ..... 3.3V ± TBD%
Thermal Resistance (θ_{JA}) (Note 2) ..... 100°C/W

ELECTRICAL TABLES

Unless otherwise specified, VCC_1 = 5V, VCC_2, $RVCC_1$, VCC_3, $RVCC_2$, VCC_4, VCC_8, VCC_5, VCC_6, $RVCC_3$ = 3.3V, T_A = Operating Temperature Range. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER CONSUMPTION TRANSMIT AND RECEIVE RF						
	All Circuits, Sleep Mode	DC Connected		10		µA
	Supply Current, Standby Mode			61		mA
	Supply Current, Receive Mode			66		mA
	Supply Current, Transmit Mode			94		mA
INTERFACE LOGIC LEVELS						
	Input High			V_{CCD}		V
	Output Low			0		V
	Input Bias Current	All States		±5		µA
	Input Capacitance	(Not Tested)		4		pF
	Lock Detect Output Low	I_{SINK} = 0.5mA		0.4		V
MODE CONTROL PINS						
	Time, Sleep to Standby, PLLs Locked (Note 3)	From LOE Asserted to 1LO and 2LO Within 20KHz of Final Frequency		150		µs
	PLL Lockup Time, Standy & Receive (Note 3)	From EN Asserted to 1LO and 2LO Within 20KHz of Final Frequency		150		µs
	Time, Standby to Receive	Time from RS Asserted to Receive RF Down Converter Enabled		1		µs
	Time, Standby to Transmit	Time from TS Asserted to Transmit RF Down Converter and Wideband PLL Enabled		1		µs
	Time, Receive to Transmit	From RS de-asserted, TS asserted and Wideband PLL & Transmit Down Converter Ready		1		µs

ELECTRICAL TABLES (CONTINUED)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Time, Transmit to Receive	From TS de-asserted, RS asserted to Receive RF Mixer Ready		1		µs
RECEIVE RF MIXER						
	Receive RF Mixer Gain			–1.5		dB
	Receive RF Mixer Noise Figure			15		dB
	Receive RF Mixer Input 1dB Gain Compression Point	In-band Tone		–9.5		dBm
	Receive RF Mixer Input IP3			0		dBm
	Receive RF Input Impedance	Nominal, single ended into RRFI, 1.5 pF shunt capacitor external matching		50		Ω
	Receive RF Output Impedance	Differential		340		Ω
	Receive RF Mixer Turn on Time.			1		µs
	Receive RF Mixer Turn off Time.			1		µs
RECEIVE 1LO VCO AND 1LO PLL						
	1LO Output Frequency		1060		1130	MHz
	Minimum Q for Performance Required of 1LO	Unloaded Q of Tank Circuits.		10		
	1LO, Integrated Noise, out of Receive	1MHz		–45		dBc
	Band in 1MHz Band at Offsets from	2MHz		–50		dBc
	Carrier. Integrated +/-500kHz about	3MHz		–55		dBc
	Comparison Frequency	>3MHz		–55		dBc
	1LO PLL Reference Frequency at Phase Detector			500		kHz
	1LO Division Range		2000		2260	Integer
	1LO Lock up Time for any Valid Frequency Change	From LE asserted. Maximum charge pump current		150		µs
	1LO Lock up Time from Sleep (Note 3)	PLL Dividers Programmed, Maximum Charge Pump Current		150		µs
REF	Reference Signal Input Level	Single Ended, Square Wave, Peak		V_{CCA}		mV
2LO VCO AND PLL						
	2LO frequency			236		MHz
	Frequency Pulling	Switching among Transmit, Receive and Standby.		10		kHz
	Phase Noise Double Sideband, Integrated from 5kHz to 600kHz (Note 4)			–50		dBc
	2LO, Integrated Noise, out of Receive	1MHz		–55		dBc
	Band in 1MHz Band at Offsets from	2MHz		–60		dBc
	Carrier. Integrated ±500kHz about	3MHz		–65		dBc
	Frequency	>3MHz		–65		dBc

ELECTRICAL TABLES (CONTINUED)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Output Signal level, Differential	200Ω Balanced Load		30		mV
	Reference Frequency			32 or 16		MHz
	2LO PLL Reference Frequency at Phase Detector			500		kHz
	2LO Division Ratio	Assumes 1MHz Comparison Frequency for 2LO	216		256	Integer
	2LO Lock up Time (Note 4)	From Enable 2LO to Within 10kHz of Final Frequency		100		µs
DAC						
	Resolution			8		bits
	Relative accuracy			±0.5		LSB
	Differential Non-linearity	Monotonic under all Conditions		±1		LSB
	Temperature coefficient			3		PPM/ºC
	Offset error			±3		LSB
	RSSI Voltage Conversion Range	Sensed by RSTH Comparator, DAC Code 0 to Code 255	2.0	3.2		V
	TPL Output Voltage Range	Load = 1MΩ, DAC Code 0 to Code 255	0.7	2.8		V
	Short Circuit Current			5		mA
	Output slew rate			0.15		V/µs
	Output Settling Time	To within ½ LSB		500		ns
	Signal to Noise and Distortion			50		dB
COMPARATOR						
	Output High			V_{CCD}		V
	Output Low			0.0 ±0.3		V
	Output Sink/Source Capability			4		mA
	Input Offset Error			2		mV
	Input to Output Propagation Delay	Input to Output High and Input to Output Low		500		ns
	Input Voltage Range			2		V
	RSSI Input Bias Current			20		µA
TRANSMIT RF MIXER AND WIDEBAND PHASE COMPARATOR						
	Transmit RF Input Signal Power			–10		dBm
	Transmit RF Mixer and Wideband Phase Comparator Turn on Time			1		µs
	Maximum Difference Frequency Between 1LO × 2 and Transmit VCO (Note 5)			500		MHz
	Minimum Difference Frequency Between 1LO × 2 and Transmit VCO (Note 5)			100		MHz

ELECTRICAL TABLES (CONTINUED)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Frequency of Reference Signal	Modulation on Reference	240	260	280	MHz
	Transmitter Phase Noise (Note 6)	External Transmit VCO Locked to the ILO		–126		dBc/Hz
	Transmitter Phase Noise in 1MHz Band at Offsets from Carrier. Integrated ±500kHz about Frequency.	1MHz		–50		dBc
		2MHz		–66		dBc
		3MHz		–66		dBc
		>3MHz		–66		dBc
	Lock up Time, from any Starting Transmit 1LO and Receive 1LO Frequency to <20kHz (Note 6)			2		µs
	Modulation Error (Note 7)	1MSymbol/s 2GFSK or 4GFSK to Ideal GFSK		3		kHz

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: θJA is measured with the component mounted on the Evaluation PCB in free air.

Note 3: Phase noise and lock up time tested with 1LO VCO Q = 10, kVCO = 100MHz/V. Phase noise measured at IF output by down converting a 2450MHz signal to a 260MHz IF. Input signal at –20dBm. Charge pump current set to default.

Note 4: Measurements taken with 236MHz 2LO. Tank circuit of 2LO VCO Q = 8, kVCO = 40MHz/V.Charge pump current set to maximum.

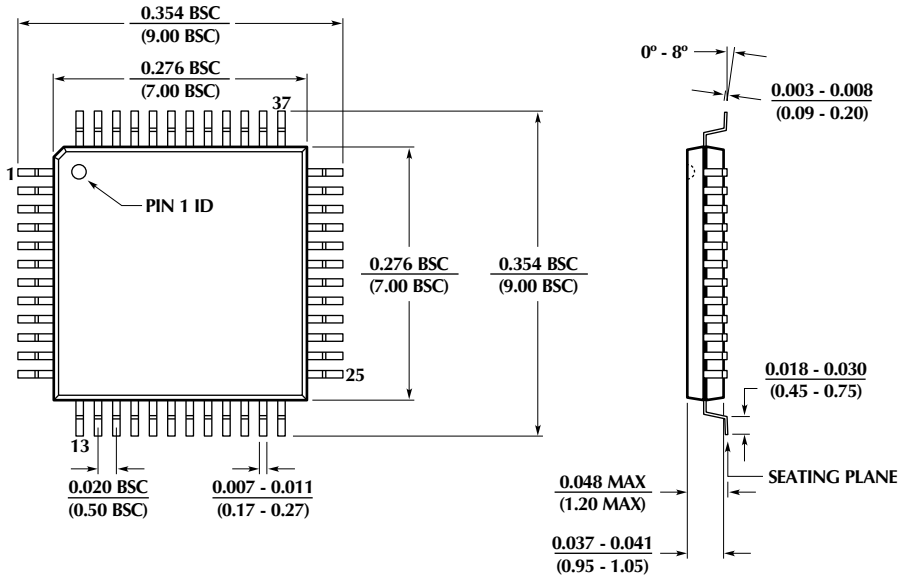
Note 5: This is proven by design, it is not tested in production.

Note 6: Measured with an external Transmit VCO, with Q = 15, kVCO = 120MHz/V, output power 0dBm, –10dBm input to TS272. Reference signal is a 260MHz sine wave.

Note 7: Measured with an external Transmit VCO, with Q = 15, kVCO = 120MHz/V, output power 0dBm, –10dBm input to TS272. Reference is a 260MHz center frequency signal, modulated with 4GFSK. Error is measured relative to the reference signal at the center of the data symbol.

PHYSICAL DIMENSIONS

Package: H48-7
48-Pin (7 x 7 x 1mm) TQFP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2712CH	0°C to 70°C	48 Pin TQFP 7mm body
ML2712EH	-20°C to 70°C	48 Pin TQFP 7mm body

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