FEDL60851E-02
Issue Date: Dec. 16, 2002

OKI Semiconductor

ML60851E

USB Device Controller

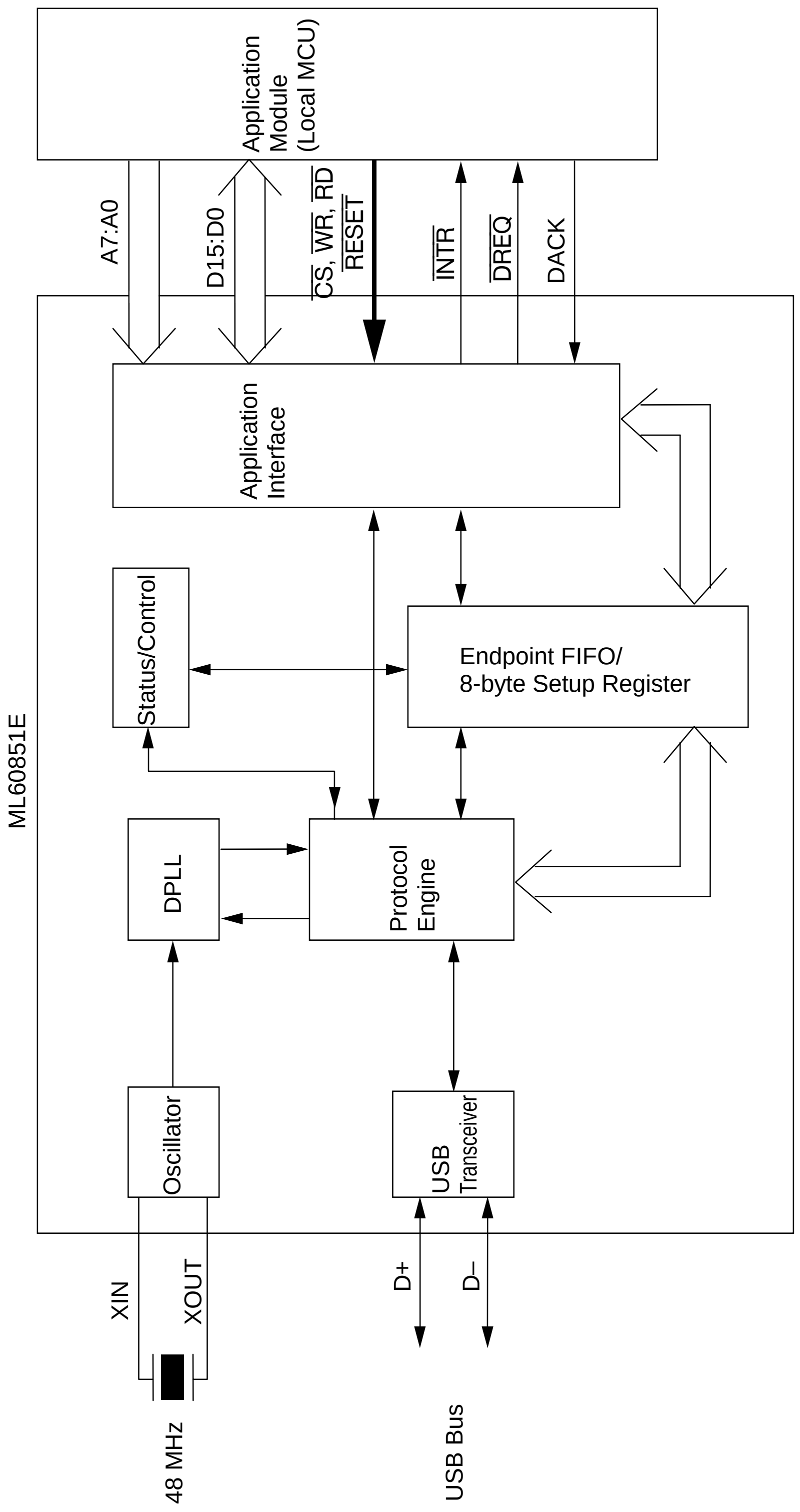
GENERAL DESCRIPTION

The ML60851E is a general purpose Universal Serial Bus (USB) device controller. The ML60851E provides a USB interface, control/status block, application interface, and FIFOs. The FIFO interface and two types of transfer have been optimized for BulkOut devices such as printers and BulkIn devices such as digital still cameras and image scanners. In addition, Mass Storage devices are also applicable to this device.

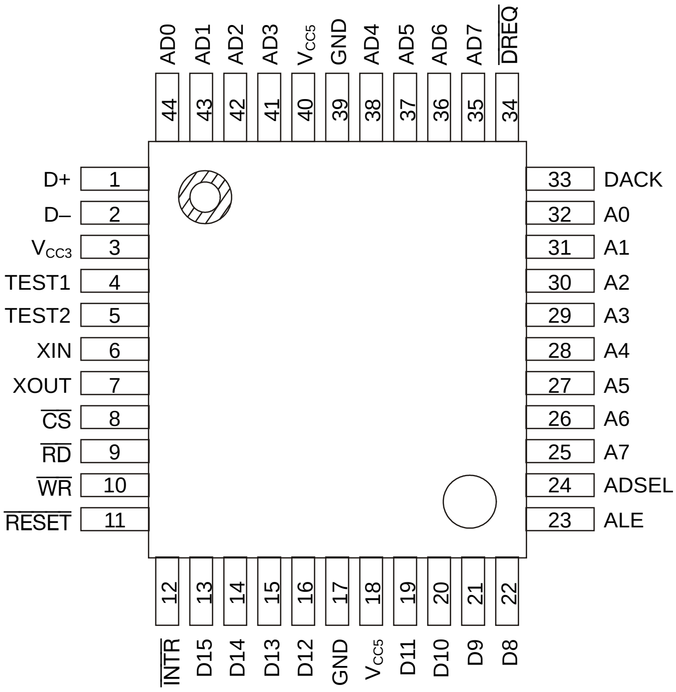
FEATURES

- USB 2.0 compliant
- Built-in USB transceiver circuit
- Full-speed (12 Mb/sec) support
- Supports printer device class, image device class, and Mass Storage device class
- Supports three types of transfer; control transfer, bulk transfer, and interrupt transfer
- Built-in FIFOs for control transfer
  Two 8-byte FIFOs (one for receive FIFO and the other for transmit FIFO)
- Built-in FIFOs for bulk transfer (available for either receive FIFO or transmit FIFO)
  One 64-byte FIFO
  Two 64-byte FIFOs
- Built-in FIFO for interrupt transfer
  One 8-byte FIFO
- Supports one control endpoint, two bulk endpoint addresses, and one interrupt endpoint address
- Two 64-byte FIFOs enable fast BulkOut transfer and BulkIn transfer
- Supports 8 bit/16 bit DMA transfer
- Supports protocol stall
- V_{CC} is 3.0 to 3.6 V
- Supporting dual power supply enables 5 V application interface
- Built-in 48 MHz oscillator circuit
- Package options:
  44-pin plastic QFP (QFP44-P-910-0.80-2K)(ML60851EGA)
  44-pin plastic TQFP (TQFP44-P-1010-0.80-K)(ML60851ETB)

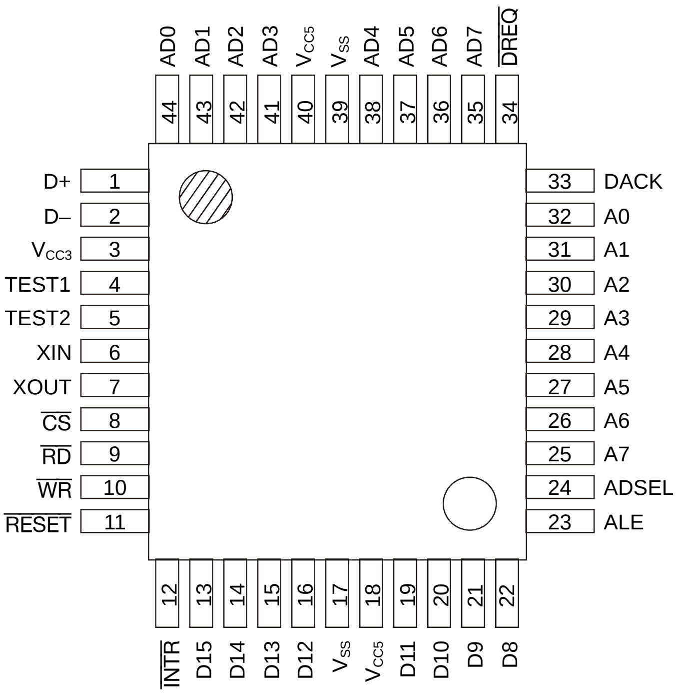
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP



44-Pin Plastic TQFP

PIN DESCRIPTION

Pin	Symbol	Type	Description
1, 2	D+, D–	I/O	USB data
6, 7	XIN, XOUT	—	Pins for external crystal oscillator
4, 5	TEST1, 2	I	Test pins (normally “L”)
13 to 16, 19 to 22	D15 to D8	I/O	Data bus (MSB)
35 to 38, 41 to 44	AD7 to AD0	I/O	Data bus (LSB)/address inputs
25 to 32	A7 to A0	I	Address inputs
8	$\overline{CS}$	I	Chip select signal input pin. LOW active
9	$\overline{RD}$	I	Read signal input pin. LOW active
10	$\overline{WR}$	I	Write signal input pin. LOW active
12	$\overline{INTR}$	O	Interrupt request signal output pin
34	$\overline{DREQ}$	O	DMA request output pin
33	DACK	I	DMA acknowledge signal input pin
23	ALE	I	Address latch enable signal input pin
24	ADSEL	I	Address input mode select input pin. “H”: address/data multiplex
11	$\overline{RESET}$	I	System reset signal input pin. LOW active.

INTERNAL REGISTERS

Addresses and Names of Registers

Addresses			Register		Page
A5:A0	Read A7, A6	Write A7, A6	Symbol	Register name	
00h	01b	—	EP0RXFIFO	Endpoint 0 Receive FIFO Data	7
01h	01b	—	EP1RXFIFO	Endpoint 1 Receive FIFO Data	7
02h	01b	—	EP2RXFIFO	Endpoint 2 Receive FIFO Data	8
03h	01b	—		Reserved	
00h	—	11b	EP0TXFIFO	Endpoint 0 Transmit FIFO Data	9
01h	—	11b	EP1TXFIFO	Endpoint 1 Transmit FIFO Data	9
02h	—	11b	EP2TXFIFO	Endpoint 2 Transmit FIFO Data	10
03h	—	11b	EP3TXFIFO	Endpoint 3 Transmit FIFO Data	10
00h	11b	01b	DVCADR	Device Address Register	11
01h	11b	01b	DVCSTAT	Device Status Register	11
02h	11b	—	PKTERR	Packet Error Register	13
03h	11b	—	FIFOSTAT1	FIFO Status Register 1	13
04h	11b	—	FIFOSTAT2	FIFO Status Register 2	14
08h	11b	01b	PKTRDY	Endpoint Packet-Ready Register	15
09h	11b	—	EP0RXCNT	Endpoint 0 Receive-Byte Count Register	19
0Ah	11b	—	EP1RXCNT	Endpoint 1 Receive-Byte Count Register	19
0Bh	11b	—	EP2RXCNT	Endpoint 2 Receive-Byte Count Register	20
0Ch	11b	—		Reserved	
0Dh	11b	—	REVISION	Revision Register	21
0Eh	—	01b	CLRFIFO	Transmit FIFO Clear Register	21
0Fh	—	01b	SYSCON	System Control Register	22
10h	11b	—	bmRequest Type	BmRequest Type Setup Register	23
11h	11b	—	bRequest	bRequest Setup Register	23
12h	11b	—	wValue LSB	WValue LSB Setup Register	24
13h	11b	—	wValue MSB	WValue MSB Setup Register	24
14h	11b	—	wIndex LSB	WIndex LSB Setup Register	24
15h	11b	—	wIndex MSB	WIndex MSB Setup Register	24
16h	11b	—	wLength LSB	WLength LSB Setup Register	25
17h	11b	—	wLength MSB	WLength MSB Setup Register	25
1Ah	11b	01b	POLSEL	Assertion Select Register	26
1Bh	11b	01b	INTENBL	Interrupt Enable Register	27
1Ch	11b	—	INTSTAT	Interrupt Status Register	28
1Dh	11b	01b	DMACON	DMA Control Register	31
1Eh	11b	01b	DMAINTVL	DMA Interval Register	32
1Fh	—	—		Reserved	

Addresses and Names of Registers (Continued)

Addresses			Register		Page
A5:A0	Read A7, A6	Write A7, A6	Symbol	Register name	
20h	11b	—	EP0RXCON	Endpoint 0 Receive Control Register	33
21h	11b	—	EP0RXTGL	Endpoint 0 Receive Data Toggle Register	33
22h	11b	01b	EP0RXPLD	Endpoint 0 Receive Payload Register	34
23h	—	—		Reserved	
24h	11b	01b	EP1CON	Endpoint 1 Control Register	35
25h	11b	01b	EP1TGL	Endpoint 1 Data Toggle Register	36
26h	11b	01b	EP1PLD	Endpoint 1 Payload Register	36
27h	—	—		Reserved	
28h	—	—		Reserved	
29h	—	—		Reserved	
2Ah	—	—		Reserved	
2Bh	—	—		Reserved	
2Ch	—	—		Reserved	
2Dh	—	—		Reserved	
2Eh	—	—		Reserved	
2Fh	—	—		Reserved	
30h	11b	—	EP0TXCON	Endpoint 0 Transmit Control Register	37
31h	11b	—	EP0TXTGL	Endpoint 0 Transmit Data Toggle Register	37
32h	11b	01b	EP0TXPLD	Endpoint 0 Transmit Payload Register	38
33h	11b	01b	EP0STAT	Endpoint 0 Status Register	39
34h	11b	01b	EP2CON	Endpoint 2 Control Register	41
35h	11b	01b	EP2TGL	Endpoint 2 Data Toggle Register	42
36h	11b	01b	EP2PLD	Endpoint 2 Payload Register	42
37h	—	—		Reserved	
38h	11b	01b	EP3CON	Endpoint 3 Control Register	43
39h	11b	01b	EP3TGL	Endpoint 3 Data Toggle Register	44
3Ah	11b	01b	EP3PLD	Endpoint 3 Payload Register	44
3Bh	—	—		Reserved	
3Ch	—	—		Reserved	
3Dh	—	—		Reserved	
3Eh	—	—		Reserved	
3Fh	—	—		Reserved	

FUNCTIONS OF REGISTERS

End Point 0 Receive FIFO (EP0RXFIFO)

Read address	40h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	×	×	×	×	×	×	×	×
After a bus reset	×	×	×	×	×	×	×	×
Definition	EP0 Receive data (R)							

The receive data from the host computer in the data state during a control Write transfer is stored in EP0RXFIFO. The EP0 receive data can be read out by the local MCU through reading the address 40h when the ML60851E issues an EP0 receive packet ready interrupt request. It is possible to read successively the data in the packet by reading continuously.

The EP0RXFIFO is cleared under the following conditions:
1. When the local MCU resets the EP0 receive packet ready bit (A “1” is written in PKTRDY(0)).
2. When a setup packet is received.
3. When the local MCU writes a “0” in the stall bit (EP0STAT(2)).

End Point 1 Receive FIFO (EP1RXFIFO)

Read address	41h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	×	×	×	×	×	×	×	×
After a bus reset	×	×	×	×	×	×	×	×
Definition	EP1 Receive data (R)							

It is possible to read out the EP1 receive data by reading the address 41h. When EP1 is set for bulk reception (BULK OUT), The local MCU should read EP1RXFIFO when the ML60851E issues an EP1 packet ready interrupt request. It is possible to read successively the data in the packet by reading continuously. When the data transfer direction of EP1 is set as “Transmit”, all accesses to this address will be invalid.
The EP1RXFIFO is cleared under the following conditions:
1. When an OUT token is received for EP1.
2. When the EP1 receive packet ready bit is reset. (A “1” is written in PKTRDY(1).)
3. When the local MCU writes a “0” in the stall bit (EP1CON(1)).

Even when a DMA read with a 16-bit width is made from EP1RXFIFO, the address is A7:A0 = 41h.

End Point 2 Receive FIFO (EP2RXFIFO)

Read address	42h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	×	×	×	×	×	×	×	×
After a bus reset	×	×	×	×	×	×	×	×
Definition	EP2 Receive data (R)							

It is possible to read out the EP2 receive data by reading the address 42h. When EP2 is set for bulk reception (Bulk OUT), the local MCU should read EP2RXFIFO when the ML60851E issues an EP2 packet ready interrupt request. It is possible to read successively the data in the packet by reading continuously. When the data transfer direction of EP2 is set as ‘Transmit’, all accesses to this address will be invalid.

The EP2RXFIFO is cleared under the following conditions:
1. When an OUT token is received for EP2.
2. When the EP2 receive packet ready bit is reset. (A “1” is written in PKTRDY(2).)
3. When the local MCU writes a “0” in the stall bit (EP2CON(1)).

End Point 0 Transmit FIFO (EP0TXFIFO)

Read address	—
Write address	C0h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	×	×	×	×	×	×	×	×
After a bus reset	×	×	×	×	×	×	×	×
Definition	EP0 Transmit data (W)							

EP0 transmit data can be written in by writing to the address C0h. The receive data from the host in the data stage during a control read transfer is stored in EP0TXFIFO. When the ML60851E issues an EP0 transmit packet ready interrupt request, the local MCU writes the transmit data to the address C0h. It is possible to write the packet data successively by writing continuously.

The EP0 TXFIFO is cleared under the following conditions:
1. When an ACK is received from the host for the data transmission from EP0.
2. When a setup packet is received.

End Point 1 Transmit FIFO (EP1TXFIFO)

Read address	—
Write address	C1h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	×	×	×	×	×	×	×	×
After a bus reset	×	×	×	×	×	×	×	×
Definition	EP1 Transmit data (W)							

The EP1 transmit data can be written in by writing to the address C1h. When EP1 has been set for bulk transmission (BULK IN), The local MCU should write the transmit data in EP1TXFIFO when the ML60851E issues an EP1 packet ready interrupt request. It is possible to write the packet data successively by writing continuously. When the data transfer direction of EP1 is set as 'Receive', all accesses to this address will be invalid.

The EP1 transmit FIFO is cleared under the following conditions:
1. When an ACK is received from the host for the data transmission from EP1.
2. When the local MCU writes a "1" in the EP1FIFO clear bit (CLRFIFO(1)).

Even when a DMA write with a 16-bit width is made in EP1TXFIFO, the address is A7:A0 = 41h.

End Point 2 Transmit FIFO (EP2TXFIFO)

Read address	—
Write address	C2h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	×	×	×	×	×	×	×	×
After a bus reset	×	×	×	×	×	×	×	×
Definition	EP2 Transmit data (W)							

EP2 transmit data can be written in by writing to the address C2h. When EP2 has been set for bulk transmission (BULK IN), the local MCU should write the transmit data in EP2TXFIFO when the ML60851E issues an EP2 packet ready interrupt request. It is possible to write the packet data successively by writing continuously. When the data transfer direction of EP2 is set as “Receive”, all accesses to this address will be invalid.

The EP2 TXFIFO is cleared under the following conditions:
1. When an ACK is received from the host for the data transmission from EP2.
2. When the local MCU writes a “1” in the EP2FIFO clear bit (CLRFIFO(2)).

End Point 3 Transmit FIFO (EP3TXFIFO)

Read address	—
Write address	C3h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	×	×	×	×	×	×	×	×
After a bus reset	×	×	×	×	×	×	×	×
Definition	EP3 Transmit data (W)							

EP3 transmit data can be written in by writing to the address C3h. The local MCU should write the transmit data in EP3TXFIFO when ML60851E issues an EP3 packet ready interrupt request. It is possible to write the packet data successively by writing continuously.

The EP3 TXFIFO is cleared under the following conditions:
1. When an ACK is received from the host for the data transmission from EP3.
2. When the local MCU writes a “1” in the EP3FIFO clear bit (CLRFIFO(3)).

Device Address Register (DVCADR)

Read address	C0h
Write address	40h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	Device address (R/W)							

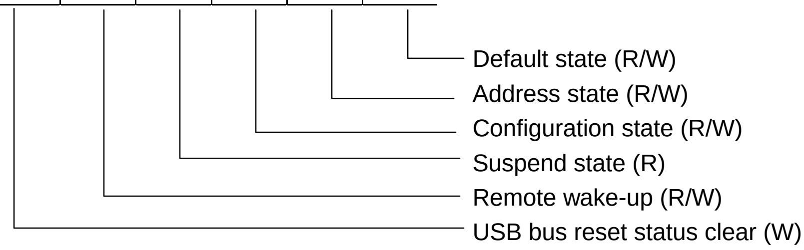
The local MCU writes in this register the device address given by the SET_ADDRESS command from the host. Thereafter, ML60851E responds only to tokens specifying this address among all the tokens from the host computer. The default value for this register, is the default address 00h (D6:D0=00) which is specified in USB specifiacations.

Note 1: It is possible to carry out addressing using a 7-bit address because up to 127 devices can be connected according to the USB standard.
Note 2: Bit D7 is fixed at “0”, and even if a “1” is written in bit D7, it will be invalid.

Device Status Register (DVCSTAT)

Read address	C1h
Write address	41h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	1
After a bus reset	0	0	0	0	0	0	0	1
Definition	0	0						



This is a register for displaying the status of the device. The functions of the different bits are described below: Bits D7 and D6 are fixed at “0” and even if a “1” is written in these bits, the write operation will be invalid.

Default state:

This bit is asserted in the initial state. The default state is valid from the time the power is switched ON and the hardware resetting is complete. There is no need to write a “0” in this bit.

Address state:

When a SET_ADDRESS request arrives, the local MCU writes the device address in the device address register. If necessary, by writing a “1” in this bit also at that time, it is possible to give an indication that the ML60851E has entered the address state. Since the content of this bit does not affect the operation of the ML60851E, there is no need to write in this bit if it will not be read out.

Configuration state:

This bit is used as an indication of whether the device has entered the configuration state. The content of this bit does not affect the operation of ML60851E and hence, it is not necessary to write to it.

If a SET_CONFIGURATION request is received from the host when the device is in the address state, the local MCU should assert the configuration bits of EP1CON, EP2CON, or EP3CON. At this time, it may be useful to write a “1” to this bit to indicate that the device has entered the configuration state.

Remarks:
When all these three states are “1”, it means that this IC is normally operating. However, since Default state bit, Address state bit and Configuration state bit do not affect the operation of the ML60851E, there is no need to write in these bits if they will not be read out.

Suspend state:

When the idle condition continues for more than 3ms in the USB bus, the ML60851E automatically asserts this bit thereby indicating that it is going into the suspend state. At the same time, bit D6 of the interrupt status register INTSTAT is asserted and the $\overline{\text{INTR}}$ pin is asserted. With this, the local MCU can suppress the current consumption.
This bit is deasserted when the EOP of any type of packet is received.

Remote wake-up:

The ML60851E is in the suspend state, the remote wake-up function is activated when the local MCU asserts this bit. When this bit is written while 5ms have not yet elapsed in the idle condition, the remote wake-up signal is output after waiting for the idle condition to continue for the full 5ms period. Further, when this bit is written after the idle condition has persisted for 5ms or more, the remote wake-up signal is output immediately after this bit is written. This bit is deasserted automatically when the suspend state is released by receiving the resume instruction over the USB bus.

USB bus reset status clear:

When the ML60851E is in the USB bus reset interrupt state (bit D5 of the interrupt status register, that is the USB bus reset interrupt status bit is “1” and the $\overline{\text{INTR}}$ pin is asserted), it is possible to clear the interrupt status by writing a “1” in this bit. (This makes the USB bus reset interrupt status bit “0” and deassertes $\overline{\text{INTR}}$.) Although this bit can be read out, the read out value will always be “0”.

Packet Error Register (PKTERR)

Read address	C2h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	0	0	0	0				

D0: Bit stuff error (R)
D1: Data CRC error (R)
D2: Address CRC error (R)
D3: PID Error (R)

Each bit is asserted when the corresponding error occurs and is deasserted when SOP is received.
This register is used to report the error information. This register is useful for the tests during development, or for preparing the error frequency measurement report. This register is not required by USB Specifications.

FIFO Status Register 1 (FIFOSTAT1)

Read address	C3h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	1	0	1	0
After a bus reset	0	0	0	0	1	0	1	0
Definition	0	0	0	0				

D0: Receive FIFO0 Full (R)
D1: Receive FIFO0 Empty (R)
D2: FIFO1 Full (R)
D3: FIFO1 Empty (R)

This register reports the status of EP0RXFIFO and the FIFO for EP1. Normally, there is no need to read this register because it is sufficient to read the packet ready status before reading out or writing in a FIFO.

Receive FIFO0 Full: This bit becomes “1” when 8-bytes of data are stored in the EP0RXFIFO. This bit is not set to “1” when a packet less than 8 bytes long (a short packet) is stored in.

Receive FIFO0 Empty: This bit will be “1” when EP0RXFIFO is empty.

FIFO1 Full: This bit becomes “1” when 64 bytes of data is stored in the FIFO for EP1. This is true during both transmission and reception. This bit does not become “1” in the case of a short packet. The FIFO for EP1 has a two-layer structure and can store up to 128 bytes of data. This bit indicates the status of the FIFO in which data is being written at that time. In other words, this bit indicates the status of the FIFO into which the host computer is writing data when EP1 is receiving data, and of the FIFO into which the local MCU is writing data when EP1 is transmitting data.

FIFO1 Empty: This bit becomes “1” when the FIFO for EP1 is empty. This is true during both transmission and reception. The FIFO for EP1 has a two-layer structure and can store up to 128 bytes of data. This bit indicates the status of the FIFO which is being read out at that time.

FIFO Status Register 2 (FIFOSTAT2)

Read address	C4h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	1	0	1	0	1	0
After a bus reset	0	0	1	0	1	0	1	0
Definition	0	0						

Transmit FIFO0 Full (R)
Transmit FIFO0 Empty (R)
FIFO2 Full (R)
FIFO2 Empty (R)
FIFO3 Full (R)
FIFO3 Empty (R)

This register reports the status of the EP0TXFIFO, the FIFO for EP2, and the FIFO for EP3. Normally, there is no need to read this register because it is sufficient to read the packet ready status before reading out or writing in a FIFO.

Transmit FIFO0 Full: This bit becomes “1” when 8-bytes of data is stored in the EP0TXFIFO. This bit is not set to “1” when a packet less than 8 bytes (a short packet) is written in.
Transmit FIFO0 Empty: This bit will be “1” when the EP0 transmit FIFO0 is empty.
FIFO2 Full: This bit becomes “1” when 64 bytes of data is either stored or written in the FIFO for EP2. This bit does not become “1” in the case of a short packet.
FIFO2 Empty: This bit becomes “1” when the FIFO of EP2 is empty.
FIFO3 Full: This bit becomes “1” when 64 bytes are written in the FIFO for EP3. This bit does not become “1” in the case of a short packet.
FIFO3 Empty: This bit becomes “1” when the FIFO for EP3 is empty.

End Point Packet Ready Register (PKTRDY)

This register indicates whether or not the preparations for reading out or writing in a packet data have been completed. In addition, this register is also used for controlling the handshake packet (ACK/NAK)

Read address	C8h
Write address	48h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition					0			

- D0: EP0 Receive packet ready (R/Reset)
- D1: EP1 Receive packet ready (R/Reset)
- D2: EP2 Receive packet ready (R/Reset)
- D4: EP0 Transmit packet ready (R/Set)
- D5: EP1 Transmit packet ready (R/Set)
- D6: EP2 Transmit packet ready (R/Set)
- D7: EP3 Transmit packet ready (R/Set)

This register in conjunction with INTENBL register is used for controlling the read/write operation of ML60851E's transmit and receive FIFOs. The interrupt generation and disassertion of ML60851E is closely related to the bits in PKTRDY register and the corresponding fields in INTENBL register.

During normal operation, when ML60851E is receiving data from the host, the data packet received succussfully without any errors will be stored in the corresponding Rx FIFO of ML60851E, at which point ML60851E will automatically assert its Receive Packet Ready bit and generate an interrupt cause. At this time if interrupt for the particular endpoint has been enabled in the INTENBL register, the corresponding interrupt status bit in register INTSTAT will be asserted and an interrupt will be generated.

In a transmit operation, when ML60851E is sending data to the host, an ACK packet received from the host in response to succussful transmission of a packet will cause ML60851E to automatically deassert (set to "0") the corresponding endpoint's transmit packet ready bit and hence, generate an interrupt cause. To transmit subsequent packets from this same end point, the local MCU sets the corresponding transmit packet ready bit after completion of interrupt servicing (such as writing data in the corresponding transmit FIFO, etc.).

Bit D3 is fixed at "0", and even if a "1" is written in this bit, that write operation will be invalid.
The operations of the different bits of PKTRDY are described in detail below.

Please note the R/Reset and R/Set notation used above. R/Reset means: the bit field can be read by the local MCU/and it is Reset (to '0') when a "1" is written to it. The R/Set means: the bit field can be read by the local MCU/and it is Set (to '1') when a 1 is written to it.

EP0 Receive packet ready bit (D0)

This bit can be read by the local MCU. Further, this bit can be set to “0” by writing “1” to the D0 bit.

The conditions of asserting and deasserting this bit are the following.

Bit name	Asserting condition	Action when asserted
EP0 Receive packet ready (D0)	1. When data is received in EP0 and storing of one packet of receive data in EP0RXFIFO is completed. 2. When a setup packet is received during a control Read or a control Write transfer.	EP0 is locked (that is, an NAK is returned automatically when a data packet is received from the host computer). (In the case of the asserting condition 1, the local MCU can read EP0RXFIFO.)

Bit name	Deasserting condition	Action when deasserted
EP0 Receive packet ready (D0)	1. When the local MCU resets (writes a “1” in) this bit. 2. When the local MCU resets the setup ready bit during a control Write transfer.	Reception is possible in EP0.

R/Reset: Reading possible/ Reset when a “1” is written
R/Set: Reading possible/ Set when a “1” is written

EP1 Receive Packet Ready Bit (D1)

This bit can be read by the local MCU. Further, this bit can be set to “0” by writing “1” to the D1 bit.
The conditions of asserting and deasserting this bit are the following. EP1 has a two-layer FIFO, and the packet ready bits are present independently for layer A and layer B. The switching between these two layers is done automatically by the ML60851E. For detailed description of double layered FIFO operation, please refer to page 77 of this manual.

Bit name	Asserting condition	Action when asserted
EP1 Receive packet ready (D1)	When an error-free packet is received in either layer A or layer B.	The local MCU can read the EP1RXFIFO. EP1 is locked when both layer A and layer B have received a packet data.

Bit name	Deasserting condition	Action when deasserted
EP1 Receive packet ready (D1)	When the local MCU resets (writes a “1”) in the bits of both layer A and layer B.	Reception is possible in EP1 when at least one of the bits of layer A and layer B has been reset.

See the explanation of the operation of the two-layer FIFO given in the Section on ‘Functional Description’.

EP2 Receive Packet Ready Bit (D2)

This bit can be read by the local MCU. Further, this bit can be set to “0” by writing “1” to the D2 bit.
The conditions of asserting and deasserting this bit are the following.

Bit name	Asserting condition	Action when asserted
EP2 Receive packet ready (D2)	When an error-free packet is received.	EP2 is locked. In other words, an NAK is returned automatically when a data packet is received from the host computer.

Bit name	Deasserting condition	Action when deasserted
EP2 Receive packet ready (D2)	When the local MCU resets (writes a “1” in) this bit.	Data reception is possible in EP2.

EP0 Transmit Packet Ready Bit (D4)

This bit can be read by the local MCU. Further, this bit can be set to “1” by writing “1” to the D4 bit.
The conditions of asserting and deasserting this bit are the following.

Bit name	Asserting condition	Action when asserted
EP0 Transmit packet ready (D4)	When the local MCU sets this bit.	Data transmission is possible from EP0.

Bit name	Deasserting condition	Action when deasserted
EP0 Transmit packet ready (D4)	1. When an ACK is received from the host computer in response to the data transmission from EP0. 2. When a setup packet is received.	EP0 is locked. In other words, an NAK is returned automatically when an IN token is received from the host computer.

EP1 Transmit Packet Ready Bit (D5)

This bit can be read by the local MCU. Further, this bit can be set to “1” by writing “1” to the D5 bit.
The conditions of asserting and deasserting this bit are the following. EP1 has a two-layer FIFO, and the packet ready bits are present independently for layer A and layer B. The switching between these two layers is performed automatically by the ML60851E. For detailed description of double layered FIFO operation, please refer to page 77 of this manual.

Bit name	Asserting condition	Action when asserted
EP1 Transmit packet ready (D5)	When the local MCU has set the bits of both layer A and layer B.	Data transmission is possible from EP1 when the bit for at least one of layer A and layer B has been asserted.

Bit name	Deasserting condition	Action when deasserted
EP1 Transmit packet ready (D5)	When an ACK is received from the host computer for the data transmission from either layer A or layer B.	EP1 is locked when both layer A and layer B have not prepared the transmit data.

See the explanation of the operation of the two-layer FIFO given in the Section on ‘Functional Description’.

EP2 Transmit Packet Ready Bit (D6)

This bit can be read by the local MCU. Further, this bit can be set to “1” by writing “1” to the D6 bit.
The conditions of asserting and negating this bit are the following.

Bit name	Asserting condition	Action when asserted
EP2 Transmit packet ready (D6)	When the local MCU has set this bit.	Data transmission is possible from EP2.

Bit name	Deasserting condition	Action when deasserted
EP2 Transmit packet ready (D6)	When an ACK is received from the host computer in response to the data transmission from EP2.	EP2 is locked. In other words, an NAK is transmitted automatically when an IN token is received from the host.

EP3 Transmit Packet Ready Bit (D7)

This bit can be read by the local MCU. Further, this bit can be set to “1” by writing “1” to the D7 bit.
The conditions of asserting and deasserting this bit are the following.

Bit name	Asserting condition	Action when asserted
EP3 Transmit packet ready (D7)	When the local MCU has set this bit.	Data transmission is possible from EP3.

Bit name	Deasserting condition	Action when deasserted
EP2 Transmit packet ready (D7)	When an ACK is received from the host computer in response to the data transmission from EP3.	EP3 is locked. In other words, an NAK is transmitted automatically when an IN token is received from the host.

End Point 0 Receive Byte Count Register (EP0RXCNT)

Read address	C9h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	0	Byte count of EP0 (R)						

The ML60851E automatically counts the number of bytes in the packet being received by EP0 and stores it in this register. Although the counting is performed up to the maximum packet size entered in the payload register in the case of a full packet, the count will be less than this value in the case of a short packet. The local MCU refers to this value and reads the data of one packet from the EP0RXFIFO.

The EP0 receive byte count register is cleared under the following conditions:
1. When the local MCU resets the EP0 receive packet ready bit (by writing a "1" in PKTRDY(0)).
2. When a setup packet is received.
3. When the local MCU writes a "0" in the stall bit (EP0STAT(2)).

End Point 1 Receive Byte Count Register (EP1RXCNT)

Read address	CAh
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	0	Byte count of EP1 (R)						

The ML60851E automatically counts the number of bytes in the packet being received by EP1 and stores it in this register. Although the counting is performed up to the maximum packet size entered in the payload register in the case of a full packet, the count will be less than this value in the case of a short packet. The local MCU refers to this value and reads the data of one packet from the EP1 receive FIFO.

This register is invalid when the EP1 transfer direction is set as 'Transmit'.

The EP1 receive byte count register is cleared under the following conditions:
1. When an OUT token is received for EP1.
2. When the EP1 receive packet ready bit is reset (by writing a "1" in PKTRDY(1)).
3. When the local MCU writes a "0" in the stall bit (EP1CON(1)).

End Point 2 Receive Byte Count Register (EP2RXCNT)

Read address	CBh
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	0	Byte Count of EP2 (R)						

The ML60851E automatically counts the number of bytes in the packet being received by EP2 and stores it in this register. Although the counting is performed up to the maximum packet size entered in the payload register in the case of a full packet, the count will be less than this value in the case of a short packet. The local MCU refers to this value and reads the data of one packet from the EP2RXFIFO.

This register is invalid when the EP2 transfer direction is set as 'Transmit'.

The EP2 receive byte count register is cleared under the following conditions:
1. When an OUT token is received for EP2.
2. When the EP2 receive packet ready bit is reset (by writing a "1" in PKTRDY(2)).
3. When the local MCU writes a "0" in the stall bit (EP2CON(1)).

Revision Register (REVISION)

Read address	CDh
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	Revision No. of Chip							
After a bus reset								
Definition								

Transmit FIFO Clear Register (CLRFIFO)

Read address	—
Write address	4Eh

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	Cannot be read (indeterminate)							
After a bus reset	Cannot be read (indeterminate)							
Definition	0	0	0					0

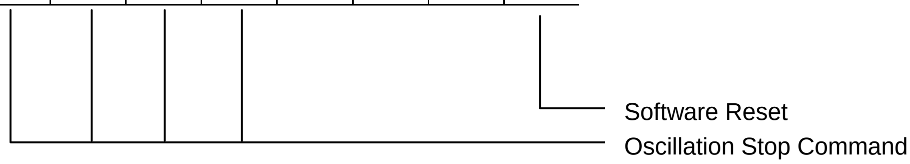
EP1 Transmit FIFO Clear
EP2 Transmit FIFO Clear
EP3 Transmit FIFO Clear

EP1 to EP3 FIFO Clear: When each EP has been set for transmission, by writing a "1" in these bits, the corresponding FIFOs are cleared at the Write pulse and also the corresponding EP Packet Ready bits are reset.

System Control Register (SYSCON)

Read address	—
Write address	4Fh

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	Cannot be read (indeterminate)							
After a bus reset	Cannot be read (indeterminate)							
Definition					0	0	0	



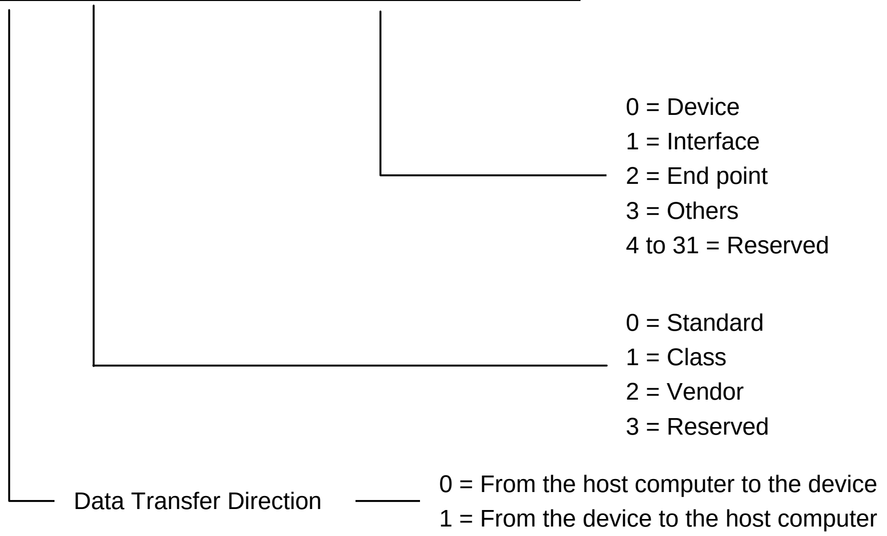
Software Reset: When a “1” is written in this bit, a system reset is executed at the Write pulse. This is functionally equivalent to a hardware reset.

Oscillation Stop command: The Oscillation circuit of the ML60851E stops and goes into the standby state when 1010b is written in D7 to D4 (that is, when A0h is written in this register).
Once the IC goes into the standby state, to start communication with the USB bus thereafter, it is necessary to carry out again disconnecting, connecting, and enumeration.
Even when the Oscillation has stopped, although it is possible to read and write the registers, it is impossible to read or write the FIFO.
The oscillation can be started again by asserting the $\overline{\text{RESET}}$ pin. The oscillation can be restarted even by a software reset.

bmRequest Type Setup Register

Read address	D0h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition		Type		Receiving side				



The format of the device request conforms to Section 9.3 of the USB standards. The eight bytes of setup data sent by the host computer during the setup stage of control transfer are stored automatically in eight registers including this register.

bRequest Setup Register

Read address	D1h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	Request Code							

The request code indicating the contents of the device request is stored automatically in this register during the setup stage of control transfer.

wValue LSB Setup Register

Read address	D2h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	wValue LSB							

A parameter of device request is stored in this register during the setup stage of control transfer.

wValue MSB Setup Register

Read address	D3h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	wValue MSB							

A parameter of device request is stored in this register during the setup stage of control transfer.

wIndex LSB Setup Register

Read address	D4h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	wIndex LSB							

A parameter of device request is stored in this register during the setup stage of control transfer.

wIndex MSB Setup Register

Read address	D5h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	wIndex MSB							

A parameter of device request is stored in this register during the setup stage of control transfer.

wLength LSB Setup Register

Read address	D6h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	wLength LSB							

A parameter of device request is stored in this register during the setup stage of control transfer.

wLength MSB Setup Register

Read address	D7h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	wLength MSB							

A parameter of device request is stored in this register during the setup stage of control transfer.

Polarity Selection Register (POLSEL)

Read address	DAh
Write address	5Ah

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	The previous value is retained							
Definition	0	0	0	0	0			

D0: Polarity of $\overline{INTR}$
0 = Active Low
1 = Active High

D1: Polarity of $\overline{DREQ}$
0 = Active Low
1 = Active High

D2: Polarity of DACK
0 =Active High
1 =Active Low

This register is used for configuring the polarity of the interrupt and DMA signals of ML60851E. Bits D7 to D3 are fixed at “0” and even if “1”s are written in them, they are ignored.

Interrupt Enable Register (INTENBL)

Read address	DBh
Write address	5Bh

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	1
After a bus reset	The previous value is retained							
Definition								

Setup ready Interrupt Enable

EP1 Packet Ready Interrupt Enable

EP2 Packet Ready Interrupt Enable

EP0 Receive Packet Ready Interrupt Enable

EP0 Transmit Packet Ready Interrupt Enable

USB Bus Reset Interrupt Enable

Suspend State Interrupt Enable

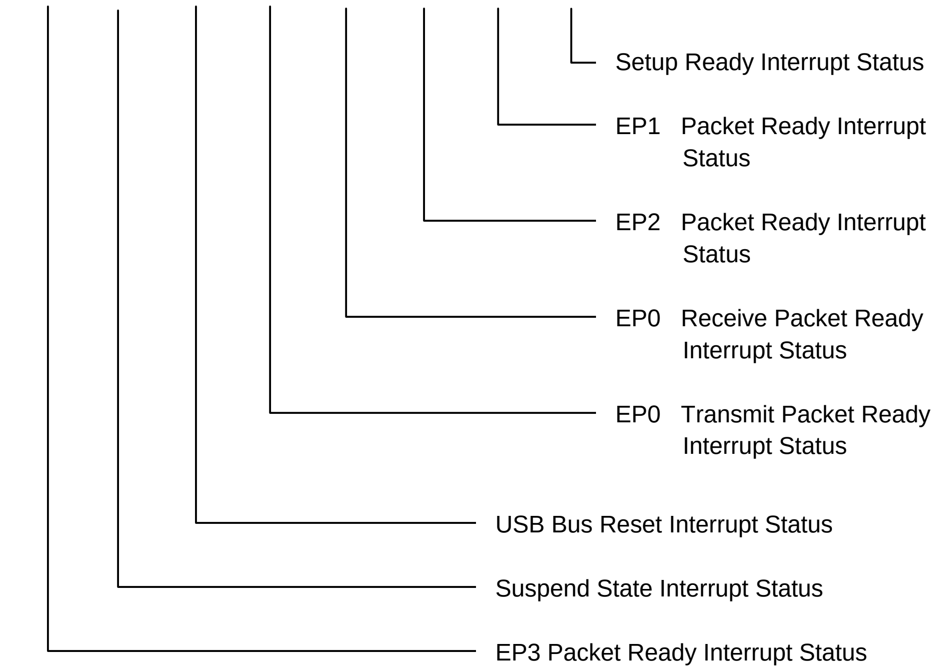
EP3 Packet Ready Interrupt Enable

The interrupts that can be accepted are set in this register. It is possible to change the setting of interrupt enable or disable dynamically depending on the operating conditions. There is a correspondence between this register the interrupt status register described next in terms of the bit numbers and the corresponding interrupt factors.

Interrupt Status Register (INTSTAT)

Read address	DCh
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	See below	0	See below	See below	0	0	0	0
Definition								



Setup Ready Interrupt Status: When bit D0 of the interrupt enable register (INTENBL) is “1”, the content of bit D0 of the EP0 status register (EP0STAT) is copied here.
This bit is “0” when D0 of INTENBL is “0”. In other words, when the eight bytes of setup data are received in the setup stage of control transfer and are correctly stored in the setup registers, this bit is set to “1” and the $\overline{\text{INTR}}$ pin is asserted.

EP1 Packet Ready Interrupt Status: When bit D1 of the interrupt enable register (INTENBL) is “0” (ednpoint 1 interrupt is masked), the content of this bit is “0” and hence no interrupt is generated.

When endpoint 1 is configured as a receive endpoint (EP1CON D7=0), if bit D1 of the interrupt enable register (INTENBL) is “1” (EP1 interrupt enabled), the content of bit D1 of the endpoint packet ready register (PKTRDY) is copied here.
When endpoint 1 is configured as a transmit endpoint (EP1CON D7=1), if bit D1 of the interrupt enable register (INTENBL) is “1” (EP1 interrupt enabled), the inverted (NOT) content of bit D5 of the endpoint pakcet ready register (PKTRDY) is copied here.

In other words, when endpoint 1 packet ready interrupt (D1 of INTENBL) has been enabled the following statements become true:

During data reception, the packet ready interrupt is generated when one packet of receive data is correctly stored in one of the two FIFO layers of EP1. During transmission, the packet ready interrupt is generated when data transmission has been completed from (and writing becomes possible again) one of the two FIFO layers of EP1.

EP2 Packet Ready Interrupt Status: When bit D2 of the interrupt enable register (INTENBL) is “0” (ednpoint 2 interrupt is masked), the content of this bit is “0” and hence no interrupt is generated.

When endpoint 2 is configured as a receive endpoint (EP2CON D7=0), if bit D2 of the interrupt enable register (INTENBL) is “1” (EP2 interrupt enabled), the content of bit D2 of the endpoint packet ready register (PKTRDY) is copied here.
When endpoint 2 is configured as a transmit endpoint (EP2CON D7=1), if bit D2 of the interrupt enable register (INTENBL) is “1” (EP2 interrupt enabled), the inverted (logical NOT) content of bit D6 of the endpoint pakcet ready register (PKTRDY) is copied here.

In other words, when endpoint 2 packet ready interrupt (D2 of INTENBL) has been set to “1” the following statements become true:
During data reception, the packet ready interrupt is generated when one packet of receive data is correctly stored in the FIFO of EP2. During transmission, the packet ready interrupt is generated when data transmission has been completed from (and writing becomes possible again) the FIFO of EP2.

EP0 Receive Packet Ready Interrupt Status:
When bit D3 of the interrupt enable register (INTENBL) is “1”, the content of bit D0 of the end point packet ready register (PKTRDY) is copied here. This bit is “0” when bit D3 of INTENBL is “0”.
In other words, when endpoint 0 receive packet ready interrtup (D3 of INTENBL) has been enabled, if a data packet is received in the data stage of control transfer and is correctly stored in the EP0RXFIFO, this bit is set to “1” and the $\overline{\text{INTR}}$ pin is asserted.

EP0 Transmit Packet Ready Interrupt Status:
When bit D4 of the interrupt enable register (INTENBL) is “1”, the inverted (logical NOT) content of bit D4 of the end point packet ready register (PKTRDY) is copied here. This bit is “0” when bit D4 of INTENBL is “0”.
In other words, when endpoint 0 transmit packet ready interrupt (D4 of INTENBL) has been enabled (set to “1”), if the transmission from EP0TXFIFO is completed, an ACK is received from the host in response to the succussful transmission which will inturn cause the ML60851E to automatically deassert (set to “0”) its EP0 transmit packet ready bit (D4 of PKTRDY) and inturn set this bit and hence generate an interrupt.

The value at the time of a bus reset is based on the value of D4 of INTENBL just prior to bus reset. If D4 of INTENBL was “1” prior to reset, its value will be the same during a bus reset and hence this bit will be “1” and an interrupt will be generated. If D4 of INTENBL was “0” prior to bus reset, interrupt for endpoint 0 was disabled and hence the value of this bit will be “0” after a bus reset.

USB Bus Reset Interrupt Status: When bit D5 of the interrupt enable register (INTENBL) is “1”, this bit becomes “1” during a bus reset. This bit is “0” when bit D5 of INTENBL is “0”. The value at the time of a bus reset is determined based on the value of INTENBL.
Write a “1” in bit D5 of the device status register (DVCSTAT) to reset this bit to “0”.

Suspend State Interrupt Status: When bit D6 of the interrupt enable register (INTENBL) is “1”, the content of bit D3 of the device status register (DVCSTAT) is copied here. This bit is “0” when bit D6 of INTENBL is “0”.

EP3 Packet Ready Interrupt Status: When bit D7 of the interrupt enable register (INTENBL) is “1”, the inverted (logical NOT) content of bit D7 of the end point packet ready register (PKTRDY) is copied here. This bit is “0” when bit D7 of INTENBL is “0”. The value at the time of a bus reset will be determined based on the value of INTENBL at that time.

DMA Control Register (DMACON)

Read address	DDh
Write address	5Dh

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	The previous value is retained							
Definition		0	0					

D0: DMA Enable
0 = DMA Inhibited
1 = DMA Transfer of EP1 is enabled

D1: DMA Address Mode
0 = Single address mode
1 = Dual address mode

D2: Byte Count
0 = The byte count is not inserted.
1 = The byte count data is inserted in the leading byte or the leading word of the transfer data. (Note 1)

D3: DMA Transfer Data Width
0 = Byte wide (8 bits)
1 = Word wide (16 bits) (Note 2)

D4: DMA Transfer Mode
0 = Single transfer mode
1 = Demand transfer mode

D7: Halting DMA Transfer
0 = Normal operation
1 = The DREQ pin is deasserted.

Note 1: In the 16-bit mode, the upper byte of the leading word is 00h.

Note 2: The allocation is made in the little-endian sequence of the upper byte followed by the LSB. In other words, the lower byte corresponds to AD0 to AD7 and the MSB corresponds to D8 to D15. In the 16-bit mode, when the packet size is an odd number of bytes, the upper byte of the last word is 00h.

Note 3: Make sure that all bits other than D7, that is, bits D4 to D0, are set completely during initialization (at the latest, before the token packet for EP1 arrives) and are not modified thereafter.
When wanting to temporarily halt the DMA transfer in the middle, write a “1” in D7. When the transfer is restarted by writing a “0” in D7, it is possible to restart the transfer from the byte (or word) next to the one at the time the transfer was halted.

Note 4: The bits D6 and D5 are fixed at “0”. Even if a “1” is written in them, it will be invalid.

DMA Interval Register (DMAINTVL)

Read address	DEh
Write address	5Eh

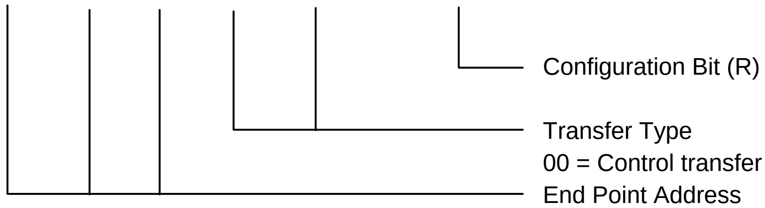
	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	The previous value is retained							
Definition	Interval time							

This register is used for specifying the interval of the single DMA transfer mode, that is, the interval from the completion of the previous byte (or word) DMA transfer until DREQ is asserted again. The time per bit is 84 ns (12 MHz, one period).
Interval time = (DREQ enable time) + 84 x n (ns)
See DMA timings (1), (2), (5), and (6) for details of the DREQ enable time.

End Point 0 Receive Control Register (EP0RXCON)

Read address	E0h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	1
Definition	0	0	0	0	0	0	0	



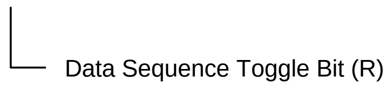
Configuration Bit: The configuration bit of EP0 becomes "1" at the time of an USB bus reset. The packets sent by the host computer to EP0 are received when this bit is "1". This IC does not respond to any transactions with this EP when this bit is "0".

The transfer mode of EP0 is a control transfer and the end point address is fixed at 0h. Therefore, the values of D6 to D2 are fixed and other values written in them are invalid.

End Point 0 Receive Data Toggle Register (EP0RXTGL)

Read address	E1h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	x
After a bus reset	0	0	0	0	0	0	0	x
Definition	0	0	0	0	0	0	0	



End Point 0 Receive Payload Register (EP0RXPLD)

Read address	E2h
Write address	62h

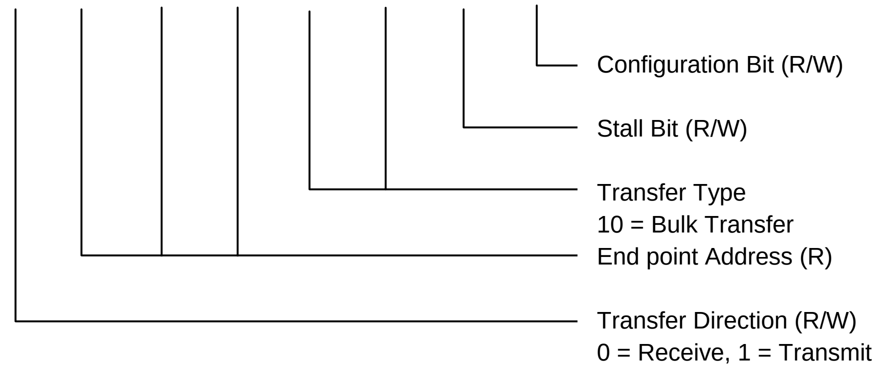
	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	1	0	0	0
After a bus reset	0	0	0	0	1	0	0	0
Definition	0	Maximum packet size						

Maximum packet size: Since the FIFO capacity for EP0 in the ML60851E is 8 bytes, write 08h in the bMaxPacketSize0 byte of the device descriptor. The maximum packet size is fixed at 8 bytes in this register EP0RXPLD.
When a packet longer than 8 bytes is received, the stall bit of the EP0 status register is asserted and the stall status is returned to the host computer.

End Point 1 control Register (EP1CON)

Read address	E4h
Write address	64h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	1	1	0	x	0
After a bus reset	0	0	0	1	1	0	x	0
Definition		0	0	1	1	0		



Configuration Bit: The local MCU should write "1" in this bit during the status stage of control transfer when a "Set Configuration" request is received from the host computer to make EP1 active.
When this bit is "1", the exchange of data between the host computer and EP1 is enabled. When this bit is "0", this IC does not respond to any transactions with this EP.

Stall Bit: When a data packet is received with a number of bytes more than the maximum packet size set in the EP1 payload register, the ML60851E automatically sets this bit to "1". It is also possible for the local MCU to write a "1" in this bit. When this bit is "1", the stall handshake is automatically returned to the host computer in response to the packet transmitted by the host computer to the end point. In addition, the packet ready status is not asserted and even the $\overline{\text{INTR}}$ pin is not asserted.

EP1 transfer type is set as bulk transfer and the end point address is 1h. Therefore, the bits D6 to D2 have fixed values, and other values written in them are ignored.

End Point 1 Data Toggle Register (EP1TGL)

Read address	E5h
Write address	65h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	0	0	0	0	0	0	0	

D0: Data Sequence Toggle Bit (R/Reset)

Data Sequence Toggle Bit: When initializing an EP, write a "1" in this bit to reset the toggle bit of the data packet and specify PID of DATA0 (this bit also becomes "0"). Thereafter, the synchronous operation is made automatically based on the data sequence toggling mechanism.

The values of bits D7 to D1 are fixed at "0" and even if a "1" is written in these bits, it will be invalid.

End Point 1 Payload Register (EP1PLD)

Read address	E6h
Write address	66h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	x	x	x	x	x	x	x
After a bus reset	0	x	x	x	x	x	x	x
Definition	0	Maximum packet size (R/W)						

Maximum Packet Size: The value of wMaxPacketSize of the end point descriptor selected by the Set_Configuration request from the host computer should be written in this register by the local MCU. The packet size of packets other than short packets is specified in units of a byte. The value can be one of 40h (64 bytes), 20h (32 bytes), 10h (16 bytes), and 08h (8 bytes).
During data reception by EP1, if a packet with more number of bytes than that specified here is received, the receive packet ready bit is not asserted, and the stall bit is set during EOP and the stall handshake is returned to the host computer.
On the other hand, when EP1 is being used for transmission, the transmit packet ready bit is set automatically when the writing of data of the number of bytes set in this register (maximum packet size) by the DMA controller is completed.

Bit D7 is fixed at "0", and even if a "1" is written, it will be ignored.

End Point 0 Transmit Control Register (EP0TXCON)

Read address	F0h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	1	0	0	0	0	0	0
After a bus reset	0	1	0	0	0	0	0	1
Definition	0	1	0	0	0	0	0	

D0: Configuration Bit (R)
D3–D2: Transfer Type
00 = Control transfer
D6–D4: FIFO Number

Configuration Bit: The configuration bit of EP0 becomes "1" during an USB bus reset (both D+ and D– being "0" for more than 2.5μs). Packets can be sent from this end point to the host computer when this bit is "1". This IC does not respond to any transactions with this EP when this bit is "0".

The transfer mode of EP0 is a control transfer and the end point address is fixed at 0h. Therefore, the values of D6 to D2 are fixed and other values written in them are invalid.

End Point 0 Transmit Data Toggle Register (EP0TXTGL)

Read address	F1h
Write address	—

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	x
After a bus reset	0	0	0	0	0	0	0	x
Definition	0	0	0	0	0	0	0	

D0: Data Sequence Toggle Bit (R)

The synchronization based on the data sequence toggling mechanism is carried out automatically by the ML60851E.

End Point 0 Transmit Payload Register (EP0TXPLD)

Read address	F2h
Write address	72h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	x	x	x	x	x	x	x
After a bus reset	0	x	x	x	x	x	x	x
Definition	0	Maximum Packet Size (R/W)						

Maximum packet size: This is a register that has no relationship with the operation of the ML60851E, and can be used as a general purpose register. Bit D7 is fixed at “0”.

End Point 0 Status Register (EP0STAT)

Read address	F3h
Write address	73h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	x	0	0
After a bus reset	0	0	0	0	0	x	0	0
Definition	0	0	0				0	

D0: Setup Ready (R/Reset)

D2: Stall Bit (R/W)

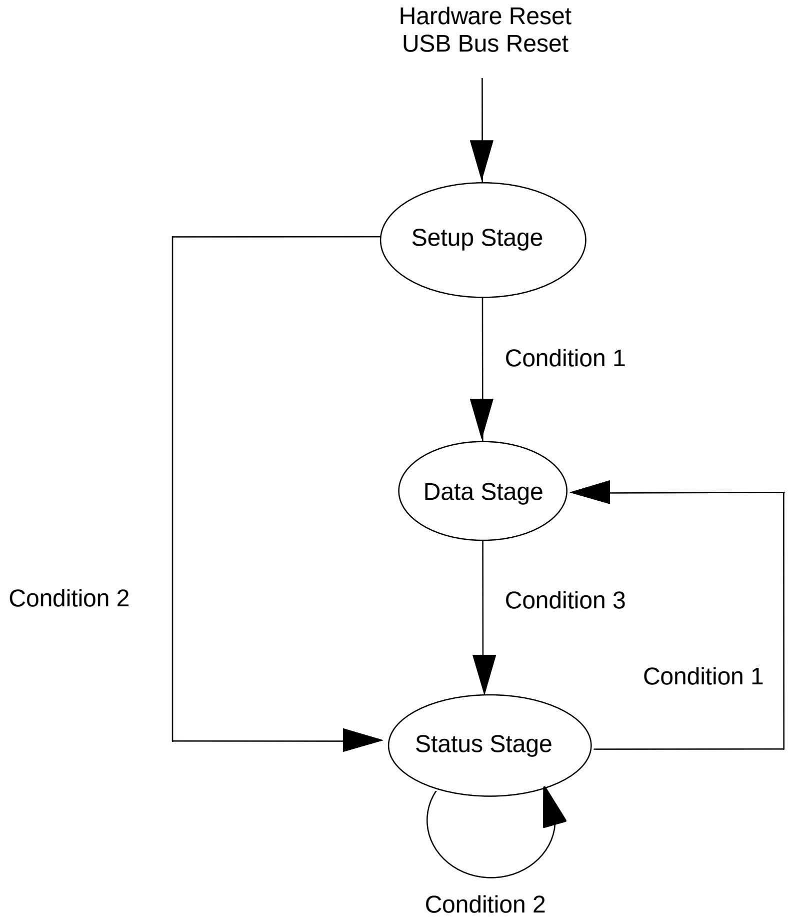
D4, D3: EP0 Stage (R)
00 = Setup stage
01 = Data stage
10 = Status stage

Setup Ready: This bit is set automatically when a proper setup packet arrives in the 8-byte setup register, and the EP0RXFIFO is locked. If D0 of INTENBL has been asserted, the $\overline{\text{INTR}}$ pin is also asserted automatically when this bit is set. The local MCU should write a "1" in this bit after reading out the 8-byte setup data. When this is performed, the setup ready bit is reset and the $\overline{\text{INTR}}$ pin is also deasserted. During a control write, the packet ready bit of EP0 is reset simultaneously, the lock condition is released, and it becomes possible to receive packets by EP0 during the data stage. This bit is reset to "0" by writing a "1" to it. Writing a '0' to this bit will not have any effects on this register.

Stall bit: During EP0 reception (in the data stage of a control write transfer), the ML60851E automatically sets this bit to "1" when a packet with a number of bytes more than the maximum packet size written in EP0RXPLD is received (or when EOP is missing). The EP0 can be set to the STALL condition by writing "1" to this bit. When the following SETUP packet is coming, this bit will be cleared automatically and the EP0 will return from the STALL condition by the procedure based on the USB specification 2.0. (refer to the 8.5.2.4 section of the USB 2.0 specification)

Bits D7 to D5 and D1 are fixed at "0", and other values written in them are invalid.

EP0 Stage: Indicates the stage transition during a control transfer. The transition conditions between the different stages are shown in the following stage transition diagram. These bits are automatically set by ML60851E.

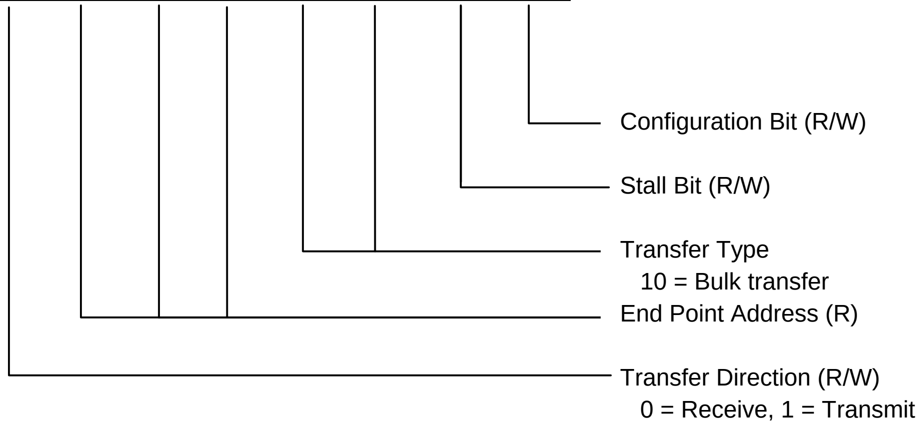


Condition 1: Reception of a setup packet of control READ transfer or control WRITE transfer.
Condition 2: Reception of a setup packet of control transfer without data.
Condition 3: Reception of a token (IN/OUT) of a direction opposite to the data flow in the data stage.

End Point 2 Control Register (EP2CON)

Read address	F4h
Write address	74

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	1	0	1	0	X	0
After a bus reset	0	0	1	0	1	0	X	0
Definition		0	1	0	1	0		



Configuration Bit: The local MCU should write a "1" in this bit during the status stage of control transfer when a "Set Configuration" request is received from the host computer to make EP2 active. When this bit is "1", the exchange of data between the host computer and EP2 is enabled. When this bit is "0", this IC does not respond to any transactions with this EP.

Stall Bit: During EP2 reception, when a data packet is received with a number of bytes more than the maximum packet size set in the pay load register EP2PLD, the ML60851E automatically sets this bit to "1". It is also possible for the local MCU to write a "1" in this bit. When this bit is "1", the stall handshake is automatically returned to the host computer in response to the packet transmitted by the host computer to the end point. In addition, the packet ready status is not asserted and the $\overline{\text{INTR}}$ pin is not asserted.

EP2 transfer type is set as bulk transfer and the end point address is 2h. Therefore, the bits D6 to D2 have fixed values, and other values written in them are ignored.

End Point 2 Data Toggle Register (EP2TGL)

Read address	F5h
Write address	75h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	0	0	0	0	0	0	0	

D0: Data Sequence Toggle Bit (R/Reset)

Data Sequence Toggle Bit: When initializing an EP after receiving a setup packet, write a "1" in this bit to reset the toggle bit of the data packet and specify PID of DATA0 (this bit also becomes "0"). Thereafter, the synchronous operation is made automatically based on the data sequence toggling mechanism.
The values of bits D7 to D1 are fixed at "0" and even if a "1" is written in these bits, it will be invalid.

End Point 2 Payload Register (EP2PLD)

Read address	F6h
Write address	76h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	x	x	x	x	x	x	x
After a bus reset	0	x	x	x	x	x	x	x
Definition	0	Maximum packet size (R/W)						

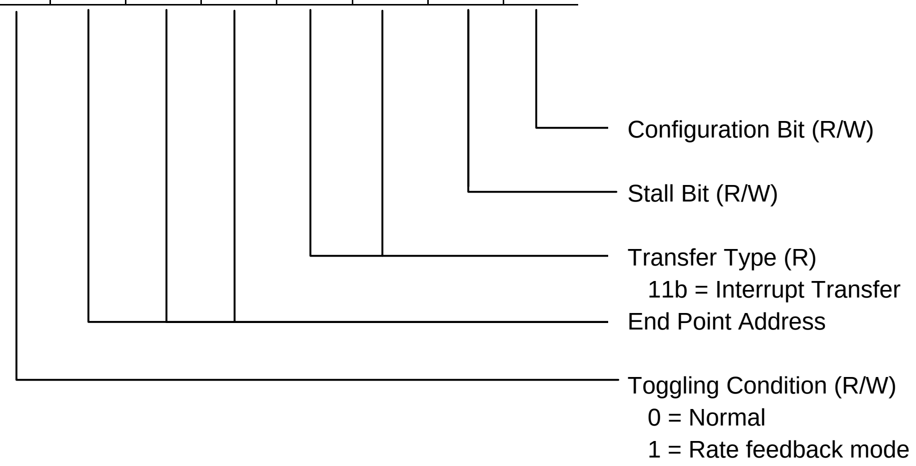
Maximum Packet Size: The value of wMaxPacketSize of the end point descriptor selected by the Set_Configuration request from the host computer should be written in this register by the local MCU. The packet size of packets other than short packets is specified in units of a byte. The value can be one of 40h (64 bytes), 20h (32 bytes), 10h (16 bytes), and 08h (8 bytes). This register is used for EP2 reception. During data reception by EP2, if a packet with more number of bytes than that specified here is received, the receive packet ready bit is not asserted, and the stall bit is set during EOP and the stall handshake is returned to the host computer.

Bit D7 is fixed at "0", and even if a "1" is written, it will be invalid.

End Point 3 Control Register (EP3CON)

Read address	F8h
Write address	78h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	1	1	1	1	x	0
After a bus reset	0	0	1	1	1	1	x	0
Definition		0	1	1	1	1		



Configuration Bit: The local MCU should write a “1” in this bit during the status stage of control transfer when a “Set Configuration” request is received from the host computer to make EP3 active.
When this bit is “1”, the exchange of data between the host computer and EP3 is enabled. When this bit is “0”, this IC does not respond to any transactions with this EP.

Stall Bit: When this bit is “1”, the stall handshake is automatically returned to the host computer in response to the packet transmitted to the host computer from this end point.

The EP3 transfer mode is set as an interrupt transfer and the end point address is fixed at 3h. Therefore, the bits D6 to D2 have fixed values, and other values written in them are invalid.

Toggling Condition Bit: When this bit is “0”, toggling is performed between DATA0 and DATA1 every time an ACK is sent from the host computer to EP3.
If this bit is set to “1”, the rate feedback mode will be set. In this case, the toggling is performed every time the packet ready bit is asserted.

End Point 3 Data Toggle Register (EP3TGL)

Read address	F9h
Write address	79h

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	0	0	0	0	0	0	0
After a bus reset	0	0	0	0	0	0	0	0
Definition	0	0	0	0	0	0	0	

D0: Data Sequence Toggle Bit (R/Reset)

Data Sequence Toggle Bit: When initializing an EP, write a “1” in this bit to reset the toggle bit of the data packet and specify PID of DATA0 (this bit also becomes “0”).

The values of bits D7 to D1 are fixed at “0” and even if a “1” is written in these bits, it will be invalid.

End Point 3 Payload Register (EP3PLD)

Read address	FAh
Write address	7Ah

	D7	D6	D5	D4	D3	D2	D1	D0
After a hardware reset	0	x	x	x	x	x	x	x
After a bus reset	0	x	x	x	x	x	x	x
Definition	0	7-Bit general purpose register						

This register can be used for any purpose. It is possible to retain or refer to the value written in this register without affecting the other operations of the ML60851E. The initial values of bits other than D7 are indeterminate. Bit D7 is fixed at “0” and even if a “1” is written in this bit, it will be invalid.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply 3	V_{CC3}	—	–0.3 to +4.6	V
Power Supply 5	V_{CC5}	—	–0.5 to +6.5	V
Input Voltage	V_I	—	–0.3 to V_{CC5} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply 3	V_{CC3}	—	3.0 to 3.6	V
Power Supply 5	V_{CC5}	—	3.0 to 5.5	V
Operating Temperature	Ta	—	0 to 70	°C
Oscillation Frequency	F_{OSC}	—	48	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{CC5} = V_{CC3} = 3.0 to 3.6 V, Tj = 0 to 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
High-level Input Voltage	V_{IH}	—	2.0	—	V_{CC5}+0.3	V	Note 1
Low-level Input Voltage	V_{IL}	—	–0.3	—	+0.8	V	Note 1
High-level Input Voltage	V_{IH}	—	V_{CC3}×0.8	—	V_{CC3}+0.3	V	XIN
Low-level Input Voltage	V_{IL}	—	–0.3	—	V_{CC3}×0.2	V	XIN
Schmitt Trigger Input Voltage	V_{t+}	—	—	1.6	2.0	V	$\overline{\text{RESET}}$
	V_{t-}	—	0.8	1.2	—	V	
	ΔV_t	$(V_{t+}) - (V_{t-})$	0.1	0.4	—	V	
High-level Output Voltage	V_{OH}	I_{OH} = –100 μA	V_{CC5}–0.2	—	—	V	D15:D8 AD7:AD0 $\overline{\text{INTR}}$, $\overline{\text{DREQ}}$
		I_{OH} = –4 mA	2.4	—	—	V	
Low-level Output Voltage	V_{OL}	I_{OL} = 100 μA	—	—	0.2	V	
		I_{OL} = 4 mA	—	—	0.4	V	
High-level Input Current	I_{IH}	V_{IH} = V_{CC5}	—	0.01	1	μA	Note 2
Low-level Input Current	I_{IL}	V_{IL} = 0 V	–1	–0.01	—	μA	Note 2
3-state Output Leakage Current	I_{OZH}	V_{OH} = V_{CC5}	—	0.01	1	μA	D15:D8 AD7:AD0
	I_{OZL}	V_{OL} = 0 V	–1	–0.01	—	μA	
Power Supply Current (Operating)	I_{CC}	Note 3	—		55	mA	V_{CC3}, V_{CC5}
Power Supply Current (Standby)	I_{CCS}	Note 4	—		100	μA	V_{CC3}, V_{CC5}

Notes:
1. Applied to D15:D8, AD7:AD0, A7:A0, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DACK, ALE, and ADSEL.
2. Applied to XIN, A7:A0, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DACK, ALE, and ADSEL.
3. Total currents when V_{CC3} and V_{CC5} are connected.
4. Total currents when V_{CC3} and V_{CC5} are connected.
   The XIN pin is fixed at a high level or a low level in the suspend state.
   All the output pins are open.

DC Characteristics (2)

(V_{CC5} = 4.5 to 5.5 V, V_{CC3} = 3.0 to 3.6 V, Tj = 0 to 85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
High-level Input Voltage	V_{IH}	—	2.2	—	V_{CC5}+0.5	V	Note 1
Low-level Input Voltage	V_{IL}	—	–0.5	—	+0.8	V	
Schmitt Trigger Input Voltage	V_{t+}	—	—	1.7	2.2	V	$\overline{RESET}$
	V_{t-}	—	0.8	1.4	—	V	
	ΔV_t	$(V_{t+}) - (V_{t-})$	0.2	0.3	—	V	
High-level Output Voltage	V_{OH}	I_{OH} = –100 μA	V_{CC5}–0.2	—	—	V	D15:D8 AD7:AD0 $\overline{INTR}$, $\overline{DREQ}$
		I_{OH} = –8 mA	3.7	—	—	V	
Low-level Output Voltage	V_{OL}	I_{OL} = 100 μA	—	—	0.2	V	
		I_{OL} = 8 mA	—	—	0.4	V	
High-level Input Current	I_{IH}	$V_{IH} = V_{CC5}$	—	0.01	10	μA	Note 2
Low-level Input Current	I_{IL}	V_{IL} = 0 V	–10	–0.01	—	μA	
3-state Output Leakage Current	I_{OZH}	$V_{OH} = V_{CC5}$	—	0.01	10	μA	D15:D8 AD7:AD0
	I_{OZL}	V_{OL} = 0 V	–10	–0.01	—	μA	
Power Supply Current (Operating)	I_{CC3}	—	—	—	50	mA	V_{CC3}
	I_{CC5}	—	—	—	5	mA	V_{CC5}
Power Supply Current (Standby)	I_{CCS3}	Note 3	—	—	50	μA	V_{CC3}
	I_{CCS5}	Note 3	—	—	50	μA	V_{CC5}

Notes:
1. Applied to D15:D8, AD7:AD0, A7:A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DACK, ALE, and ADSEL. The DC characteristics (1) applies to XIN.
2. Applied to A7:A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DACK, ALE, and ADSEL. The DC characteristics (1) applies to XIN.
3. The XIN pin is fixed at a high level or a low level in the suspend state. All the output pins are open.

DC Characteristics (3) USB Port

(V_{CC3} = 3.0 to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Differential Input Sensitivity	V_{DI}	(D+) – (D–)	0.2		—	V	D+, D–
Differential Common Mode Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V	
Single Ended Receiver Threshold	V_{SE}		0.8		2.0	V	
High-level Output Voltage	V_{OH}	RL of 15 kΩ to GND	2.8		3.6	V	
Low-level Output Voltage	V_{OL}	RL of 1.5 kΩ to 3.6 V	—		0.3	V	
Output Leakage Current	I_{LO}	0 V < V_{IN} < 3.3 V	–10		+10	μA	

AC Characteristics USB Port

(V_{CC3} = 3.0 to 3.6 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition (Notes 1. and 2.)	Min.	Typ.	Max.	Unit	Applicable pin
Rise Time	t_R	CL = 50 pF	4		20	ns	D+, D–
Fall Time	t_F	CL = 50 pF	4		20	ns	
Rise/Fall Time Matching	t_{RFM}	(t_R/t_F)	90		111.11	%	
Output Signal Crossover Voltage	V_{CRS}		1.3		2	V	
Driver Output Resistance	Z_{DRV}	Steady State Driver (Note 3)	28		44	Ω	
Data Rate	t_{DRATE}	Ave. Bit Rate (12 Mbps ±0.25%)	11.97		12.03	Mbps	

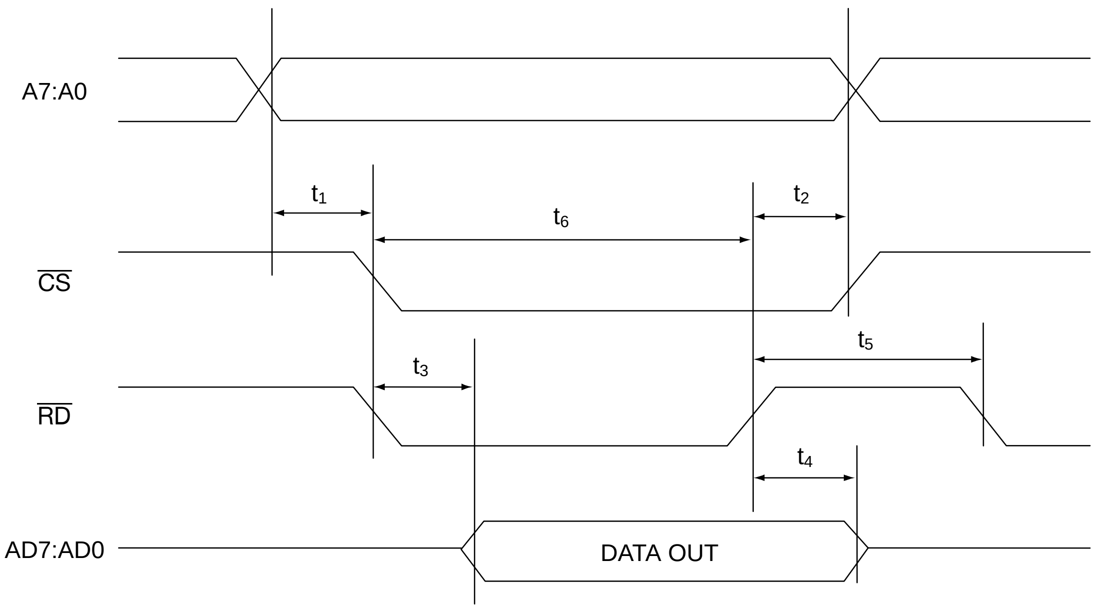
Notes: 1. 1.5 kΩ pull-up to 3.3 V on the D+ data line.
2. t_R and t_F are measured from 10% to 90 % of the data signal.
3. Including an external resistance of 22 Ω ± 5% on the D+ and D– data lines.

TIMING DIAGRAM

READ Timing (1)
(Address Separate, ADSEL = 0)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Address Setup Time ($\overline{\text{RD}}$)	t_1 ($\overline{\text{RD}}$)		21	—	ns	5
Address Setup Time ($\overline{\text{CS}}$)	t_1 ($\overline{\text{CS}}$)		10	—	ns	5
Address ($\overline{\text{CS}}$) Hold Time	t_2		0	—	ns	2
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	1
Read Data Hold Time	t_4	Load 20 pF	0	25	ns	
Recovery Time	t_5	FIFO READ	63	—	ns	3
FIFO Access Time	t_6	FIFO READ	42	—	ns	4

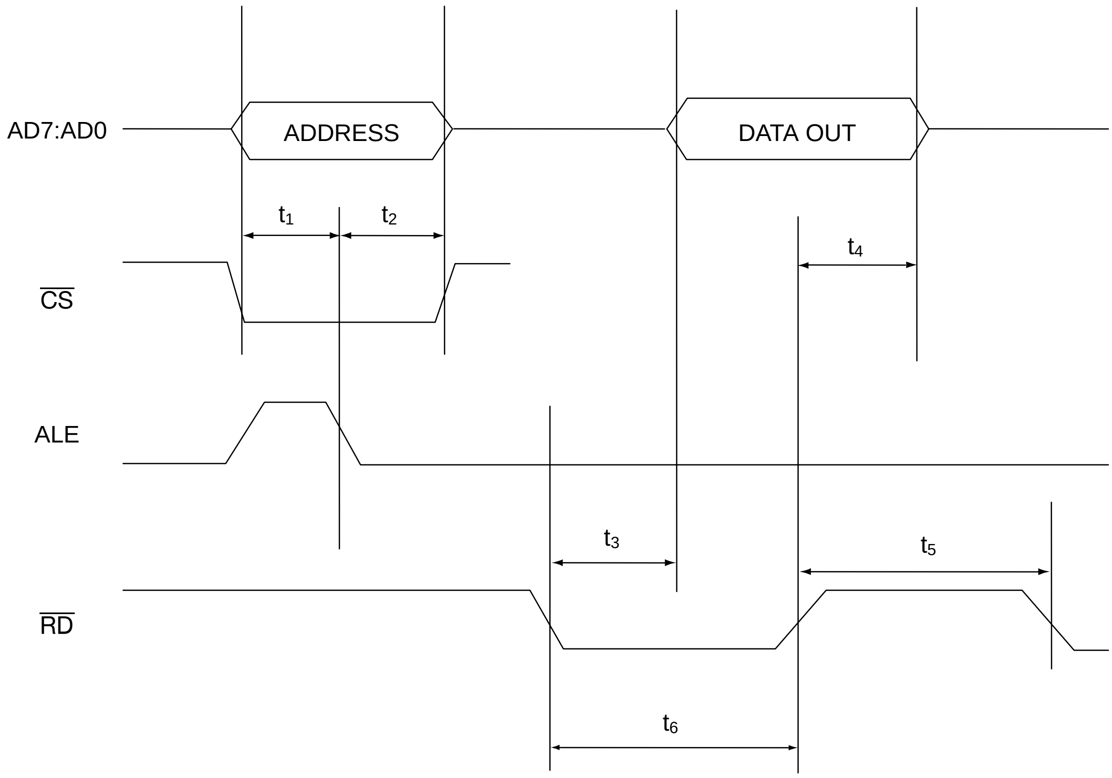
Notes:
1. t_3 is defined depending upon $\overline{\text{CS}}$ or $\overline{\text{RD}}$ which becomes active last.
2. t_2 is defined depending upon $\overline{\text{CS}}$ or $\overline{\text{RD}}$ which becomes active first.
3. 3-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
4. 2-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
5. t_1 is required for reading FIFO. t_1 is defined when either t_1 ($\overline{\text{CS}}$) or t_1 ($\overline{\text{RD}}$) is satisfied.



READ Timing (2)
(Address/Data Multiplex, ADSEL = 1)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Address ($\overline{CS}$) Setup Time	t_1		10	—	ns	
Address ($\overline{CS}$) Hold Time	t_2		0	—	ns	
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	
Read Data Hold Time	t_4	Load 20 pF	0	25	ns	
Recovery Time	t_5	FIFO READ	63	—	ns	1
FIFO Access Time	t_6	FIFO READ	42	—	ns	2

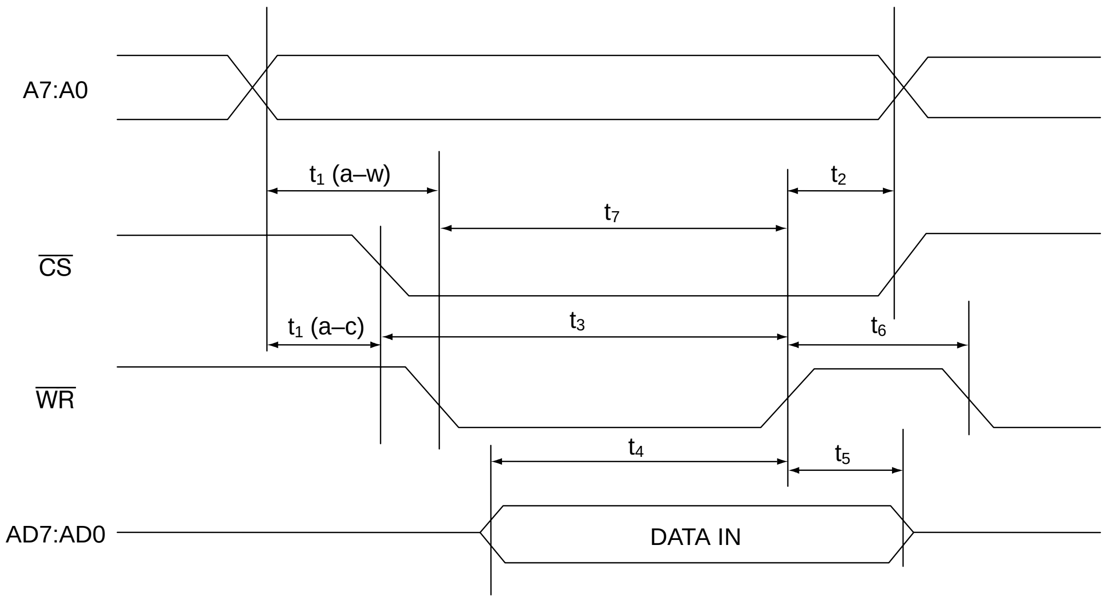
Notes: 1. 3-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
2. 2-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.



WRITE Timing (1)
(Address Separate, ADSEL = 0)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Address Setup Time	t_1 (a–w)		21	—	ns	1
Address Setup Time	t_1 (a–c)		10	—	ns	1
Address ($\overline{CS}$) Hold Time	t_2		0	—	ns	
$\overline{CS}$ Setup Time	t_3		10	—	ns	
Write Data Setup Time	t_4		30	—	ns	
Write Data Hold Time	t_5		2	—	ns	
Recovery Time	t_6	FIFO WRITE	63	—	ns	2
FIFO Access Time	t_7	FIFO WRITE	42	—	ns	3

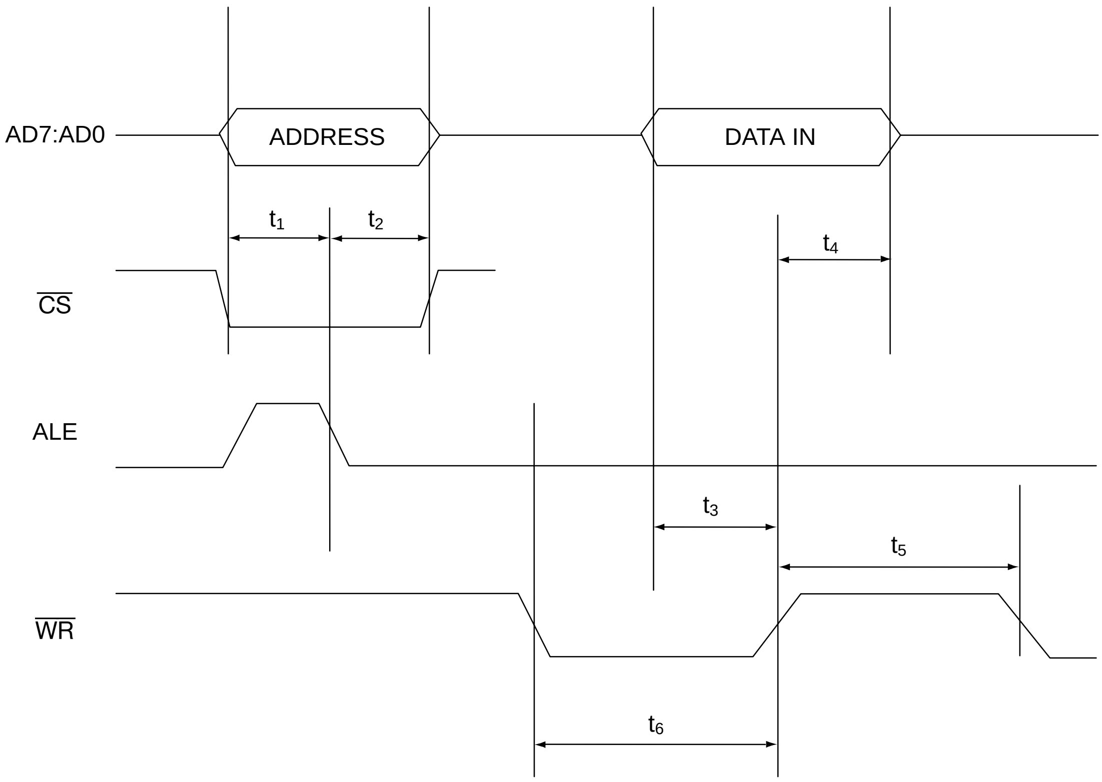
Notes:
1. Either t_1 (a–w) or t_1 (a–c) should be satisfied.
2. t_1 is defined depending upon $\overline{CS}$ or $\overline{WR}$ which becomes active first.
3. 3-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
4. 2-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
5. Applied to all registers including CLRFIFO (address: 4Eh).



WRITE Timing (2)
(Address/Data Multiplex, ADSEL = 1)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Address ($\overline{CS}$) Setup Time	t_1		10	—	ns	
Address ($\overline{CS}$) Hold Time	t_2		0	—	ns	
Write Data Setup Time	t_3		30	—	ns	
Write Data Hold Time	t_4		2	—	ns	
Recovery Time	t_5	FIFO WRITE	63	—	ns	1
FIFO Access Time	t_6	FIFO WRITE	42	—	ns	2

Notes: 1. 3-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
2. 2-clock time of oscillation clock (clock period: 21 ns). It is required for increment of FIFO.
3. Applied to all registers including CLRFIFO (address: 4Eh).

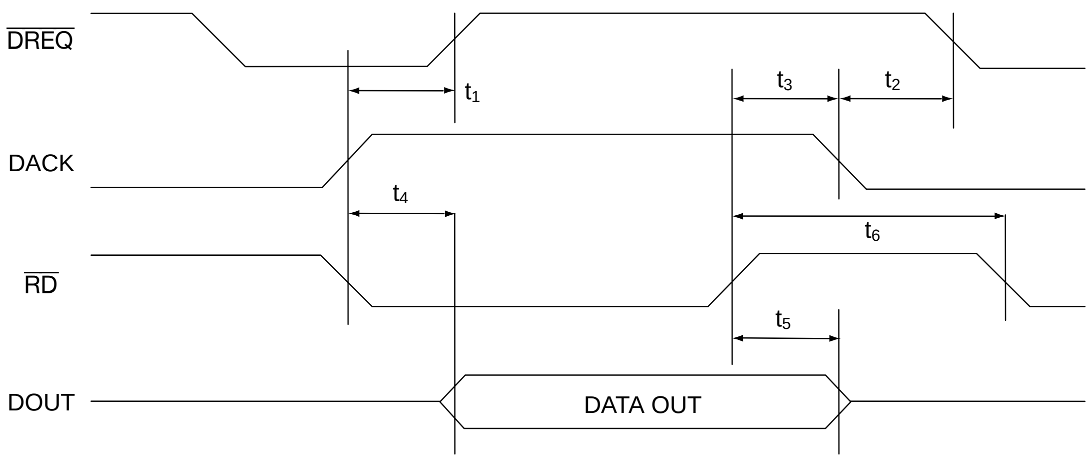


DMA Transfer Timing (1)

ML60851E to Memory (Single Transfer, Single Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{DREQ}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{DREQ}$ Enable Time	t_2		—	63	ns	4
DACK Hold Time	t_3		0	—	ns	
Read Data Delay Time	t_4	Load 20 pF	—	25	ns	1
Data Hold Time	t_5	Load 20 pF	0	25	ns	
Recovery Time	t_6	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Single Address mode, $\overline{CS}$ and A7:A0 are ignored.
t_1 and t_4 are defined depending on DACK or $\overline{RD}$ which becomes active last.
2. 3-clock time of oscillation clock (clock period: 21 ns)
3. 5-clock time of oscillation clock (clock period: 21 ns)
4. It is possible to increase t_2 by setting the DMA interval register (DMAINTVL).

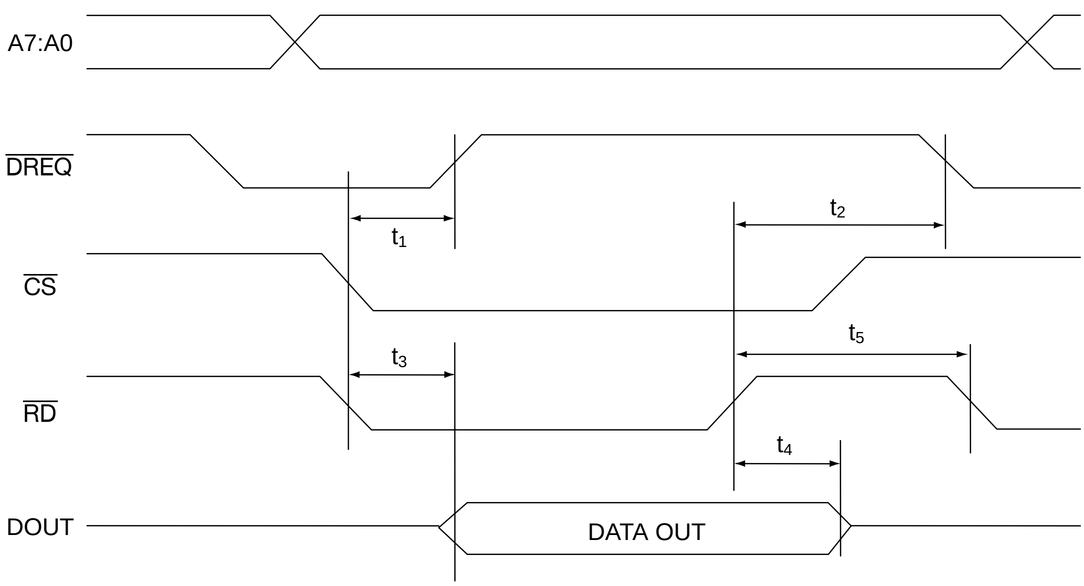


DMA Transfer Timing (2)

ML60851E to Memory (Single Transfer, Dual Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{DREQ}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{DREQ}$ Enable Time	t_2		—	63	ns	4
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	1
Data Hold Time	t_4	Load 20 pF	0	25	ns	
Recovery Time	t_5	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Dual Address mode, the DACK is ignored.
t_1 and t_3 are defined depending on $\overline{CS}$ or $\overline{RD}$ which becomes active last.
A7:A0 specifies the FIFO address.
Refer to READ Timing (1) for Address Setup Time and Address Hold Time.
2. 3-clock time of oscillation clock (clock period: 21 ns)
3. 5-clock time of oscillation clock (clock period: 21 ns)
4. It is possible to increase t_2 by setting the DMA interval register (DMAINTVL).

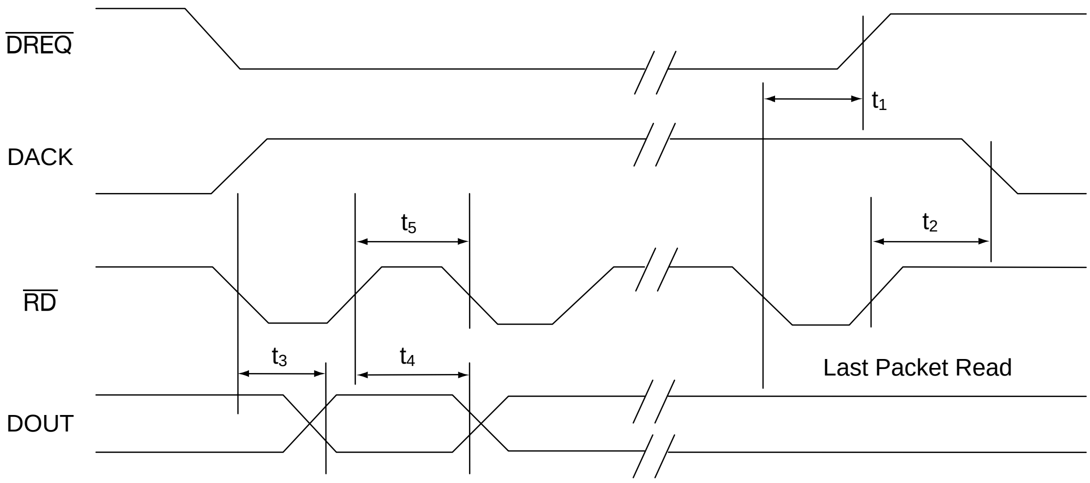


DMA Transfer Timing (3)

ML60851E to Memory (Demand Transfer, Single Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
DACK Hold Time	t_2		0	—	ns	
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	1
Data Hold Time	t_4	Load 20 pF	0	25	ns	
Recovery Time	t_5	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes:
1. When in Single Address mode, t_3 is defined depending on DACK or $\overline{\text{RD}}$ which becomes active last.
   A7:A0 and $\overline{\text{CS}}$ are ignored.
2. 3-clock time of oscillation clock (clock period: 21 ns)
3. 5-clock time of oscillation clock (clock period: 21 ns)

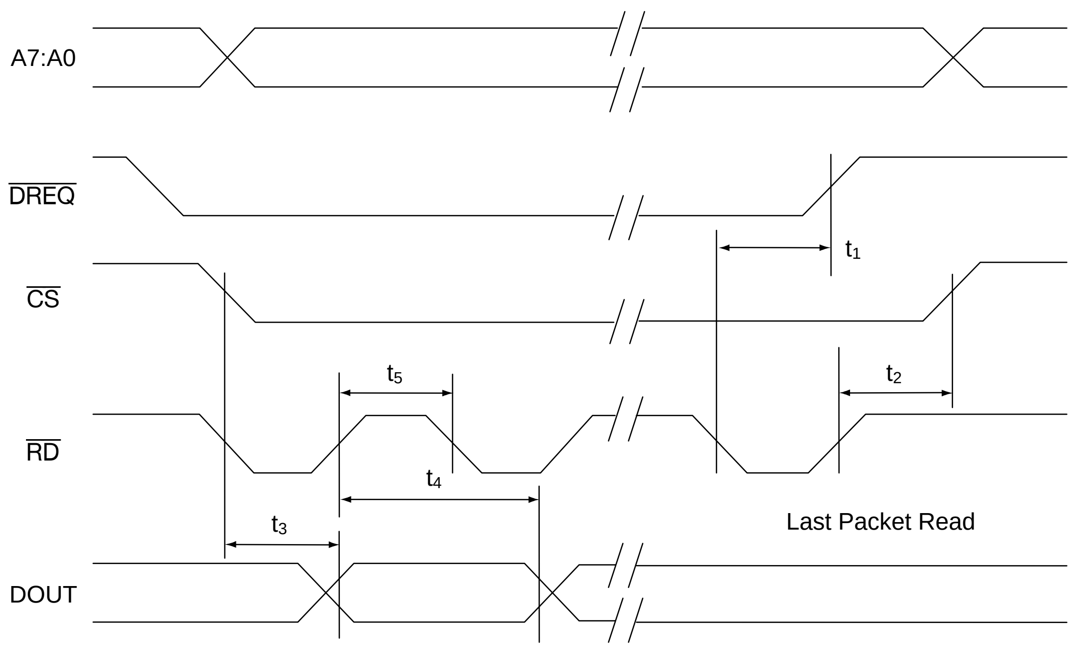


DMA Transfer Timing (4)

ML60851E to Memory (Demand Transfer, Dual Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{\text{CS}}$ Hold Time	t_2		0	—	ns	
Read Data Delay Time	t_3	Load 20 pF	—	25	ns	1
Data Hold Time	t_4	Load 20 pF	0	25	ns	
Recovery Time	t_5	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Dual Address mode, the DACK is ignored.
t_3 is defined depending on $\overline{\text{CS}}$ or $\overline{\text{RD}}$ which becomes active last.
A7:A0 specifies the FIFO address.
Refer to READ Timing (1) for Address Setup Time and Address Hold Time.
2. 3-clock time of oscillation clock (clock period: 21 ns)
3. 5-clock time of oscillation clock (clock period: 21 ns)

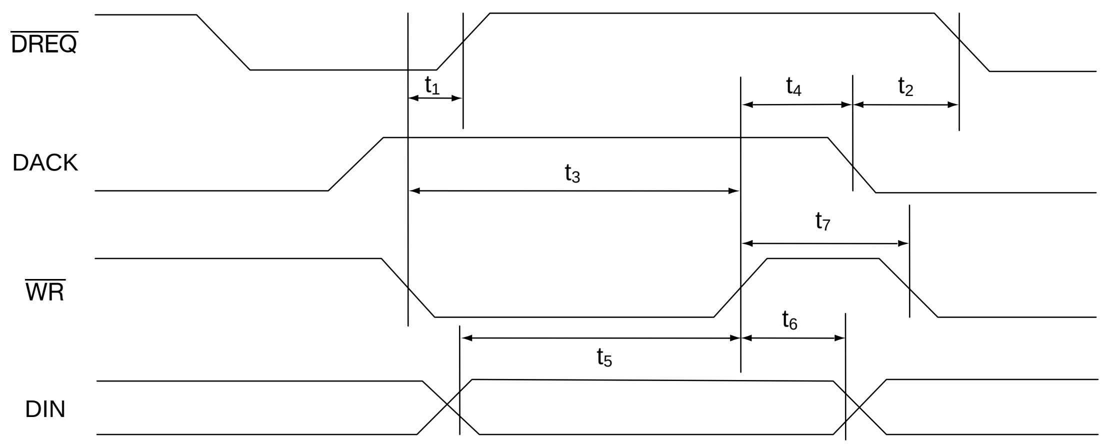


DMA Transfer Timing (5)

Memory to ML60851E (Single Transfer, Single Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{\text{DREQ}}$ Enable Time	t_2		—	63	ns	4
FIFO Access Time	t_3	FIFO WRITE	42	—	ns	1
DACK Hold Time	t_4		0	—	ns	
Write Data Setup Time	t_5		30	—	ns	
Write Data Hold Time	t_6		2	—	ns	
Recovery Time	t_7	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Single Address mode, $\overline{\text{CS}}$ and A7:A0 are ignored.
2. 3-clock time of oscillation clock (clock period: 21 ns)
3. 5-clock time of oscillation clock (clock period: 21 ns)
4. It is possible to increase t_2 by setting the DMA interval register (DMAINTVL).

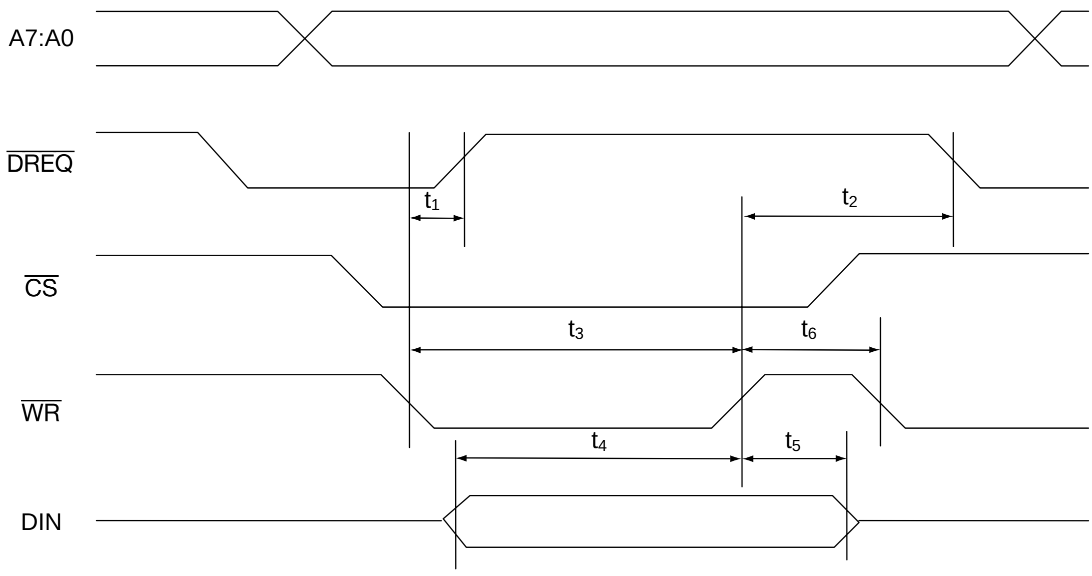


DMA Transfer Timing (6)

Memory to ML60851E (Single Transfer, Dual Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{DREQ}$ Disable Time	t_1	Load 20 pF	—	20	ns	
$\overline{DREQ}$ Enable Time	t_2		—	63	ns	4
FIFO Access Time	t_3	FIFO WRITE	42	—	ns	1
Write Data Setup Time	t_4		30	—	ns	
Write Data Hold Time	t_5		2	—	ns	
Recovery Time	t_6	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Dual Address mode, the DACK is ignored.
t_1 and t_3 are defined depending on $\overline{CS}$ or $\overline{WR}$ which becomes active last.
Refer to WRITE Timing (1) for Address Setup Time and Address Hold Time.
2. 3-clock time of oscillation clock (clock period: 21 ns)
3. 5-clock time of oscillation clock (clock period: 21 ns)
4. It is possible to increase t_2 by setting the DMA interval register (DMAINTVL).

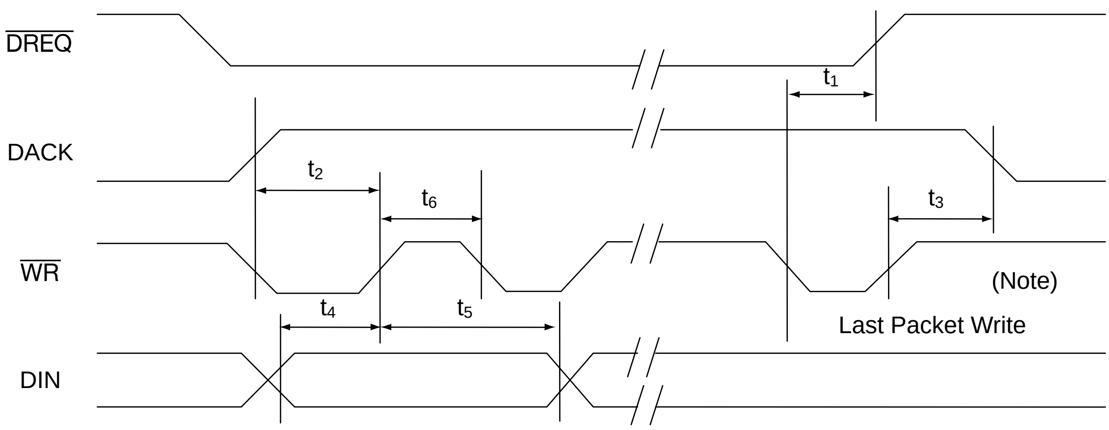


DMA Transfer Timing (7)

Memory to ML60851E (Demand Transfer, Single Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{DREQ}$ Disable Time	t_1	Load 20 pF	—	20	ns	
FIFO Access Time	t_2	FIFO WRITE	42	—	ns	1
DACK Hold Time	t_3		0	—	ns	
Write Data Setup Time	t_4		30	—	ns	
Write Data Hold Time	t_5		2	—	ns	
Recovery Time	t_6	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Single Address mode, A7:A0 and $\overline{CS}$ are ignored.
t_2 is defined depending on DACK or $\overline{WR}$ which becomes active last.
2. 3-clock time of oscillation clock (clock period: 21 ns)
3. 5-clock time of oscillation clock (clock period: 21 ns)



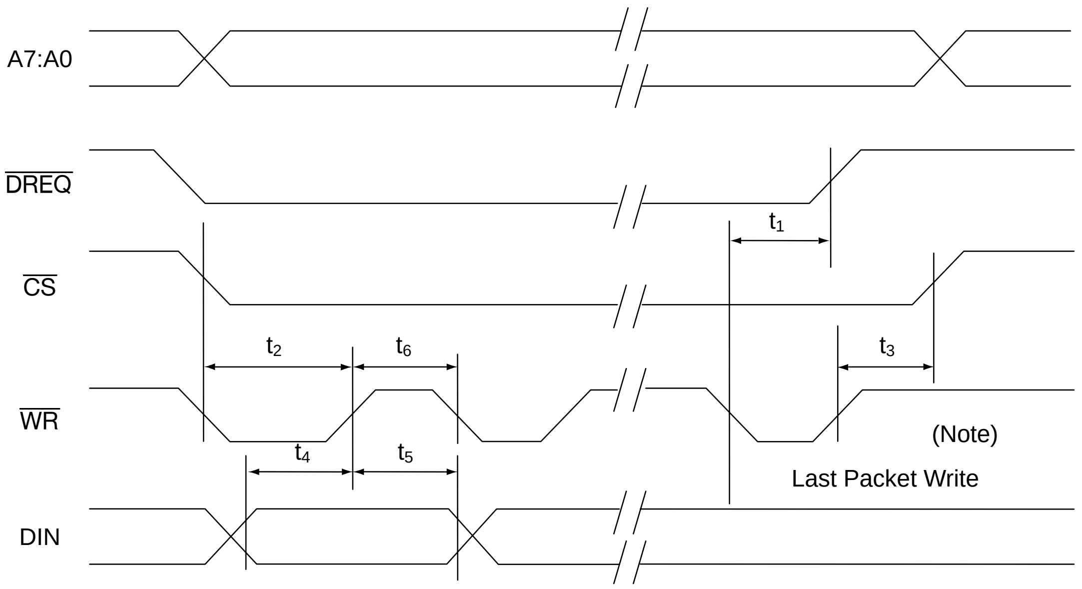
(Note) The last Write to reach the byte size (maximum packet size) specified by the EP1 Payload Register.
To terminate DMA transfer before reaching the maximum packet size, set EP1 Packet Ready by writing "1" to the EP1 Endpoint Packet Ready bit.

DMA Transfer Timing (8)

Memory to ML60851E (Demand Transfer, Dual Address Mode)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
$\overline{\text{DREQ}}$ Disable Time	t_1	Load 20 pF	—	20	ns	
FIFO Access Time	t_2	FIFO WRITE	42	—	ns	1
$\overline{\text{CS}}$ Hold Time	t_3		0	—	ns	
Write Data Setup Time	t_4		30	—	ns	
Write Data Hold Time	t_5		2	—	ns	
Recovery Time	t_6	8-bit DMA	63	—	ns	2
		16-bit DMA	105	—	ns	3

Notes: 1. When in Dual Address mode, the DACK is ignored.
A7:A0 specifies the FIFO address.
Refer to WRITE Timing (1) for Address Setup Time and Address Hold Time.
t_2 is defined depending on $\overline{\text{CS}}$ or $\overline{\text{WR}}$ which becomes active last.
2. 3-clock time of oscillation clock (clock period: 21 ns)
3. 5-clock time of oscillation clock (clock period: 21 ns)



(Note) Refer to the previous page.

FUNCTIONAL DESCRIPTIONS

Pin Functional Description

USB Interface

<table>
<tr><th>Signal</th><th>Type</th><th>Assertion</th><th>Description</th></tr>
<tr><td>D+</td><td>I/O</td><td>—</td><td>USB data (Plus). This signal and the D– signal are the transmitted or received data from/to USB Bus. The table below shows values and results for these signals.
<table>
<tr><th>D+</th><th>D–</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>Single end 0</td></tr>
<tr><td>0</td><td>1</td><td>Differential “0”</td></tr>
<tr><td>1</td><td>0</td><td>Differential “1”</td></tr>
<tr><td>1</td><td>1</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>D–</td><td>I/O</td><td>—</td><td>USB Data (Minus). This signal and the D+ signal are the transmitted or received data from/to USB Bus. The table above shows values and results for these signals.</td></tr>
</table>

Crystal Oscillator Interface

<table>
<tr><th>Signal</th><th>Type</th><th>Assertion</th><th>Description</th></tr>
<tr><td>XIN</td><td>I</td><td>—</td><td rowspan="2">For internal oscillation, connect a crystal to XIN and XOUT.
For external oscillation, supply an external 48 MHz clock signal to XIN.
Set XOUT to be open.</td></tr>
<tr><td>XOUT</td><td>O</td><td>—</td></tr>
</table>

Application Interface

Signal	Type	Assertion	Description
D15:D8	I/O	—	Upper byte (MSB) of data bus. This data bus is used by applications to access register files and FIFO data.
AD7:AD0	I/O	—	Lower byte (LSB) of data bus when ADSEL is LOW. Address and lower byte of data bus are multiplexed when ADSEL is HIGH.
A7:A0	I	—	Address when ADSEL is LOW. This address signal is used by application to access register files and FIFO data. This signal is ignored (all lows or all highs) when ADSEL is HIGH.
$\overline{\text{CS}}$	I	LOW	Chip Select. When this signal is asserted LOW, the ML60851E is selected and ready to read or write data.
$\overline{\text{RD}}$	I	LOW	Read Strobe. When this signal is asserted LOW, the Read instruction is executed.
$\overline{\text{WR}}$	I	LOW	Write Strobe. When this signal is asserted LOW, the Write instruction is executed.
$\overline{\text{INTR}}$	O	LOW (Note 1)	Interrupt Request. When this signal is asserted, the ML60851E makes an interrupt request to the application.
$\overline{\text{DREQ}}$	O	LOW (Note 1)	DMA Request. This signal requests the Endpoint FIFO to make a DMA transfer.
DACK	I	HIGH (Note 1)	DMA Acknowledge Signal. This signal, when asserted, enables accessing FIFOs, without address bus setting.
ALE	I	—	When ADSEL is HIGH, the address and $\overline{\text{CS}}$ on AD7:AD0 is latched at the trailing edge of this signal. This signal is ignored when ADSEL is LOW.
ADSEL	I	—	When ADSEL is LOW, the address is input on A7:A0 and data is input on D15:D8 and AD7:AD0. When ADSEL is HIGH, the lower bytes (LSB) of address and data are multiplexed on AD7:AD0.
$\overline{\text{RESET}}$	I	LOW	System Reset. When this signal is asserted LOW, the ML60851E is reset. When the ML60851E is powered on, this signal must be asserted for 1 μs or more.

Note: 1. Initial value immediately after resetting. Its assertion can be changed by programming.

Functional Description

ML60851E USB device controller contains Protocol Engine, DPLL, Timer, Status/Control, FIFO Control, Application Interface, and Remote Wakeup blocks.

• Protocol Engine
The Protocol Engine handles the USB communication protocol. It performs control of packet transmission/reception, generation/detection of synchronous patterns, CRC generation/checking, NRZI data modulation, bit stuffing, and packet ID (PID) generation/checking.

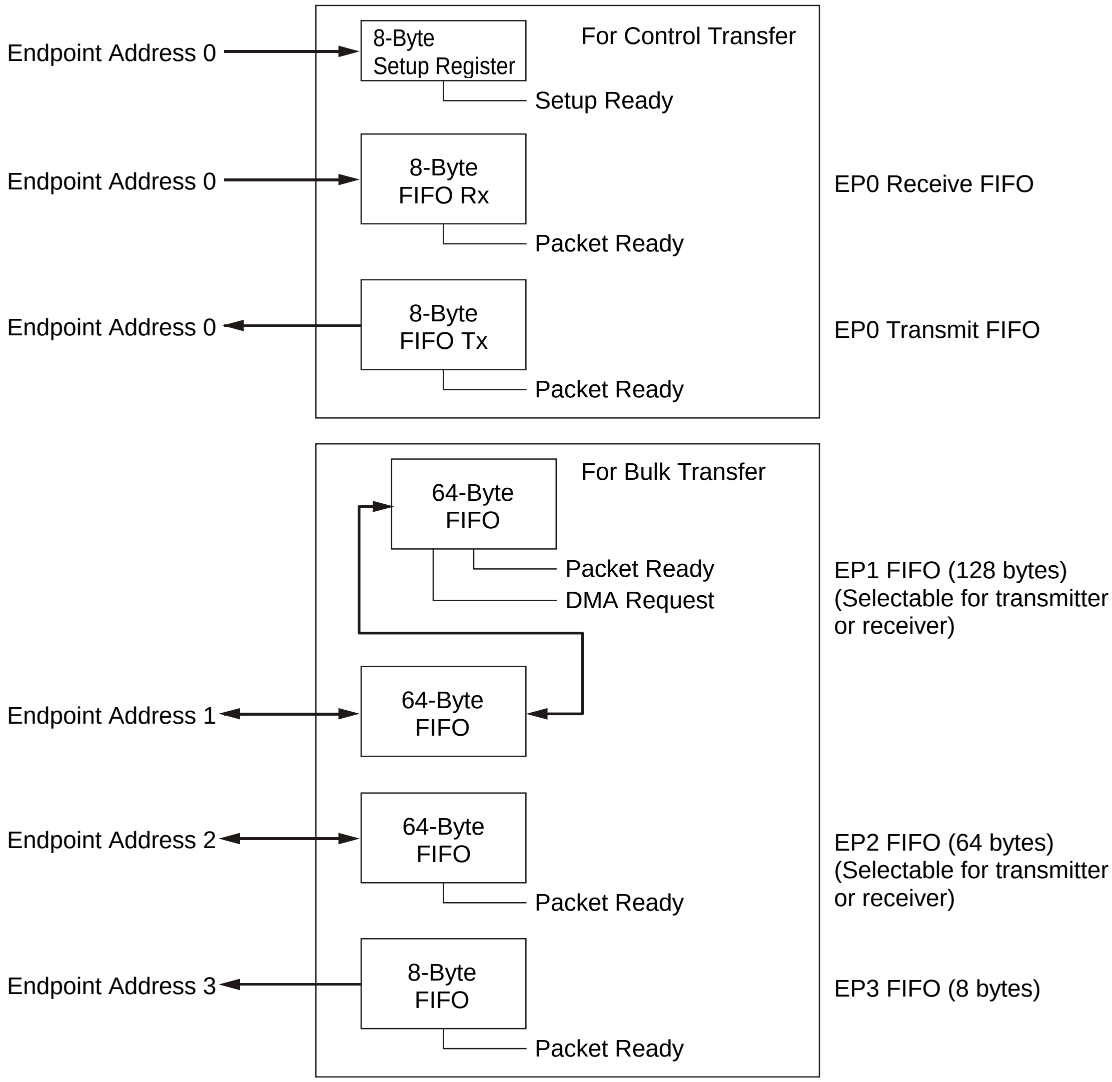
• DPLL (Digital Phase Locked Loop)
The DPLL extracts clock and data from the USB differential received data (D+ and D–).

• Timer
The Timer block monitors idle time on the USB bus.

• Status/Control
The Status Control block moniors the transaction status and transmits control events to the application through an interrupt request.

• FIFO Control
The FIFO Control block controls all FIFO operations for transmitting and receiving USB packets.
The FIFO configuration is described below.

Endpoint FIFO/8-Byte Setup Register Configuration



FIFO type	Endpoint address	Program size	Function
Reception	0	8 Bytes	Transfer control
Transmission	0	8 Bytes	Transfer control
Reception/Transmission	1	64 Bytes (2 levels)	Bulk-In and bulk-Out
Reception/Transmission	2	64 Bytes	Bulk-Out and bulk-In
Transmission	3	8 Bytes	Interrupt

Every FIFO has a flag that indicates a full or empty FIFO and the capability of re-transmitting and re-receiving data. Endpoint addresses 1 and 2 can be used for either of reception and transmission by writing the register. The FIFO at endpoint address 1 can be used for DMA transfer.

- Remote Wakeup
  This functional block supports the remote wakeup function.

- USB Transfers
  ML60851E supports three types of transfers: Control, Bulk and Interrupt Transfers as defined by USB Specifications.
  – Control Transfer is required for transfer of configuration, commands, and status information between the host and devices.
  – Bulk Transfer enables transfer of large amounts of data when the bus bandwidth is adequate.
  – Interrupt Transfers are used when moderate amounts of data have to transfer within a specific amount of time.

- USB Transceiver
  ML60851E contains Oki's USB transceiver which converts internal unidirectional signals into USB-compatible signals.
  This enables the designer's application module to interface to the physical layer of USB.

• Interrupts

The ML60851E requests interrupts to the local MCU, etc., by asserting the -INTR pin. The interrupt causes are the following:

(a) Setup ready for the 8-byte setup data
(b) EP0 receive packet ready
(c) EP0 transmit packet ready
(d) EP1 transmit/receive packet ready
(e) EP2 transmit/receive packet ready
(f) EP3 transmit packet ready
(g) USB Bus reset
(h) Suspend

Although there is only one $\overline{\text{INTR}}$ pin, the local MCU can identify the contents of the interrupt by reading out the interrupt status register. These interrupts can also be masked dynamically by making individual settings in the interrupt enable register.
The causes of the interrupts, their setting and resetting conditions, and the responses to them are described below. The functions of the setup ready bit and the packet ready bit can, in some situations, be different from those described here because of some special automatic operations done by the ML60851E. Please see the descriptions of the registers EP0STAT and PKTRDY for more details of such functions.

(1) Setup ready interrupt

Operation	Source of operation	Description (conditions, responses, etc.)
Setup ready interrupt generation	ML60851E	The setup ready bit (D0 of EP0STAT) is asserted when the 8-byte setup control data is received normally and has been stored in the set of setup registers. An interrupt is generated at this time if D0 of INTENBL has been asserted. → The firmware can now read the set of setup registers.
End of setup ready interrupt	Local MCU (firmware)	After making the firmware read the 8-byte setup data, write a “1” in bit D0 of EP0 status register (EP0STAT). This causes the interrupt to be de-asserted. The interrupt will not be de-asserted If a new 8-byte setup data is received during this period. In this case, discard the setup data that was being read at that time and read the new 8-byte setup data.

The following table outlines the relationship between ML60851E registers and setup ready interrupt generation.

INTENBL(D0)	EP0STAT(D0)	INTSTAT(D0)
1	0	0
1	1	1
0	X	0

X This symbol means that it does not matter whether the value is ‘1’ or ‘0’

(2) EP0 Receive packet ready interrupt

This is used mainly during the reception of a data packet in a control write transfer.

Operation	Source of operation	Description (conditions, responses, etc.)
EP0 Receive packet ready interrupt generation	ML60851E	The EP0 receive packet ready bit (D0 of PKTRDY) is asserted during a control write transfer when the processing has changed from the setup stage to the data stage, and the ML60851E has detected EOP of the data packet and has stored the data without error in the EP0 receive FIFO. The end of a packet is recognized when an EOP has arrived in the cases of both full packets and short packets. An interrupt is generated at this time, if the EP0 receive packet ready interrupt enable bit (D3 of INTENBL) has been asserted. (EOP: End of packet)
End of EP0 receive packet ready interrupt	Local MCU (firmware)	In the case of EP0 reception, after the number of bytes of the EP0 receive FIFO data indicated by the EP0 receive byte count register (EP0RXCNT) has been read, write a '1' in the EP0 receive packet ready bit (bit D0 of PKYRDY). (This status is reset when a '1' is written in this bit.)

Note: A short packet is a packet with a number of bytes less than the maximum packet size.

The following table outlines the relationship between ML60851E registers and EP0 receive packet ready interrupt generation.

INTENBL(D3)	EP0 Rx PKTRDY(D0)	INTSTAT(D3)
1	0	0
1	1	1
0	X	0

X This symbol means that it does not matter whether the value is ‘1’ or ‘0’

(3) EP0 Transmit packet ready interrupt

This is used mainly during the transmission of a data packet in a control read transfer.

Operation	Source of operation	Description (conditions, responses, etc.)
EP0 Transmit packet ready interrupt generation	ML60851E	The EP0 transmit packet ready bit (D4 of PKTRDY) is de-asserted during a control read transfer when the processing has changed from the setup stage to the data stage, and it is possible to write the transmit data to the FIFO. At this time, an interrupt is generated if the EP0 transmit packet ready interrupt enable bit (bit D4 of INTENBL) has been asserted. For the second and subsequent packets, in addition to this condition, before the interrupt is generated, it is necessary for an ACK response to come from the host for the packet that has just been sent.
End of EP0 transmit packet ready interrupt	Local MCU (firmware)	In the case of EP0 transmission, after the one packet of the EP0 transmit data has been written in EP0TXFIFO, write a "1" into the EP0 transmit packet ready bit (bit D4 of PKTRDY). This puts the ML60851E in a state in which it can transmit the data (that is, it can transmit the data packet when an IN token arrives), and the $\overline{\text{INTR}}$ pin is de-asserted at the same time. Even when the number of bytes in the write data is less than the maximum packet size, it is possible to transmit the data by writing a "1" into the transmit packet ready status bit. This makes it possible to transmit a short packet.

The following table outlines the relationship between ML60851E registers and EP0 transmit packet ready interrupt generation.

INTENBL(D4)	EP0 Tx PKTRDY(D4)	INTSTAT(D4)
1	0	1
1	1	0
0	X	0

X This symbol means that it does not matter whether the value is '1' or '0'

(4) Receive packet ready interrupts (EP1, EP2)
These interrupts are generated when the respective EP has received an appropriate data packet from the USB bus and the local MCU can read that data.

Operation	Source of operation	Description (conditions, responses, etc.)
Receive packet ready interrupt generation	ML60851E	The receive packet ready bit of the corresponding EP status register (EPnSTAT) is asserted during data reception when the EOP of the data packet has been received and the data has been stored without error in the corresponding FIFO. The end of a packet is recognized when an EOP has arrived in the cases of both full packets and short packets. An interrupt is generated at this time, if the corresponding receive packet ready interrupt enable bit has been asserted. (EOP: End of packet)
End of receive packet ready interrupt	Local MCU (firmware)	After the number of bytes in the receive FIFO data (EPnFIFO) indicated by the corresponding receive byte count register (EPnRXCNT) has been read, write a “1” into the respective receive packet ready bit of the end point packet ready register (PKTRDY). (This bit is reset when a '1' is written in this bit.)

The following table outlines the relationship between ML60851E registers and packet ready interrupt generation during EP1 or EP2 receive (host to device communication) operation.

INTENBL(D1/D2)*	EPnCON(D7)	Rx PKTRDY(D1/D2)*	INTSTAT(D1/D2)*
1	0	0	0
1	0	1	1
1	1	X	0
0	X	X	0

* Use D1 bit when considering EP1 operation or use D2 bit when considering EP2 operation

(5) Transmit packet ready interrupts (EP1, EP2, EP3)
These interrupts are generated when it is possible for the local MCU to write the data packet to be sent to the USB bus from the corresponding EP.

Operation	Source of operation	Description (conditions, responses, etc.)
Transmit packet ready interrupt generation	ML60851E	(1) In the case of bulk transfer and interrupt transfer When the respective EP has been set for transmission, the transmit packet ready bit of the corresponding EP is de-asserted when it is possible to write the transmit data into the FIFO. At this time, an interrupt is generated if the corresponding EP transmit packet ready interrupt enable bit (INTENBL) has been asserted. For the second and subsequent packets, in addition to this condition, before the interrupt is generated, it is necessary for an ACK response to come from the host for the packet that has just been sent.
End of transmit packet ready interrupt	Local MCU (firmware)	(1) In the case of bulk transfer and interrupt transfer After the one packet of the corresponding EP transmit data has been written in EPnTXFIFO, write a "1" into the corresponding transmit packet ready bit (PKTRDY register). This puts the ML60851E in a state in which it can transmit the data and the $\overline{\text{INTR}}$ pin is de-asserted at the same time. When the number of bytes in the write data is less than the maximum payload size of the endpoint, a short packet can be transmitted by writing a "1" into the transmit packet ready bit (PKTRDY register).

The following table outlines the relationship between ML60851E registers and packet ready interrupt generation during a transmit (device to host communication) operation.

INTENBL(D1/D2/D7)*	EPnCON(D7)[I]	Tx PKTRDY(D5/D6/D7)*	INTSTAT(D1/D2/D7)*
1	0	X	0
1	1	1	0
1	1	0	1
0	X	X	0

X This symbol means that it does not matter whether the value is '1' or '0'
* Use the appropriate bit field corresponding to the endpoint being considered
I EP3 is only capable of transmission and hence this register does not play a roll in interrupt generation of EP3

(6)USB Bus reset interrupt

Operation	Source of operation	Description (conditions, responses, etc.)
USB Bus reset interrupt generation	ML60851E	The ML60851E automatically detects the condition when the SE0 state continues for 2.5 µs or longer at the D+ and D– pins. → Carry this out by firmware processing for bus reset.
End of USB bus reset interrupt	Local MCU (firmware)	Write a “1” into the device status register (bit D5 of DVCSTAT).

(7) Suspend state interrupt

Operation	Source of operation	Description (conditions, responses, etc.)
Suspend state interrupt generation	ML60851E	When the idle condition persists for 3ms or more at the D+ and D– pins. → Perform firmware processing to the suspend state if needed in your system.
End of suspend state interrupt	ML60851E	When an EOP, which marks the end of resume signal, is detected.

• DMA (Direct Memory Access)

It is possible to carry out 8-bit wide or 16-bit wide DMA transfer for the bulk transfer of EP1. The data bus used is the following:

During 8-bit transfer: AD7 to AD0
During 16-bit transfer: D15 toD8, AD7 to AD0

Demand transfer and single transfer are supported. The settings of the DMA transfer mode and parameters are done using the DMA control register and the DMA interval register described later in this manual.

In the demand transfer mode, the $\overline{\text{DREQ}}$ pin is asserted when the reading or writing of a data packet becomes possible. The $\overline{\text{DREQ}}$ pin is de-asserted when the transfer of all the data of the receive packets is completed by the external DMA controller. Therefore, other devices cannot access the local bus during DMA transfer.

On the other hand, in the single transfer mode, the $\overline{\text{DREQ}}$ pin is de-asserted at the end of transfer of the number of bytes (or words) of one transfer, and the other devices can access the local bus during this period.

• Power-down

By setting the system control register (SYSCON) to value A0h, the oscillator circuit of the ML60851E can be stopped and the ML60851E enters the power-down state.

The ML60851E cannot communicate with the USB bus after the internal oscillations are stopped.

In order to communicate with the USB bus after the termination of the power-down state, the internal oscillations should be restarted and the initial settings should be done. Therefore, the ML60851E should not be powered down during normal operation.

Note 1: Assertion of the $\overline{\text{RESET}}$ signal causes the internal oscillations to be restarted.
Note 2: In the power-down state, reads and writes to the registers are possible but reads or writes to FIFO are not possible.

• Control transfer

(a) Setup stage
The setup token and 8 bytes of setup data are transmitted from the host. The ML60851E decodes the setup token, and automatically stores the 8 bytes of setup data in the setup registers. When this is completed normally, the ML60851E returns an ACK to the host.
The 8-byte setup data is the standard request code defined in Section 9.3 of the USB Standards, or a code of the requests unique to each device class, etc. The request is decoded on the local MCU side.

(b) Data stage
If the request specified by the 8-byte setup data is also accompanied by transfer of parameter data from the host to the device, the transfer is a control write transfer, and the OUT token and the data packet are transmitted from the host. When these are received normally, the ML60851E stores the parameter data in the EP0 receive FIFO and returns ACK to the host.
If the request is accompanied by transfer of parameter data from the device to the host, the transfer is a control read transfer, and when the host sends the IN token, the ML60851E sends the parameter data that was already stored beforehand in the EP0 transmit FIFO by the local MCU. When the host receives this normally, it returns an ACK to the ML60851E.
On the other hand, in the case of requests that do not contain any parameter data that need to be transmitted or received, this data stage will not be present and the processing proceeds directly to the status stage from the setup stage.

(c) Status stage
The status stage is a stage intended for reporting the status of the result of executing a request from the device to the host. During a control write transfer or a control transfer without data, the IN token is sent by the host, and the ML60851E returns a response to it. During a control read transfer, the OUT token and data of zero length are sent by the host, and the ML60851E returns a response to it.

• Data packet transmission and reception procedure during bulk transfer and interrupt transfer modes

The ML60851E is normally used on the peripheral device side. In this method of use, the ML60851E is connected on one side to the host via the USB bus and is connected on the other side via a parallel interface to the local microcontroller (local MCU) inside the peripheral device.
The transfer of data is the major function in all types of transfermodes other than the control transfer mode. When carrying out transfer of data packets between the ML60851E and the host, the following packet communication is carried out via the USB bus for the data transfer of each packet.

(a) Token packet transfer (IN token or OUT token) from the host to the ML60851E.

(b) Data packet transfer in the desired direction (from the host to the device or from the device to the host).

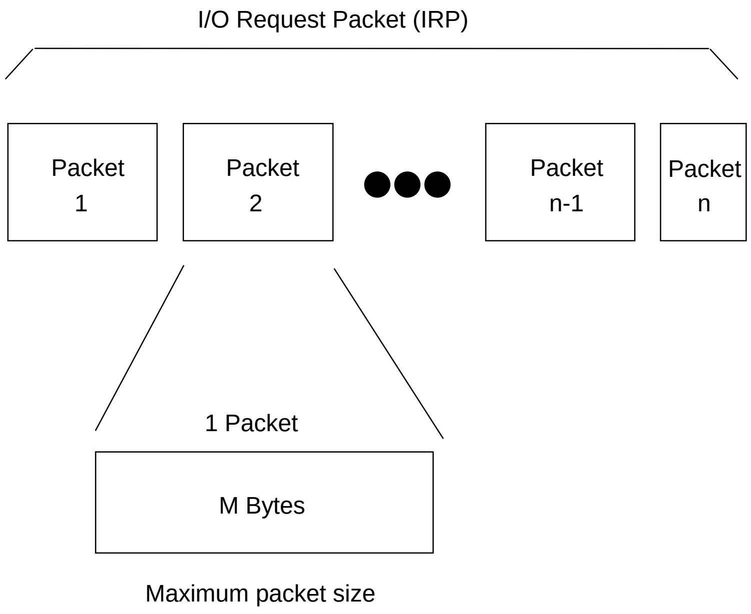
(c) Transfer of handshake packet in a direction opposite to that of the data packet.
When packet transfer is completed normally, an ACK packet is returned in step (c) and the operation proceeds to the next packet transfer.
The ML60851E requests the local MCU to transmit or receive a packet of data by asserting the $\overline{\text{INTR}}$ pin. The interrupt cause will be "packet ready". The transmit packet ready interrupt is one that requests that the packet of data to be transmitted be written in the transmit FIFO, and the receive packet ready interrupt is one that requests the local MCU to read out the data that has been received and stored in the receive FIFO.
The above procedures of transferring one packet of data are explained below for transmission and reception separately.

1) During transmission
The local MCU writes one packet of data that has to be transmitted in the transmit FIFO of the corresponding EP in the ML60851E, and sets the transmit packet ready bit of the corresponding EP status register of the ML60851E. When the host transmits the IN token packet to the ML60851E specifying the communication method, etc., the ML60851E transmits to the host the data packet stored in the above transmit FIFO. When the host receives one data packet normally, it returns the ACK packet to the ML60851E. Consequently, the ML60851E resets the transmit packet ready status, thereby completing the transfer of one data packet over the USB bus. When the transmit packet ready status is reset, the ML60851E gives a request to the local MCU in terms of a transmit packet ready interrupt thereby prompting the local MCU to write the next packet of data to be transmitted.

2) During reception
The host sends to the ML60851E an OUT token followed by a data packet. The ML60851E stores the received data packet in the receive FIFO of the corresponding EP. When it is confirmed that all the data packets have been accumulated and that there is no error, the ML60851E returns an ACK packet to the host. At the same time, the receive packet ready bit of the corresponding EP status register will also be set and a request is sent to the local MCU in terms of an interrupt. Upon receiving this interrupt, the local MCU reads out the received data from the ML60851E and resets the receive packet ready bit.

• Packets and packet sizes

The ML60851E packs the transmit data into packets and unpacks (restores to the original form) the received data. The packed data that is recognized by the software client is a set of data consisting of one or more packets, and this is called an I/O request (IRP).
Among the several packets in an IRP, all the packets other than the last packet are transferred with the maximum packet size. Only the last packet can be transferred as a "short packet", that is, a packet whose size is less than the maximum packet size.



The ML60851E has payload registers corresponding to each end point, and it is possible to set the maximum packet size for each end point in these registers. The maximum packet size should be within the capacity of the corresponding FIFO, and can be set as follows:

(1) EP0 Receive packet size can be 8 bytes or less;
(2) EP0 Transmit packet size can be 8 bytes or less;
(3) EP1 Transmit/receive packet size can be 64 bytes or less;
(4) EP2 Transmit/receive packet size can be 64 bytes or less;
(5) EP3 Transmit packet size can be 8 bytes or less;

On the USB bus, the separation between successive packets is distinguished by appending a special signal condition called EOP (End of Packet) at the end of each packet. The appending of EOP during transmission and the detection and removal of EOP during reception are carried out by the ML60851E automatically.

(1) At the time of transmission, the packet is deemed to have ended when the local MCU has completed writing the required number of bytes of data in the transmit FIFO and has then asserted the transmit ready status bit. (The actual addition of EOP is executed at the time of transmitting the data over the USB bus after waiting for the IN token from the host.) The packet will be a short packet if the transmit packet ready status bit is asserted after writing data with less number of bytes than the maximum packet size. In particular, by asserting the transmit packet ready status bit without writing any data, it is possible to form a null packet whose data length is zero.

(2) At the time of reception, when an EOP is detected in the received data string, the ML60851E recognizes it as the end of the received packet and asserts the receive packet ready status bit. The number of bytes in the received packet is counted automatically in the receive byte count register (EP0RXCNT, EP1RXCNT or EP2RXCNT) corresponding to that end point.

• **Operation of 2-layer structure FIFO during bulk transfer**

The FIFOs of EP1 have a 64 bytes x 2-layer structure. As a consequence, these FIFOs can temporarily store a maximum of 128 bytes of bulk transfer data.

(1) 2-Layer reception operation (O indicates the assert condition and X indicates de-assert condition)
The following description assumes that interrupt has been enabled for EP1 (D1 of INTENBL=1)

	In the case of 1→2→3→4→5a→6 In the case of 1→2→3→4→5b→6	Layer A 64 bytes	Layer B 64 bytes	Layer A PKT RDY	Layer B PKT RDY	EP1 receive PKT RDY	$\overline{\text{INTR}}$
1	Start storing data in layer A of reception			×	×	×	×
2	Data of one packet has been stored.			○	×	○	○
3	Start reception and storing of data in layer B.			○	×	○	○
4	Local MCU starts reading layer A.			○	×	○	○
5a	When the storing of packet in layer B is completed following the completion of reading layer A.			○	○	○	○
5b	When the reading of packet in layer A is completed following the completion of storing data in layer B.	changed		×	×	×	×
6	From 5a: Layer A has become empty. From 5b: Layer B has become full.			×	○	○	○
7	Starting reading layer B also.			×	○	○	○

- When one packet of receive data is stored in layer A of the FIFO and EOP is received, the ML60851E asserts the packet ready bit of EP1 and also asserts the $\overline{\text{INTR}}$ pin. This makes it possible for the local MCU to read the receive data.
- Subsequently, data can be received from the host, and the ML60851E switches the FIFO for storing to layer B.
- When one packet of data described above has been read from layer A of the FIFO, make the local MCU reset the receive packet ready status of EP1 (by writing a "1" into bit D1 of PKTRDY).
- At the time the EP1 receive packet ready status is reset, if the reception of layer B has not been completed, the ML60851E resets the EP1 receive packet ready status and de-asserts the $\overline{\text{INTR}}$ pin.
- However, if the reception of layer B has been completed at the time the EP1 receive packet ready status is reset, the ML60851E rejects the request from the local MCU to reset the EP1 receive packet ready status, and continues to maintain the EP1 receive packet ready status and the asserted condition of the $\overline{\text{INTR}}$ pin.

(2) 2-Layer transmission operation (O indicates the assert (set to “1”) condition and X indicates de-assert (set to “0”) condition)

	In the case of 1→2→3→4→5a→6 In the case of 1→2→3→4→5b→6	Layer A 64 bytes	Layer B 64 bytes	Layer A PKT RDY	Layer B PKT RDY	EP1 transmit PKT RDY	$\overline{\text{INTR}}$
1	Layer A and layer B are both empty.			×	×	×	○
2	The local MCU starts writing into layer A.			×	×	×	○
3	Writing of one packet is completed.			○	×	×	○
4	Data of layer A is being transmitted while the next packet is being written in layer B.			○	×	×	○
5a	When layer A is still being transmitted while writing in layer B is completed.			○	○	○	×
5b	When layer B is still being written while layer A has already become empty.			×	×	×	○
6	From 5a: Layer A has become empty. From 5b: Layer B has become full.			×	○	×	○
7	Transmission of layer B is also started.			×	○	×	○

- If the EP1 transmit packet ready interrupt enable bit has been asserted, the transmit FIFO is empty, and EP1 transmit packet ready bit is de-asserted, the EP1 transmit packet ready interrupt is asserted. This makes it possible to write the transmit data into the EP1 transmit FIFO.
- When the data of one packet is written in layer A FIFO, make the local MCU set the transmit packet ready status (D5 of PKTRDY set to “1”). By setting the transmit packet ready status, it becomes possible to transmit data to the host. At this time, since layer B is still empty, the $\overline{\text{INTR}}$ pin maintains the asserted condition, thereby indicating that the next packet data can be written. In this case, although bit D5 of PKTRDY remains in the “0” condition, the ML60851E recognizes that transmission is possible from layer A and starts transmission when an IN token is received from the host.
- It is possible for the local MCU to write the next packet of transmit data in the layer B FIFO while the data in layer A is being transmitted over the USB bus.
- When the writing of the data to be transmitted in layer B has been completed, the local MCU sets the transmit packet ready bit, and the $\overline{\text{INTR}}$ pin becomes de-asserted at this time if the transmission of layer A data has not been completed (that is, the ACK message is received from the host and the transmit packet ready bit is reset). The local MCU cannot yet write the subsequent packet.
- If the layer A becomes empty before layer B goes into the transmit enable condition and transmission is carried out normally, an ACK response is received from the host. The $\overline{\text{INTR}}$ pin remains asserted, and the local MCU can write data into layer A FIFO after writing into layer B FIFO.
- The transmission of data in layer A is continued from the state 4a, and when layer A becomes empty and the transmission is completed normally, an ACK response is received from the host, whereupon the ML60851E asserts the $\overline{\text{INTR}}$ pin thereby prompting the local MCU to write data into layer A.

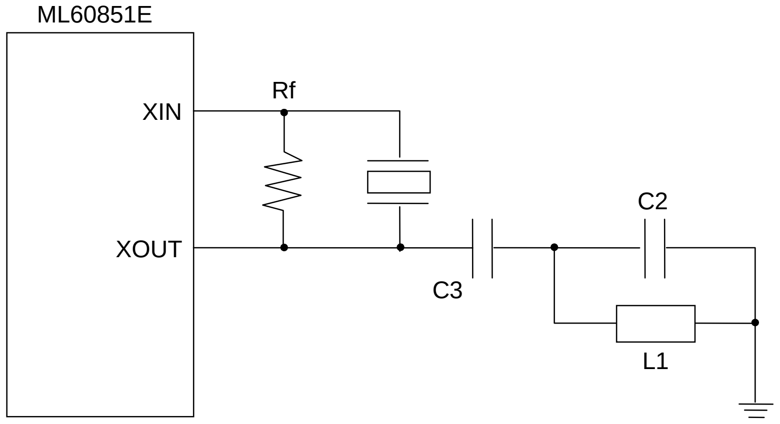
• Error processing and retry operation

1) Error processing during transmission
When an error such as a CRC error is detected in the data transmitted by the ML60851E, the host will not send the ACK packet, and hence the ML60851E does not reset the transmit packet ready status, but waits while retaining the current packet of data. The current packet of data is transmitted again when the next IN token is received from the host.

2) Error processing during reception
When an error is detected in the data received over the USB bus, the ML60851E does not assert the interrupt signal to the local MCU and will also not send any message to the host (leading to a timeout condition).
When the timeout condition is generated, the host recognizes that an error has occurred, and can take measures such as re-transmitting the data, etc. In addition, since no interrupt request is generated, the local MCU will not read the erroneous data.

EXAMPLE OF OSCILLATOR CIRCUIT

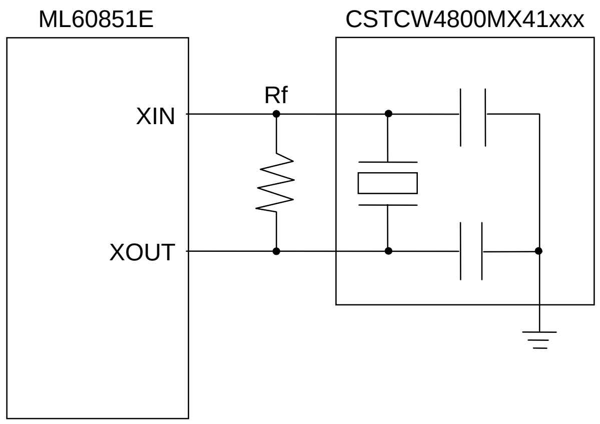
• Oscillation Circuit Example 1



Crystal: HC-49U (KINSEKI, LTD)
C2 = 5 pF
C3 = 1000 pF
Rf = 1 MΩ
L1 = 2.2 μH

Note: The example shown above is not guaranteed for circuit operation.

• Oscillation Circuit Example 2



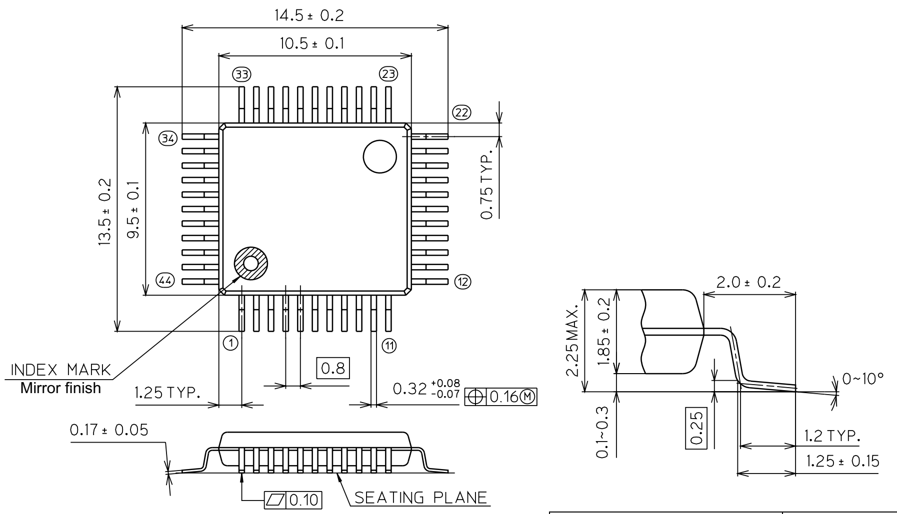
Ceramic oscillator: CSTCM4800MXxxx (MURATA MFG.)
(C-built-in type)

Note: The example shown above is not guaranteed for circuit operation.

PACKAGE DIMENSIONS

(Unit: mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

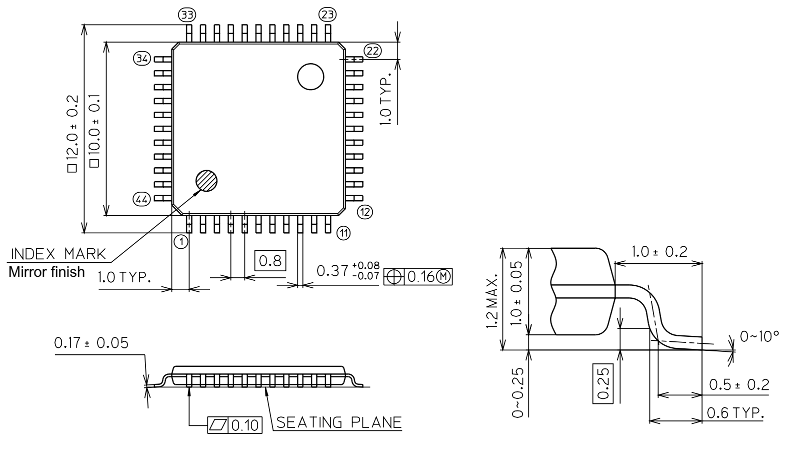
Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

TQFP44-P-1010-0.80-K



Oki Electric Industry Co., Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.28 TYP.
Rev. No./Last Revised	5/Oct. 28, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki’s responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL60851E-01	Nov. 27, 2002	–	–	Final edition 1
FEDL60851E-02	Dec. 16, 2002	–	–	Final edition 2
		–	–	USB compliant changed from “1.1” to “2.0”

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.