National Semiconductor Corporation

PRELIMINARY

MM57409 Super Number Cruncher

General Description

The Super Number Cruncher (SNC) is an MOS/LSI arithmetic processor (actually, a pre-programmed member of National's single-chip microcontroller COPS™ family) intended for use in number processing applications. Scientific calculator functions, conditional output capability, internal number storage, and input/output instructions have been combined in this single chip device. Programming is done in calculator keyboard level language which simplifies software development. Data or instructions can be synchronous or asynchronous, I/O digit count, I/O notation mode, and error control are user programmable; a sense input and flag outputs are available for single bit control; and instructions and lines are available for I/O expansion.

Applications

- Instruments
- Microprocessor/minicomputer peripheral
- Test Equipment
  Process controllers

Features

- Scientific calculator instructions (RPN)
  - Up to 12-digit mantissa, 2-digit exponent
  - 4-register stack, one memory register
  - Trigonometric functions, logarithmic functions, Y^X, e^X, π
  - Error flag generation and recovery
- Flexible input/output
  - Multidigit OUT instruction with foating-point or scientific notations
  - Programmable mantissa digit count for OUT instruction
  - Sense input and flag outputs
  - Eight high-impedance I/O lines (TRI-STATE®), six I/O lines, and four output lines for I/O expansion.
- Interface simplicity
  - On-chip clock OSC
  - Generates all I/O control signals
  - MICROBUS™ interface

Block Diagram

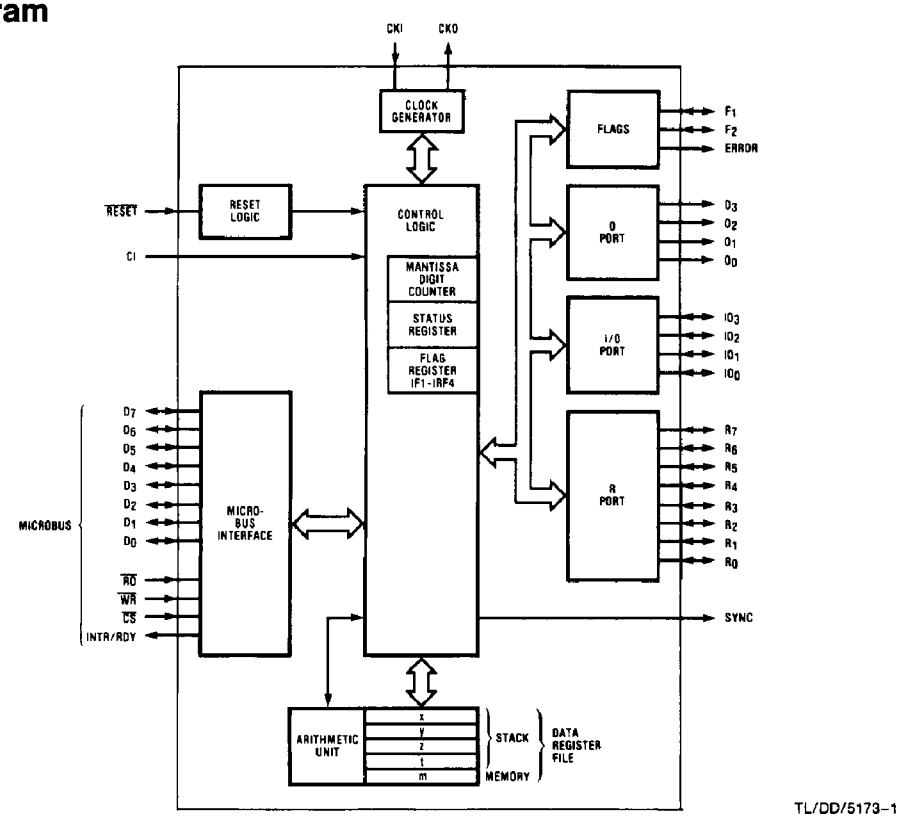

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FIGURE 1

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Voltage at Any Pin Relative to GND	−0.5V to +7V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +50°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	0.75W at 25°C 0.4W at 70°C
Total Source Current	80 mA
Total Sink Current	75 mA

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not insured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A \le 70°C$; $4.5V \le V_{CC} \le 6.3V$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})	(Note 1)	4.5	6.3	V
Power Supply Ripple	(Peak to Peak)		0.4	V
Operating Supply Current	All inputs and outputs open			
	$T_A = 0°C$		41	mA
	$T_A = 25°C$		35	
	$T_A = 70°C$		27	
Input Voltage Levels				
CKI				
Logic High (V_{IH})	$V_{CC} = 5V \pm 5\%$	2.0		
Logic Low (V_{IL})	$V_{CC} = 5V \pm 5\%$	−0.3	0.4	
Logic High (V_{IH})	V_{CC} = Max	2.5		
$\overline{RESET}$				
Logic High		0.7 V_{CC}		V
Logic Low		−0.3	0.6	
All Other Inputs				
Logic High	V_{CC} = Max	2.5		
Logic High	$V_{CC} = 5V \pm 5\%$	2.0		
Logic Low		−0.3	0.8	
Input Capacitance			7.0	pF
Input Leakage ($\overline{RD}$, $\overline{CS}$, $\overline{WR}$)		−1.0	1.0	μA
Output Voltage Levels				
TTL Operation				
Logic High (V_{OH})	$I_{OH} = -100\ \mu A$	2.4		
Logic Low (V_{OL})	$I_{OL} = 1.6$ mA		0.4	V
CMOS Operation				
Logic High (V_{OH})	$I_{OH} = -10\ \mu A$	$V_{CC} - 0.4$		
Logic Low (V_{OL})	$I_{OL} = 10\ \mu A$		0.2	
Output Current Levels				
Output Source Current	$V_{CC} = 4.5V$			
	$V_{OH} = 2.4V$	−100	−650	μA
TRI-STATE Output Leakage				
Current (R, D Lines)		−2.5	2.5	μA
CKO Output				
Output Source Current (I_{OH})	$V_{OH} = 2.0V$	−0.2		mA
Output Sink Current (I_{OL})	$V_{OL} = 0.4V$	0.4		mA
Input Current Levels				
Input Load Source Current	$V_{IH} = 2.0V$	14	230	μA
(CI, $\overline{RESET}$)	V_{CC} 4.5V			
Total Sink Current Allowed				
All I/O Combined			75	mA
Each D, R Port			20	mA
Each, O, I/O, F1, F2			10	mA
SYNC Line			2.5	mA
Total Source Current Allowed				
All I/O Combined			80	
Each D Pin			5.0	mA
All Other Output Pins			1.6	

AC Electrical Characteristics $0°C \le T_A \le 70°C$; $4.5V \le V_{CC} \le 6.3V$, unless otherwise noted.

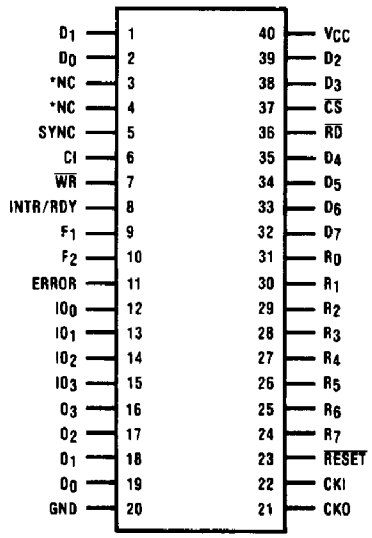
Parameter	Conditions	Min	Max	Units
Microcycle Time (tm)		4.0	10	μs
CKI Frequency (f_I)		1.6	4.0	MHz
Duty Cycle (Note 2)	f_I = 4.0 MHz	30	60	%
Rise Time			60	ns
Fall Time			40	ns
Inputs *(Figure 3)*				
t_{SETUP}		1.7		μs
t_{HOLD}		300		ns
Output Propagation Delay	C_L = 50 PF			
(Figure 3)	V_{OUT} = 1.5V			
CKO t_{PD1}, t_{PD0}			0.17	μs
SYNC t_{PD1}, t_{PD0}	R_L = 2.4 kΩ		1.0	μs
All Other Outputs	R_L = 5.0 kΩ		1.4	μs
MICROBUS Timing	C_L = 100 pF			
	V_{CC} = 5V ±5%			
Read Operation *(Figure 4)*				
$\overline{CS}$ Stable Before $\overline{RD}$—t_{CSR}		65		
$\overline{CS}$ Hold Time for $\overline{RD}$—t_{RCS}		20		
$\overline{RD}$ Pulse Width—t_{RR}		400		
Data Delay from $\overline{RD}$—t_{RD}			375	
$\overline{RD}$ to Data Floating—t_{DF}			250	ns
Write Operation *(Figure 5)*				
$\overline{CS}$ Stable Before $\overline{WR}$—t_{CSW}		65		
$\overline{CS}$ Hold Time for $\overline{WR}$—t_{WCS}		20		
$\overline{WR}$ Pulse Width—t_{WW}		400		
Data Setup Time—t_{DW}		320		
Data Hold Time—t_{WD}		100		
INTD/RDY Transition Time from $\overline{WR}$—t_{WI}			700	

Note 1: V_{CC} voltage change must be less than 0.5V in a 1 ms period to maintain proper operation.

Note 2: Duty Cycle = $t_{W1}/(t_{W1} + t_{W0})$.

Connection Diagram

Dual-In-Line



Top View TL/DD/5173-2

*NC means no external connection allowed on these pins.

FIGURE 2

Molded Dual-In-Line Package (N)
Order Number MM57409N
See NS Package Number N40A

Pin Name	Description
D_0–D_7	8-Bit Data Bus (bidirectional)
IO_0–IO_3	4-Bit I/O Lines (bidirectional)
O_0–O_3	4-Bit Output Lines
R_0–R_7	8-Bit Bidirectional I/O Lines with TRI-STATE
ERROR	Error Flag Line
V_{CC}, GND	Power Supply
F1, F2	Two Bidirectional Flags
INTR/RDY, $\overline{WR}$ $\overline{RD}$, $\overline{CS}$	MICROBUS Handshake Signals
$\overline{RESET}$	System Reset
SYNC	Microcycle Clock
CKI, CKO	System Oscillator
CI	Test/Conditional Input

Functional Description

The MM57409 Super Number Cruncher (SNC) is intended for microprocessor number processing applications as a microcomputer peripheral device. The block diagram of the SNC is shown in *Figure 1*. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other. Positive logic is used, i.e., when a bit is set, it is a logic "1" (greater than 2V) and when a bit is reset, it is a logic "0" (less than 0.8V).

INTERNAL LOGIC

The data register file, consisting of a 4-level stack and one memory location, is the source and destination register for all mathematic operations. The organization of an x, y, z, or t level is shown in *Figure 6*. The structure of the M (memory) level is similar, lacking only the guard/link digit. The mantissa and the exponent each have a sign, which may be read or changed by SNC instructions. The guard/link digit in each of the x, y, z, and t levels of the stack is used for the execution of the arithmetic instructions. Regardless of any operating mode, all data internal to the SNC is stored in scientific notation format with the mantissa rounded to 12 digits.

The arithmetic unit performs all mathematic operations of the MM57409, storing its results in the data register file.

The R port can be used as an 8-bit high-impedance I/O port. If the R port is to be used, the first instruction the SNC must receive after a power up or reset is the RIO instruction. The state of the R port will be 03 hex. A host processor can then instruct the SNC to output an 8-bit value to the R port or read the state of the R lines. Before reading the input state of the R lines, the lines *must be* put into a high-impedance mode. The R lines are then high-impedance inputs and must be externally driven high or low.

An external processor may also cause a 4-bit value to be output to either the O or I/O ports. The input state of the I/O port or the present state of the output lines of the O port may be read from the SNC. If the I/O lines are to be used as inputs, the value F must first be written to the port using the I/O instruction.

Two flags are provided on the SNC—F1 and F2. These flags may be set high or pulsed high through the use of appropriate SNC instructions. When pulsed, the pulse width of F1 is four microcycles and the pulse width of F2 is three microcycles. (A microcycle is the external clock input divided by 16—see Oscillator section for further information.) These flags may also be tested by test/conditional output instructions if they are first set high. An external test input (CI) is also provided for conditional output control and is tested by the TCI instruction.

There are four general purpose internal flags (IF1–IF4) in the SNC that can be reset, or tested using the appropriate instructions.

OPERATING MODES

The SNC has several user controllable operating modes. Any combination of these modes may be selected. These modes are:

1. Angular mode—The SNC can be instructed to accept and return data in either degrees or radians.
2. Input/Output mode—The SNC will accept and output numerical data in either scientific notation (signed exponent and mantissa) or floating-point (decimal point position, signed mantissa). Note that only the input or output data can be in floating-point or scientific notation—the data internal to the SNC is always in scientific notation.
3. Rounding—The SNC can be instructed to round the output to the Mantissa Digit Count (MDC). This rounding may also be disabled. The rounding mode causes rounding on the output data only—the data internal to the SNC is still in scientific notation format with the mantissa rounded to 12 digits.

Note: If both the floating-point I/O mode and the rounding mode are selected, the output data is rounded to the MDC before it is converted to the floating-point mode. This means that fractional numbers ($|x| < 1$) may not appear to be rounded.

4. Mantissa Digit Counter (MDC)—The number of digits the SNC expects in the mantissa during the multiple digit OUT operation may be set anywhere between 1 and 12.

Functional Description (Continued)

STATUS REGISTER

The SNC contains an 8-bit status register *(Figure 7)* which the host can read to determine the exact status of the SNC. The various status information is described below.

Bit 7: Scientific Notation/Floating-Point I/O mode
(MSB) = 1 indicates floating-point I/O
= 0 indicates scientific notation I/O

Bit 6: Rounding
= 1 indicates no rounding to MDC is performed
= 0 indicates rounding to MDC is performed

Bit 5: Not Used

Bit 4: Angular Mode
= 1 indicates angles are expressed in radians
= 0 indicates angles are expressed in degrees

Bit 3: Status of x stack level as fraction
= 1 indicates the absolute value of x is a non-zero fraction
= 0 indicates the absolute value of x is ≥ 1

Bit 2: Polarity of x register
= 1 indicates $x < 0$
= 0 indicates $x > 0$ or $x = 0$

Bit 1: x equivalence to 0
= 1 indicates $x = 0$
= 0 indicates $x \neq$ zero

Bit 0: Error
= 1 indicates an error has occurred
= 0 indicates no error

OSCILLATOR

An oscillator between 1.6 MHz and 4 MHz is required. This may be supplied from an external oscillator that is input to CKI or through the use of the external crystal network as shown in *Figure 8*. In either case, the frequency at CKI is divided by 16 to provide the basic timing reference (microcycle) for the SNC. This signal is available at the SYNC output. A single period of the SYNC signal (measured from rising edge to rising edge) corresponds to one microcycle. The microcycle will be between 5 and 10 μs, depending on the CKI frequency.

INITIALIZATION

The SNC is reset upon power up or upon application of a low going pulse to the $\overline{\text{RESET}}$ input. The reset pulse must be a minimum of three microcycles (three SYNC pulses) in duration in order to reliably reset the device. If the power supply rise time is greater than 1 ms, the circuit of *Figure 9* must be used.

In the reset state, R and the D ports are in a high impedance state; SYNC is the CKI inut frequency divided by 16; and O, I/O, F1, F2, ERROR, and INTR/RDY are reset to 0. The DMC is set to 10, the angular mode is set to degrees, the input/output mode is set to scientific notation, and any data output will be rounded to the MDC.

ERROR CONDITIONS

The error flag and error output are set upon detection of any of the error conditions listed in Table I. The resultant status of the SNC after an error condition is also shown in Table I. The error flag and error output are cleared only upon execution of any one of the following:

1. an ECLR (error clear) instruction
2. an MCLR (master clear) instruction
3. a hardware system reset

Timing Diagram

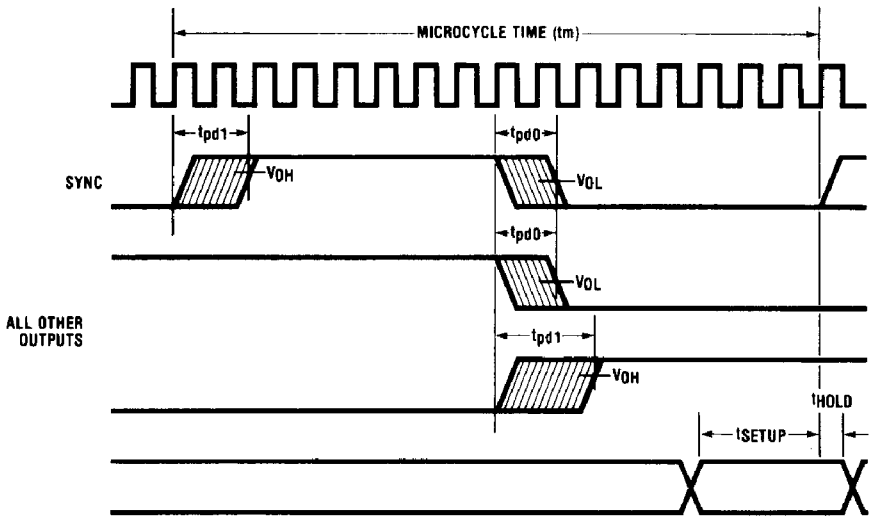


FIGURE 3. Basic Timing

Timing Diagrams (Continued)

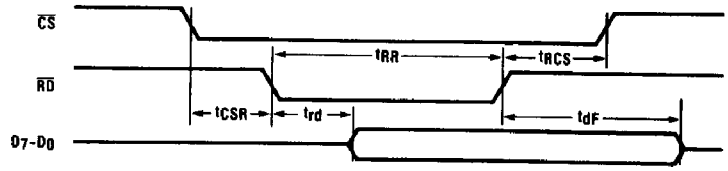


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FIGURE 4. MICROBUS Read Operation Timing

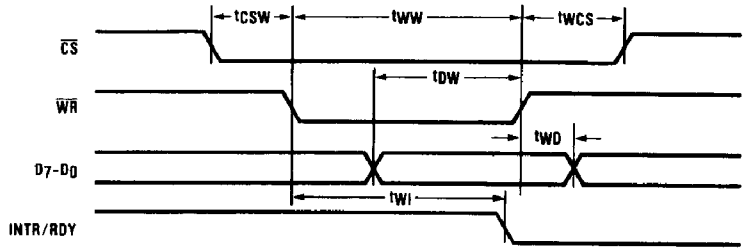

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FIGURE 5. MICROBUS Write Operation Timing

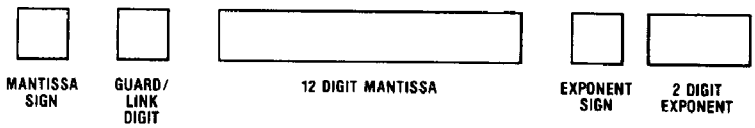

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FIGURE 6. Stack Level x, y, z or t Structure

Bit

7	0 =	Scientific Notation I/O Mode
	1 =	Floating Point I/O Mode
6	0 =	Round the Output to the MDC
	1 =	Do Not Round the Output to the MDC
5		Not Used
4	0 =	Angular Data is Expressed in Degrees
	1 =	Angular Data is Expressed in Radians
3	0 =	$\|x\| \geq 1$ or $= 0$
	1 =	$\|x\|$ is a Non-Zero Fraction
2	0 =	$x \geq 0$
	1 =	$x < 0$
1	0 =	$x \neq 0$
	1 =	$x = 0$
0	0 =	No Error Has Occurred
	1 =	Error Has Occurred

FIGURE 7. SNC Status Register

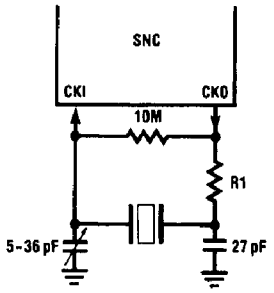

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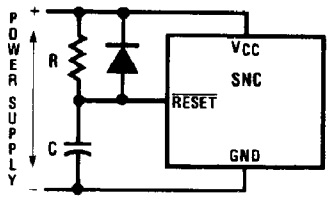
FIGURE 8. Crystal Oscillator Configuration

Crystal Oscillator

Crystal Value	R_1
4 MHz	1k
3.58 MHz	1k
2.097 MHz	2k



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RC ≥ Power Supply Rise Time

FIGURE 9. Power-Up Reset Circuit

Functional Description (Continued)

MICROBUS COMMUNICATION

The SNC communicates via an 8-bit bidirectional bus (D_0–D_7). The 8-bit instruction opcodes are sent to the SNC on this bus and data is transferred between the SNC and its host on this bus. In addition to the bus, a chip select ($\overline{CS}$), read strobe ($\overline{RD}$), write strobe ($\overline{WR}$), and an interrupt/ready signal (INTR/RDY) complete the interface. The SNC will not respond to any signal on the bus or any of the control signals unless it has been selected (i.e., $\overline{CS}$ low) by the host. The SNY is ready to receive data or an instruction whenever the INTR/RDY is high. INTR/RDY high also indicates that the SNC has data available for the host. Pulsing the $\overline{WR}$ line (write strobe) transfers the information on the bus into the SNC. The write strobe going low forces INTR/RDY to go low. INTR/RDY will not return to the high state until the SNC has completed the operation required by the previous write. Pulsing the $\overline{RD}$ line (read strobe) will cause an internal 8-bit register of the SNC to be transferred to the external bus. INTR/RDY does not go low. Therefore, a read in this manner does not affect the readiness of the SNC. The SNC is in an idle condition when INTR/RDY is high. It is waiting for the next write and it will not proceed or escape from the idle loop until the device is selected and the $\overline{WR}$ is pulsed low. This characteristic makes the interface simple and allows the device to work with a host running at any speed.

Note: Do not pulse $\overline{WR}$ with the $\overline{CS}$ low when INTR/RDY is low. This can, in some cases, create errors in the SNC.

INPUT/OUTPUT CONFIGURATIONS

The SNC input lines have the following configurations, illustrated in *Figure 10:*

1. $\overline{RD}$, $\overline{WR}$, $\overline{CS}$—High-impedance *(Figure 10a)*
2. CI, $\overline{RESET}$—Internal load device *(Figure 10b)*

The output lines have the following configurations, illustrated in *Figure 11:*

1. D_7–D_0—TRI-STATE *(Figure 11a)*
2. R_7–R_0—Push-pull with TRI-STATE *(Figure 11b)*
3. O_3–O_0, I/O_0, INTR/RDY, F1, F2, ERROR—Standard *(Figure 11c)*
4. SYNC—Push-pull *(Figure 11d)*

Number Entry Mode Description

If the SNC is not in the number entry mode, the instructions AIN1, DP, BP, PI, or the numbers 0 through 9 will initiate number entry. This means that the stack is pushed (z → t, y → z, x → y), the x register is cleared, and the number entry mode established. If a number was entered to initiate the entry mode, that digit will go into the x register; or, if EE was entered prior to the digit, that digit will go into the x exponent. The subsequent entry of numbers, DP, EE, or PI does not again initiate number entry. Up to 12 mantissa digits may be entered, MSD entered first. Any digit entered after the 12th mantissa digit will simply be ignored. Up to two exponents digits may be entered, MSD entered first. If the user enters more than two exponent digits, only the last two entered will be accepted.

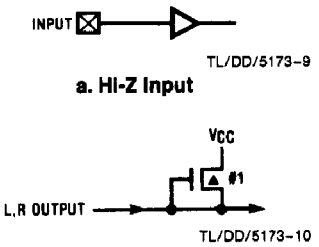
If number entry is initiated by the EE instruction, the x mantissa is loaded with a "1". Subsequent digits will go into the x exponent.

The CS instruction does not initiate number entry. It normally toggles the sign of the x mantissa. If, however, CS is entered after an EE instruction, the sign of the x exponent will be toggled if the exponent is a non-zero number. CS may be mixed with the various digit entry instructions without interference.

Only mantissa digits may be entered through the use of the AIN1 instruction. This instruction causes the SNC to enter data into the x mantissa, starting at the MSD and ending at the LSD. One digit is entered for each AIN1 instruction. This instruction is actually a 2-byte instruction. The first byte is the instruction's opcode—0E hex. When INTR/RDY goes high, the SNC will respond with a digit address (0N, where N is a number from 0 to 11, MSD → LSD). The second byte writes the address N and the data for that address back to the SNC.

The following example illustrates the first time an AIN1 is entered:

WRITE:	0E hex	(AIN1 opcode)
READ:	00 hex	(SNC says write data to mantissa address 0)
WRITE:	09 hex	(9 → mantissa digit 0)



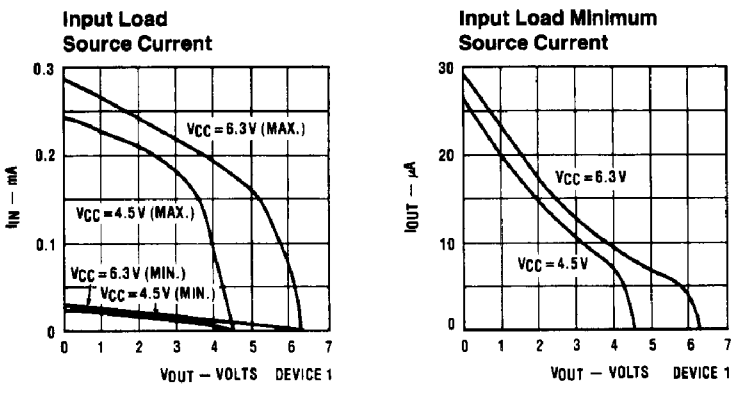
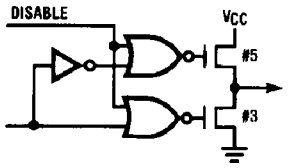


FIGURE 10. SNC Input Characteristics

Input/Output Configuration (Continued)



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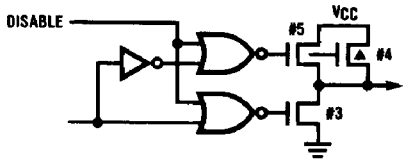
a. TRI-STATE Output



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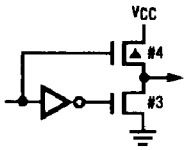
b. Push-Pull Outputs with TRI-STATE



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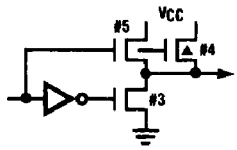
c. Standard Output



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d. Push-Pull Output

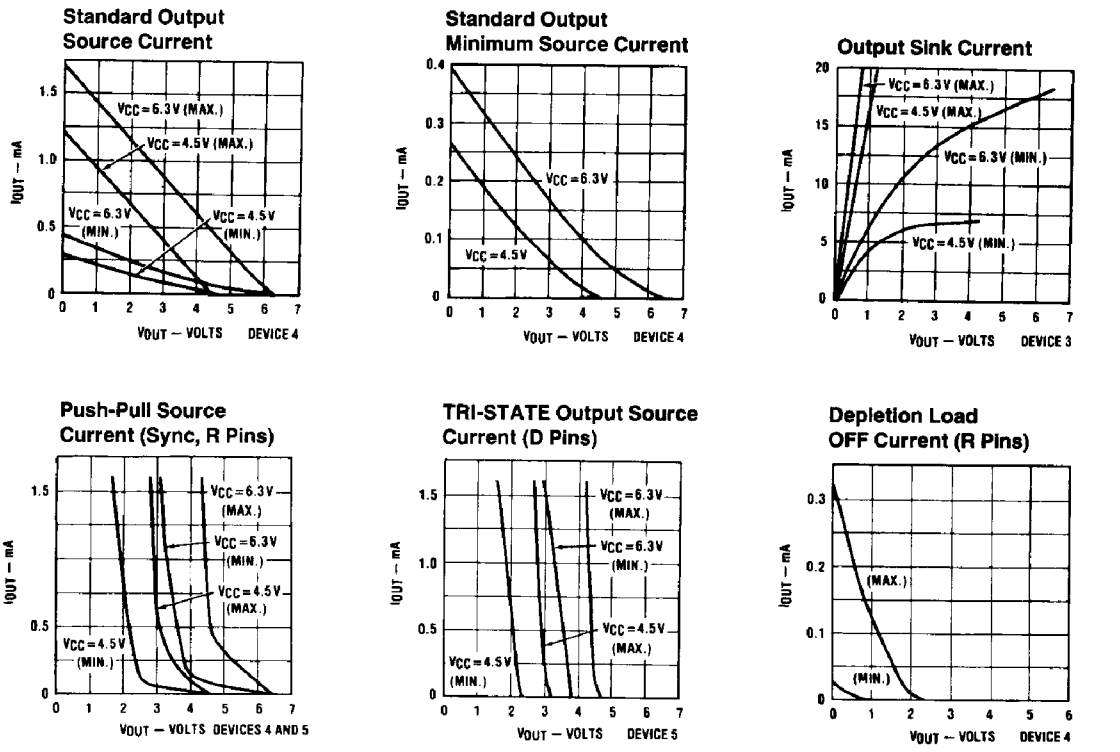

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FIGURE 11. SNC Output Characteristics

The next example illustrates when AIN1 is entered immediately after the previous example:

WRITE	0E hex	(AIN1 opcode)
AD:	01 hex	(SNC says write data to mantissa address 1)
WRITE:	15 hex	(5 → mantissa digit 1)

One exception to the number entry initiation is that the stack is not pushed if the instruction prior to an entered digit was EN (enter)—EN pushed the stack. However, the x register is still cleared and the entered data put in x.

The number entry mode is terminated by any instruction except DP, EE, CS, PI, AIN1, NOP1, or any number.

Data Input Description

The AIN2 instruction is a 2-byte, single digit asynchronous input instruction. This instruction does not initiate number entry mode and the x level of the stack is not cleared. The first byte is the instruction's opcode: 91 hex. The second byte is of the form nD where n is the digit address and D is the BCD digit. Since n is specified by the host, AIN2 can be used to write to any digit in the x register. Digits may only be entered in scientific notation format. This example will write a 7 to the MSD of the x mantissa. Refer to Table IV.

WRITE:	91 hex	(AIN2 opcode)
WRITE:	47 hex	(4 is the address of the MSD mantissa digit, 7 is data)

Data Output Description

The OUT instruction is a multidigit output instruction that will output all digits of the x register. The host writes the OUT opcode (8F hex) and the SNC will respond with the address of the data and the data in the form nD where n is the address and D is the data. The host should then write the same information back to the SNC to indicate that it received the data. This procedure continues until all data has been read by the host. The data addresses are shown in Table III for scientific notation mode and in Table II for floating-point mode.

Table V contains data formats for other output instructions.

Instruction Set Notes

Two of the TEST/CONDITIONAL OUTPUT instructions—IMNZ and DMNZ—deserve special comment. These instructions increment or decrement the memory mantissa and if the new value of the mantissa is = 0, then R will have the value contained in the operand field. The increment/decrement portion affects the entire 12-digit mantissa, starting at digit 12 (LSD), regardless of the MDC and the decimal point. So, if the host wished to decrement the memory twice and then change R, the x register would be cleared, AIN2 would be used to write a 2 to digit 12, and the memory and x would be exchanged. The host could then expect the SNC to load R upon the second execution of the DMNZ instruction.

If the host wished to observe the true results of the LSH (left shift x mantissa) and RSH (right shift x mantissa), rounding the output to the MDC should be disabled. Otherwise the shift might be obscured due to rounding.

Execution times for all SNC instructions are contained in Table VI. Typical instruction times are given for math and memory operation instructions, and worst case times given for all else. These times were found with the CKI input frequency equal to 4 MHz (4 μs microcycle time) and are measured from the rising edge of the $\overline{WR}$ signal to the rising edge of the INTR/RDY line.

TABLE I. SNC Error Conditions

	Error Condition	SNC Status
1.	ln x or log x when x is ≤ 0	x, y, z, t, M unchanged
2.	x+y, x−y, x*y, or y/x when result is ≤ 10^{100} or < 10^{-99}	Previous x → y; x is invalid data
3.	M+x, M−x, M*x, or M/x which result is ≥ 10^{100} or < 10^{-99}	y, z, t, M unchanged; x is invalid data
4.	Tan 90°, 270°, 450°, etc.	y, z, t, M unchanged; x is invalid data
5.	Sin x, Cos x, or Tan x when the absolute value of x is ≤ 9000° (157.08 radians)	y, z, t, M unchanged; x is invalid data
6.	arcsin x or across x when the absolute value of x is > 1 or ≤ 10^{-50}	y, z, t, M unchanged; x is invalid data
7.	square root of x when x < 0	x, y, z, t, M unchanged
8.	y/x when x = 0	x, y swapped; z, t, M unchanged
9.	1/x when x = 0	1 → x, y, z, t, M unchanged
10.	M/x when x = 0	M to x; y, z, t, M unchanged
11.	y^x when y ≤ 0	x, y swapped; z, t, M unchanged
12.	Floating-point OUT instruction when the number of mantissa digits to the left of the decimal point is > 12	x, y, z, t, M unchanged
13.	Attempt to enter a number ≥ 10^{100} or < 10^{-99}	Error occurs on termination of number entry mode. The stack push at initiation of number entry will occur normally. x contains invalid data.

TABLE II. OUT Instruction—Floating-Point

D_7–D_4	DPX	D_3	D_2	D_1	D_0
2		Sm	0	0	Se
3		Decimal Point Position (DP POS).			
4	11	Most significant mantissa digit. On the Out instruction, this digit will be nonzero unless $\|x\| < 1$, in which case it will be zero and decimal point position will be 11.			
5	10	Second most significant mantissa digit.			
.	.	.			
.	.	.			
.	.	.			
MDC+3	2−MDC	Least significant mantissa digit.			

TABLE III. OUT Instruction—Scientific Notation

D_7–D_4	D_3	D_2	D_1	D_0
0	Most significant exponent digit.			
1	Least significant exponent digit.			
2	Sm	0	0	Se
3	Not used.			
4	Most significant mantissa digit. Decimal point follows this digit.			
5	Second most significant mantissa digit.			
.	.			
.	.			
.	.			
MDC+3	Least significant mantissa digit.			

TABLE IV. AIN2 Instruction

D_7–D_4	D_3	D_2	D_1	D_0
0	Most significant exponent digit.			
1	Least significant exponent digit.			
2	Sm	0	0	Se
3	Not used.			
4	Most significant mantissa digit.			
5	Second most significant mantissa digit.			
.	.			
.	.			
.	.			
14	Second least significant mantissa digit.			
15	Least significant mantissa digit.			

Sm = Sign of mantissa, 0 = positive, 1 = negative.

Se = Sign of exponent, 0 = positive, 1 = negative.

MDC = Mantissa digit count.

DP POS = Decimal point position indicator is a value in the range from 11 down to 12−MDC, which indicates a digit, as given by the DPX column in the table, after which the decimal point is located.

TABLE V. Output Instruction Data Formats

Output Instruction	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUT1	(LSD+1) Digit 1					(LSD) Digit 0		
OUT2	(LSD+3) Digit 3					(LSD+2) Digit 2		
OUT3	(LSD+5) Digit 5					(LSD+4) Digit 4		
OUT4	(LSD+7) Digit 7					(LSD+6) Digit 6		
OUT5	(LSD+9) Digit 9					(LSD+8) Digit 8		
OUT6	(MSD) Digit 11					(MSD−1) Digit 10		
OUTSGN	Sign of Mantissa	0	0	Sign of Exponent		Link/Guard Digit		
OUTEXP	MSD EXPONENT					LSD Exponent		
OUTST	I/P Mode	Round. Mode	Not Used	Angles Mode	x As Fraction	Sign of x	x Comp. to 0	Error Status
OUTIO	IO_3	IO_2	IO_1	IO_0	1	0	0	1
OUTO	O_3	O_2	O_1	O_0	1	1	0	1
OUTR	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
OUTFL	O	F_2	F_1	0	IF_4	IF_3	IF_2	IF_1
OUTMDC	MDC_{MSB}	MDC_{MSB-1}	MDC_{MSB-2}	MDC_{LSB}	1	1	0	0

TABLE VI. Instruction Execution Times

All times are measured with 4 MHz at CKI and are measured from the rising edge of $\overline{WR}$ to the rising edge of INTR/RDY.

Instruction	Worst Case Execution Time (ms)	Instruction		Worst Case Execution Time (ms)
0–9	1.6	TJC	1st Byte	3.0
DP	1.5	a	2nd Byte	1.4
EE	1.5	TX2	1st Byte	3.0
CS		a	2nd Byte	1.4
PI	1.8	TXN	1st Byte	3.0
AIN1 1st Byte	0.3	a	2nd Byte	1.4
2nd Byte	0.9	TXF	1st Byte	3.0
NOP1	1.6	a	2nd Byte	1.4
NOP2	3.1	TERR	1st Byte	3.0
SMDC n	3.1	a	2nd Byte	1.4
IO n	3.1	TMNZ	1st Byte	4.0
O n	3.1	a	2nd Byte	1.4
LDR 1st Byte	3.1	TMZ	1st Byte	4.0
2nd Byte	1.5	a	2nd Byte	1.4
AIN2 1st Byte	3.1	TFI	1st Byte	1.1
2nd Byte	1.5	a	2nd Byte	0.5
OUT1–OUT6	3.0	TFL	1st Byte	1.1
OUTSGN	3.0	a	2nd Byte	0.5
OUTEXP	3.0	IMNZ	1st Byte	3.0
OUTST	3.0	a	2nd Byte	0.5
OUTIO	3.0	DMNZ	1st Byte	4.4
OUTO	3.0	a	2nd Byte	0.5
OUTR	3.0	TIF1–4	1st Byte	3.0
OUTFL	3.0	a	2nd Byte	1.5
OUTMDC	3.0			
OUT 1st Byte	3.0			

TABLE VI. Instruction Execution Times (Continued)

Instruction	Worst Case Execution Time (ms)	Instruction	Worst Case Execution Time (ms)
RAD	2.7	MCLR	5.1
DEG	2.7	EN	5.5
NRND	2.7	ROLL	8.4
RND	2.7	POP	8.6
FLP	2.7	SIN	820
SCI	2.7	COS	830
ECLR	2.7	TAN	540
SIF1–4	2.7	ARCSIN	840
RIF1–4	2.7	ARCCOS	700
ROFF	2.7	ARCTAN	410
RON	2.7	RTD	162
RIO	2.7	DTR	162
SF1	2.7	XXY	2.9
PF1	2.7	EX	440
SF2	2.7	IOX	100
PF2	2.7	SQ	18
Math/Memory Instruction	**Typical Execution Time (ms)**	SQRT	48
		LN	210
XXM	4.2	LOG	140
MS	5.7	1/X	66
MR	7.0	YX	400
M+	13.2	+	20
M−	13.2	−	20
M*	11.8	*	28
M/	60	/	66
CLRM	6.0	LSH	5.2
CLRX	3.0	RSH	2.5

Note 1: Add 0.3 ms to the execution time of any instruction which initiates number entry and is preceded by an enter instruction.

Note 2: Add 2.5 ms to the execution time of any instruction which initiates number entry and is not preceded by an enter instruction.

Note 3: Add 2.0 ms to the execution time of any instruction which terminates number entry mode.

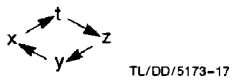
MM57409 Number Cruncher Instruction Set

Mnemonic	Operand	Hex Code	Description
BASIC NUMBER ENTRY INSTRUCTIONS			
0		00	Mantissa or exponent digits. If the previous code was EN (enter), then the digit is placed in x. If the previous code was not EN, the stack is pushed as follows: digit → x x → y y → z z → t
1		01	
2		02	
3		03	
4		04	
5		05	
6		06	
7		07	
8		08	
9		09	See Number Entry Mode Description
DP		0A	Decimal point. Digits that follow will be mantissa fraction.
EE		0B	Enter exponent. Digits that follow will be exponent digits. If this is the first data entry, a "1" will be loaded into the mantissa.
CS		0C	Change sign. The mantissa's sign is changed unless EE was the last number entry initiation, in which case the exponent's sign is changed.
PI		0D	3.14159265359 → x.
AIN1		0E	Single digit asynchronous input. See Number Entry Mode Description.
NOP1		0F	No operation.
NOP2		22	Terminate number entry, no other operation.

MM57409 Number Cruncher Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Description
MANTISSA DIGIT COUNT (MDC) CONTROL INSTRUCTIONS			
SMDC	n	7(n−1)	Set the MDC = n.n = 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C hex
I/O, O, AND PC PORT WRITE INSTRUCTIONS			
IO	n	A(n)	Write n to the 4-bit general I/O port. n = 0 through F hex.
O	n	B(n)	Write n to the 4-bit general O port. n = 0 through F hex.
LDR	a	92 a	Load the R port with "a", where "a", is 8-bit value from 00 hex through FF hex.
DATA INPUT INSTRUCTIONS			
AIN2		91	Asynchronous input 2. See Data Input Description.
DATA OUTPUT INSTRUCTIONS			
OUT1		80	Output x mantissa LSD and LSD + 1.
OUT2		81	Output x mantissa LSD + 2 and LSD + 3.
OUT3		82	Output x mantissa LSD + 4 and LSD + 5.
OUT4		83	Output x mantissa LSD + 6 and LSD + 7.
OUT5		84	Output x mantissa LSD + 8 and LSD + 9.
OUT6		85	Output x mantissa MSD − 1 and MSD.
OUTSGN		86	Output link/guard digit and mantissa/exponent sign digit.
OUTEXP		87	Output x exponent digit.
OUTST		88	Output 8-bit status register.
OUTIO		89	Output the state of the 4-bit general I/O port.
OUTO		8D	Output the state of the 4-bit general outut port.
OUTR		8A	Output the state of the 8-bit R port.
OUTFI		8B	Output F1, F2, and the four internal flags, IF1 through IF4.
OUTMDC		8C	Output the Mantissa Digit Count.
OUT		8F	Multiple digit output instruction. See Data Output Description.
TEST/CONDITIONAL OUTPUT INSTRUCTIONS			
TCI	a	10 a	If external test input CI = logic "1", load R with "a", where "a" is an 8-bit value from 00 hex through FF hex.
TXZ	a	11	If x = 0, load R with "a".
TXN	a	12 a	If x is negative, load R with "a".
TXF	a	13 a	If the absolute value of x is a fraction, load R with "a".
TERR	a	14	If the error flag is set, load R with "a".
TMNZ	a	16 a	If memory is not equal to 0, load R with "a".
TMZ	a	17 a	If memory equals 0, load R with "a".
TF1	a	18 a	If the external flag input 1 = logic "1", load R with "a".
TF2	a	1B a	If the external flag input 2 = logic "1", load R with "a".
IMNZ	a	19 a	Increment the mantissa contained in memory, and if the new value of the memory is not = 0, load R with "a".
DMNZ	a	1A a	Decrement the mantissa contained in memory, and if the new value of the memory is not = 0, load R with "a".
TIF	n, a	1(B + n) a	If the internal flag n = logic "1", load R with "a". n = 1,2,3,4.

MM57409 Number Cruncher Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Description
MATH INSTRUCTIONS			
CLRX		20	0 → x.
MCLR		2F	Master clear: clear all internal registers and outputs; 10 → MDC. Scientific notation mode; round to MDC on output; R port set to 03 hex and is enabled; I/O port unaffected.
EN		21	Enter and push stack. The same digit will be in x and y.
ROLL		23	Roll stack:  TL/DD/5173–17
POP		2E	Pop the stack: y → x z → y t → z 0 → t
SIN		24	sin(x) → x
COS		25	cos(x) → x
TAN		26	tan(x) → x
ARCSIN		27	arcsin(x) → x
ARCCOS		28	arccos(x) → x
ARCTAN		29	arctan(x) → x
RTD		2C	Convert the value in x from radians to degrees.
DTR		2D	Convert the value in x from degrees to radians.
XXY		30	Exchange x and y.
EX		31	e^x → x
10X		32	10^x → x
SQ		33	x^2 → x
SQRT		34	Square root(x) → x
LN		35	ln x → x
LOG		36	Log x → x
1/X		37	1/x → x
YX		38	y^x → x; 0 → t, t → z, z → y
+		39	y + x → x; 0 → t, t → z, z → y
—		3A	y − x → x; 0 → t, t → z, z → y
*		3B	y*x → x; 0 → t, t → z, z → y
/		3C	y/x → x; 0 → t, t → z, z → y
LSH		3E	Left shift x mantissa, DP unchanged, MSD in guard/link digit.
RSH		3F	Right shift x mantissa, DP unchanged, link/guard digit → MSD.
MEMORY INSTRUCTIONS			
XXM		40	Exchange x and memory.
MS		41	Store x in memory.
MR		42	Memory → x → y → z → t.
M+		43	Memory + x → memory.
M−		44	Memory − x → memory.
M*		45	Memory*x → memory.
M/		46	Memory divided by x → memory.
CLRM		47	Clear memory; 0 → memory.

MM57409 Number Cruncher Instruction Set (Continued)

Mnemonic	Operand	Hex Code	Description
MODE AND FLAG INSTRUCTIONS			
RAD		50	Set radian angular mode.
DEG		51	Set degrees angular mode.
NRND		54	Round to MDC on output disabled.
RND		55	Round to MDC on output enabled.
FLP		56	Set floating-point I/O mode.
SCI		57	Set scientific notation I/O mode.
ECLR		2B	Clear error flag.
SIF1		58	Set internal flag 1.
SIF2		5A	Set internal flag 2.
SIF3		5C	Set internal flag 3.
SIF4		5E	Set internal flag 4.
RIF1		59	Reset internal flag 1.
RIF2		5B	Reset internal flag 2.
RIF3		5D	Reset internal flag 3.
RIF4		5F	Reset internal flag 4.
OUTPUT CONTROL INSTRUCTIONS			
ROFF		60	TRI-STATE the R port.
RON		61	Enable the R port.
RIO		52	R port is enabled as high-impedance I/O.
SF1		67	Set external flag 1 high.
PF1		68	Pulse external flag 1 high. If F1 is already high, then it is reset.
SF2		69	Set external flag 2 high.
PF2		6A	Pulse external flag 2 high. If F2 is already high, then it is reset.