



MMC 4020 MMC 4024 MMC 4040

RIPPLE-CARRY BINARY COUNTER/DIVIDERS:

4020 - 14 STAGE
4024 - 7 STAGE
4040 - 12 STAGE

GENERAL DESCRIPTION

These devices are monolithic I.C's fabricated with standard AL-gate CMOS technology. All counter stages are master-slave flip-flops.

The state of a counter advances one count on the negative transition of each input pulse. A high level on the RESET line resets the counter to its all zeros stage. Schmitt trigger action on the input-pulse line permits unlimited clock rise and fall times. All inputs and outputs are buffered. MMC 4020, MMC 4040 are available in 16-lead dual-in-line ceramic or plastic package and MMC 4024 is available in 14-lead dual-in-line plastic or ceramic package.

FEATURES

- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- Common RESET
- Quiescent current specified to 20 V
- Standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: G and H types E and F types	-0.5 to 20	V
V_i	Input voltage	-0.5 to 18	V
I_i	DC input current (any one input)	-0.5 to $V_{DD}+0.5$	V
P_{tot}	Total power dissipation (per package)	± 10	mA
	Dissipation per output transistor for T_A = full package-temperature range	200	mW
T_A	Operating temperature: G and H types E and F types	-55 to 125	°C
T_{stg}	Storage temperature	-40 to 85	°C
		-65 to 150	°C

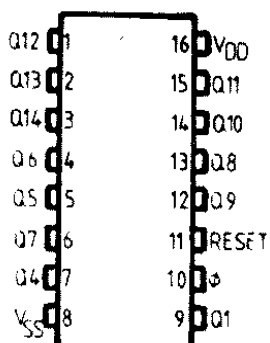
* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

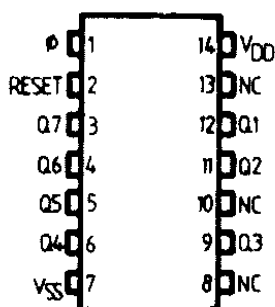
V_{DD}^*	Supply voltage: G and H types E and F types	3 to 18	V
V_i	Input voltage	3 to 15	V
T_A	Operating temperature: G and H types E and F types	0 to V_{DD}	V
		-55 to 125	°C
		-40 to 85	°C

CONNECTION DIAGRAM

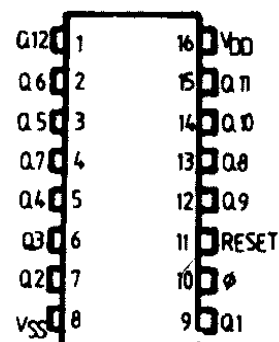
MMC 4020



MMC 4024

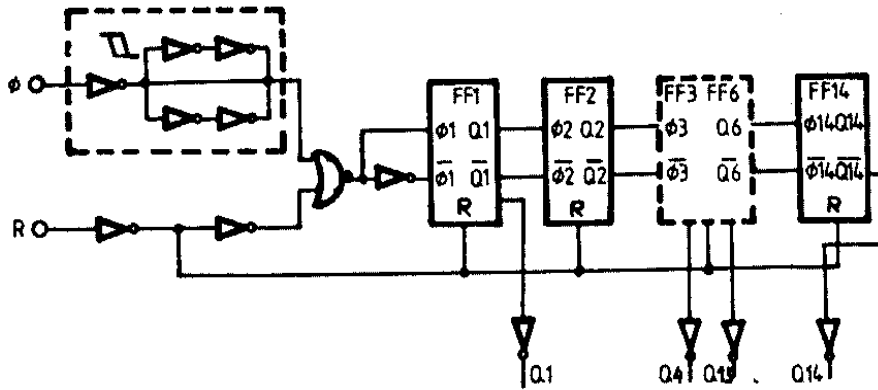


MMC 4040

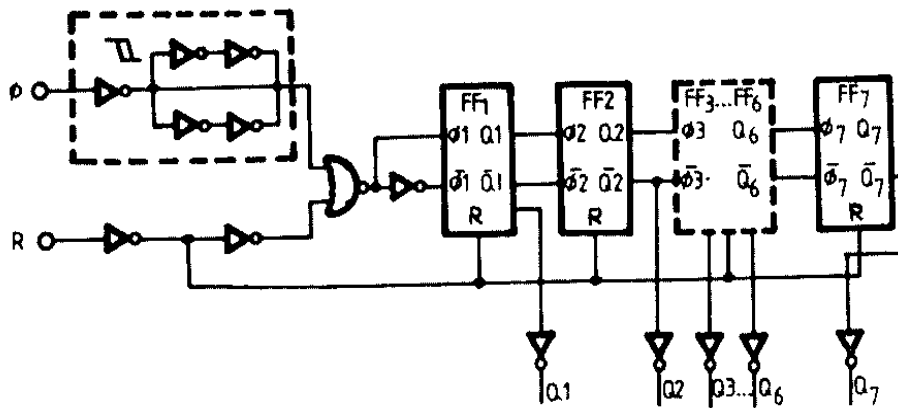


LOGIC DIAGRAM

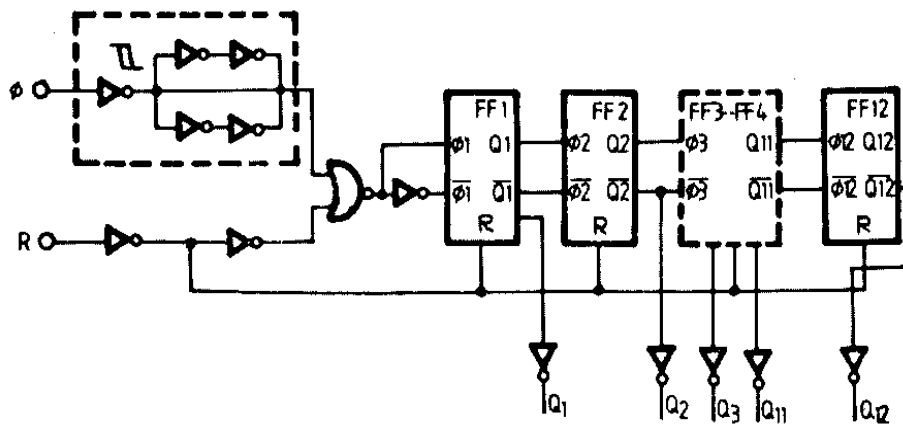
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STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT		
		V _I (V)	V _O (V)	I _{IQ} (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}			
						min.	max.	min.	typ.	max.	min.		max.	
I _L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
	E, F types	0/ 5			5		20		0.04	20		150		
		0/10			10		40		0.04	40		300		
		0/15			15		80		0.04	80		600		
V _{OH}	Output high voltage			< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL}	Output low voltage			< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH}	Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL}	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9			
		0/15	13.5		15	-3.6		-3.0	-6.8		-2.4			
I _{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} / I _{IL}	Input leakage current	G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
		E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C _I	Input capacitance		Any input							5	7.5		pF	

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V2 V min. with V_{DD} = 10 V2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_i = 200\text{ kohm}$, typical temperature coefficient for all $V_{DD} = 0.3\%/^\circ\text{C}$ values, all input rise and fall time = 20 ns)

PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES			UNIT
		min.	typ.	max.	
Input pulse operation					
t_{PLH} Propagation delay time (Φ to Q1 Out)	5		180	360	ns
t_{PHL}	10		80	160	
	15		65	130	
t_{PLH} Propagation delay time Q_n to Q_{n+1}	5		100	200	ns
t_{PHL}	10		40	80	
	15		30	60	
t_{TLH} Transition time	5		100	200	ns
t_{THL}	10		50	100	
	15		40	80	
t_W Minimum input pulse width	5		70	140	ns
	10		30	60	
	15		20	40	
t_r, t_f Input rise and fall time	5	Unlimited			μs
	10				
	15				
f_{max} Maximum input clock frequency	5	3.5	7		MHz
	10	8	16		
	15	12	24		

Reset operation

t_{PHL} Propagation delay time	5		140	280	ns
	10		60	120	
	15		50	100	
t_W Minimum reset pulse width	5		100	200	ns
	10		40	80	
	15		30	60	
t_{rem} Reset removal time	5		175	350	ns
	10		75	150	
	15		50	100	

Detail of flip-flop stage

