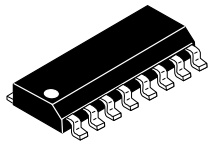
The MRFIC Line
900 MHz Driver and Ramp

MRFIC2004

900 MHz DRIVER & RAMP SILICON MONOLITHIC INTEGRATED CIRCUIT

The MRFIC2004 is an integrated Driver and Ramp designed for transmitters operating in the 800 MHz to 1.0 GHz frequency range. The Ramp is an integrator which can be used for burst control for TDD/TDMA systems. The Driver uses a cascode configuration for high gain and reverse isolation. A power down control is provided to minimize current drain with minimum recovery/turn-on time. Also, an on-board inverter is included to provide complementary control for an antenna switch, such as the MRFIC2003. The design utilizes Motorola's advanced MOSAIC 3 silicon bipolar RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC2004 include CT1 and CT2 cordless telephones, GSM, remote controls, video and audio short range links, low cost cellular radios, and ISM band transmitters.

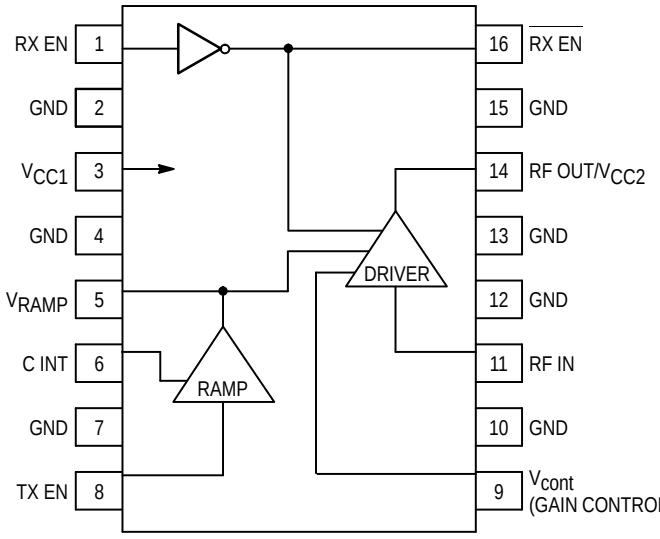
- Small Signal Gain = 21.5 dB (Typ)
- Small Signal Gain Control = 34 dB (Typ)
- $P_{o\ 1.0\ dB}$ = –1.0 dBm (Typ)
- On Board Ramp for Burst Control
- Power Down Supply Current = 0.7 mA (Typ)
- Low Operating Supply Voltage (2.7 to 4.0 Volts)
- Input/Output VSWR Insensitive to Gain Control
- Order MRFIC2004R2 for Tape and Reel.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2004



CASE 751B-05
(SO-16)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC1} V_{CC2}	4.5 6.0	Vdc
Control Voltages	RXEN, TXEN, V_{cont}	6.0	Vdc
Input Power, RF IN Port	P_{RF}	+10	dBm
Operating Ambient Temperature	T_A	–35 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C



Pin Connections and Functional Block Diagram

REV 2

MOTOROLA

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage Ranges	V_{CC1}, V_{CC2}	2.7 to 4.0	Vdc
Control Voltage Ranges	TX EN, RX EN, V_{cont}	0 to V_{CC1}	Vdc
Frequency Range	f	800 to 1000	MHz

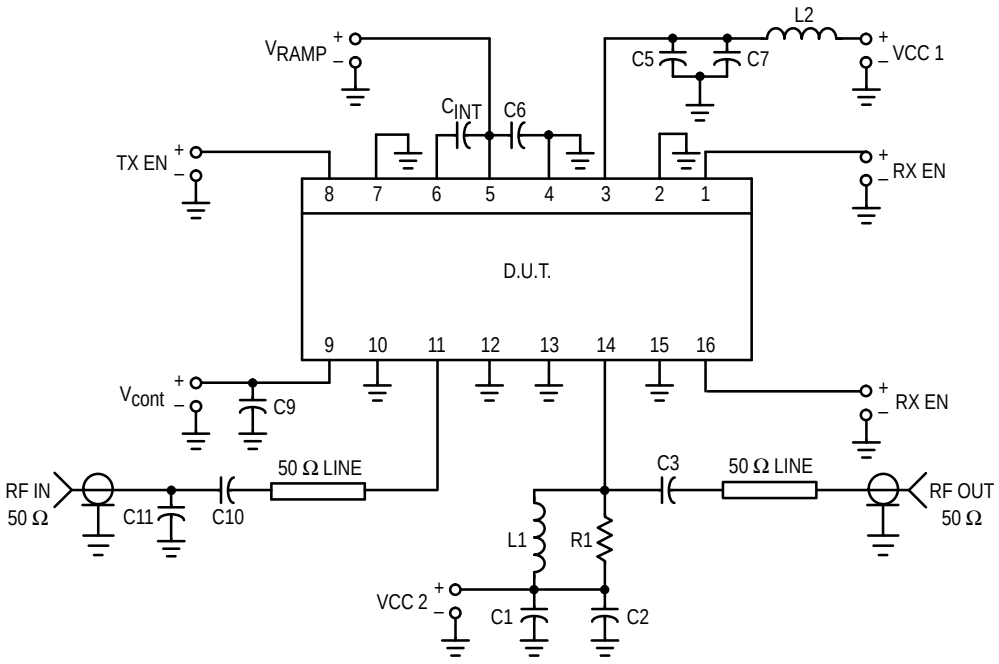
ELECTRICAL CHARACTERISTICS (V_{CC1}, V_{CC2} = 3.0 V, C_{INT} = 2.0 nF, T_A = 25°C, f = 900 MHz, V_{CONT} = 1.3 V)

Characteristics (1)	Min	Typ	Max	Unit
Supply Current, TX EN High, RX EN Low	—	11	13	mA
Supply Current, TX EN Low, RX EN High	—	0.7	1.5	mA
Driver Characteristics (1)				
Gain (Small Signal)	19	21.5	24	dB
Gain Control (Small Signal)	—	34	—	dB
Power Out @ 1.0 dB Gain Compression	–4.0	–1.0	—	dBm
Third Order Intercept Point (out)	—	+7.5	—	dBm
Reverse Isolation	—	32	—	dB
Ramp Characteristics (1)				
Ramp Up Delay Time Rise Time Total Time	— — —	4.0 18 22	— — —	µs
Ramp Down Delay Time Fall Time Total Time	— — —	4.0 18 22	— — —	µs

LOGIC LEVELS (V_{CC1} = 2.7 to 4.0 V, T_A = 25°C)

RX EN & TX EN Input Voltage	Min	Typ	Max	Unit
High Low	V_{CC1} – 0.8 —	— —	— 0.8	V
$\overline{\text{RX EN}}$ Output Voltage				
High Low	V_{CC1} – 0.2 —	— —	— 0.2	V

NOTE:
1. All electrical characteristics measured in test circuit schematic shown in Figure 1 below.



C1, C7, C9 — 1000 pF Chip Capacitor
C2, C5, C6, C10 — 100 pF Chip Capacitor
C3 — 1.6 pF Chip Capacitor
C_{INT} — 2000 pF Chip Capacitor
C11 — 6.2 pF Chip Capacitor
L1 — 4.7 nH Chip Inductor
L2 — 150 nH Chip Inductor
R1 — 330 Ω Chip Resistor
RF Connectors — SMA Type
Board Material — Epoxy/Glass ε_r = 4.5,
Dielectric Thickness = 0.014″ (0.36 mm)

Figure 1. Typical Biasing Configuration

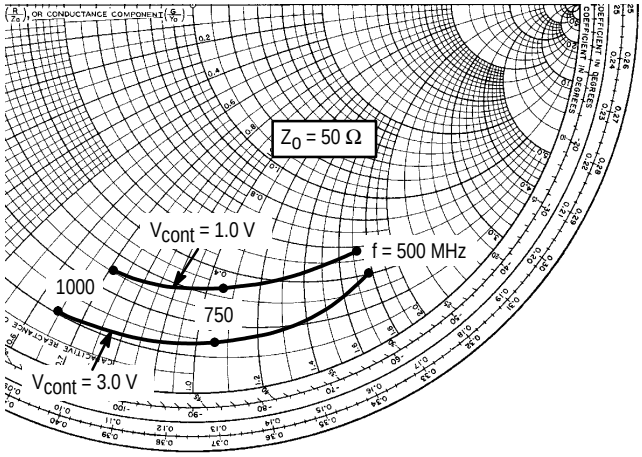


Figure 2. S_{11} versus Frequency versus V_{cont}

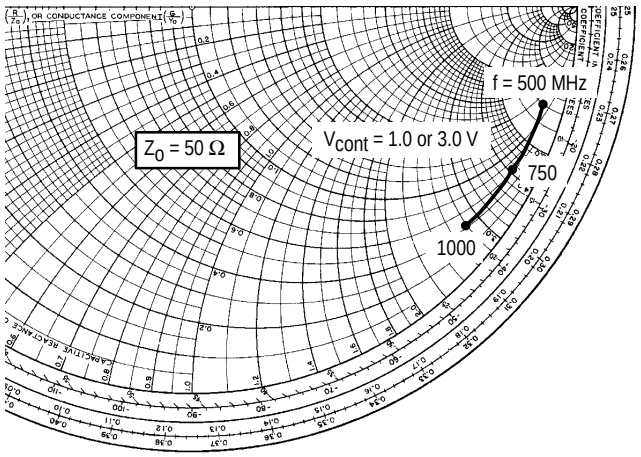


Figure 3. S_{22} versus Frequency

V_{cont}	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
		$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
1.0	100	0.85	−11.3	10.48	171.5	0.0002	142.7	0.99	−2.9
	300	0.83	−32.8	10.33	156.3	0.0020	129.0	0.99	−7.3
	500	0.79	−56.9	10.15	140.5	0.0030	130.6	0.98	−15.9
	550	0.79	−62.5	10.04	135.9	0.0030	132.6	0.98	−17.9
	600	0.78	−68.5	9.85	130.2	0.0040	133.3	0.98	−20.0
	650	0.77	−74	9.47	126.9	0.0040	135.9	0.98	−22.3
	700	0.76	−79	9.23	123.6	0.0050	137.2	0.98	−24.7
	750	0.76	−84.4	9.02	119.4	0.0050	138.1	0.97	−27.0
	800	0.75	−89.6	8.69	113.8	0.0060	139.7	0.97	−29.3
	850	0.74	−94.5	8.33	110.8	0.0070	140.3	0.97	−31.4
	900	0.73	−99.1	8.13	108.9	0.0080	141.2	0.96	−33.2
	950	0.73	−102	7.98	105.4	0.0090	138.3	0.96	−36.3

	1000	0.72	−106.9	7.70	101.0	0.0100	133.7	0.95	−38.4
1.9	100	0.85	−11.3	0.53	−173.5	0.0002	104.3	0.99	−2.9
	300	0.86	−33.5	0.69	−169.7	0.0009	118.7	0.98	−8.7
	500	0.87	−59.3	0.89	−179.5	0.0010	134.3	0.98	−15.5
	550	0.87	−65.7	0.96	175.1	0.0020	136.3	0.98	−17.5
	600	0.88	−73.1	1.02	169.9	0.0020	138.9	0.97	−19.6
	650	0.88	−78.7	1.04	167.3	0.0020	142.6	0.97	−21.8
	700	0.88	−84.7	1.07	165.0	0.0030	147.8	0.97	−24.1
	750	0.89	−90.7	1.14	161.5	0.0030	153.4	0.96	−26.4
	800	0.89	−98.2	1.17	155.8	0.0040	161.0	0.96	−28.8
	850	0.88	−104.6	1.22	151.2	0.0050	161.8	0.96	−30.7
	900	0.87	−110.1	1.24	144.6	0.0060	162.7	0.95	32.8
	950	0.86	−114.6	1.26	139.9	0.0070	160.3	0.95	−35.1
	1000	0.85	−118.8	1.27	134.1	0.0080	158.2	0.94	−37.2
3.0	100	0.85	−10.9	0.003	−85.9	0.0001	115.0	0.99	−2.8
	300	0.86	−31.9	0.014	−78.8	0.0006	121.0	0.99	−8.5
	500	0.87	−56.9	0.032	−61.1	0.0010	128.0	0.98	−15.1
	550	0.88	−62.4	0.038	−65.8	0.0010	136.2	0.98	−17.0
	600	0.89	−69.4	0.048	−68.3	0.0010	140.0	0.98	−19.2
	650	0.90	−75.1	0.058	−75.1	0.0020	145.1	0.98	−21.3
	700	0.90	−81.3	0.069	−82.4	0.0020	150.8	0.97	−23.6
	750	0.91	−87.3	0.081	−89.4	0.0020	156.8	0.97	−25.8
	800	0.91	−93.8	0.092	−113.4	0.0030	160.3	0.97	−28.1
	850	0.92	−100.7	0.092	−121.8	0.0040	163.3	0.96	−30.1
	900	0.91	−106.8	0.089	−128.2	0.0050	163.3	0.96	−32.3
	950	0.90	−111.4	0.083	−137.1	0.0060	155.2	0.95	−34.5
	1000	0.89	−115.2	0.077	−151.9	0.0060	150.0	0.95	−36.6

Table 1. Small Signal Deembedded S Parameters

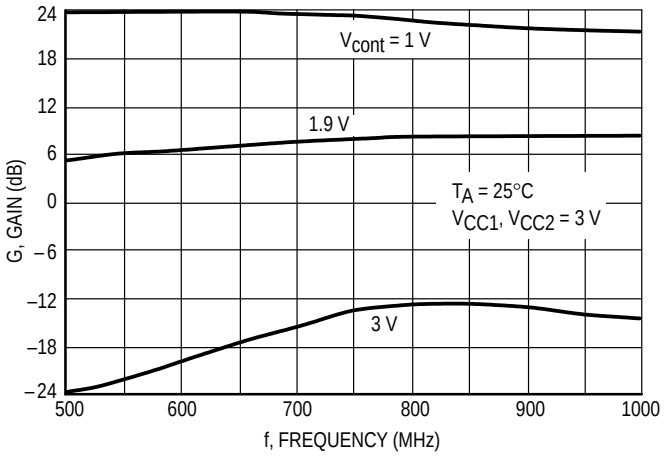


Figure 4. Small Signal Gain versus Frequency

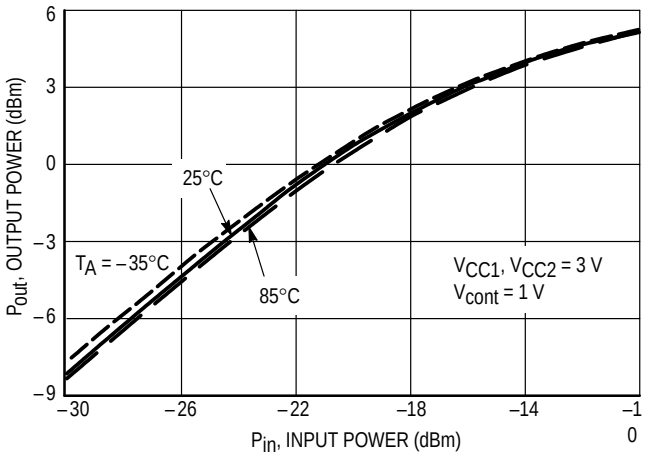


Figure 5. Output Power versus Input Power

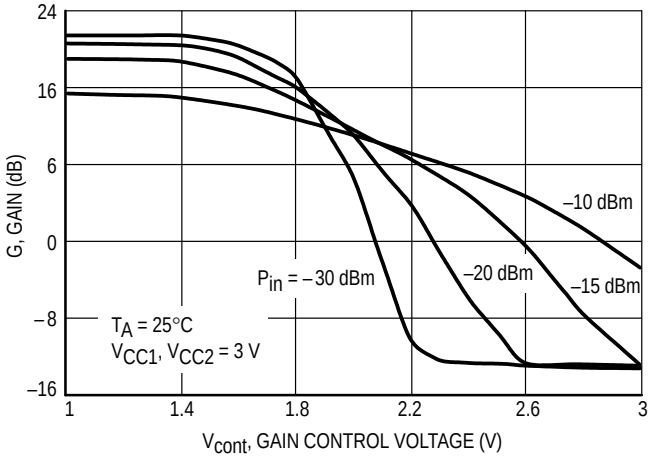


Figure 6. Driver Gain versus Gain Control Voltage

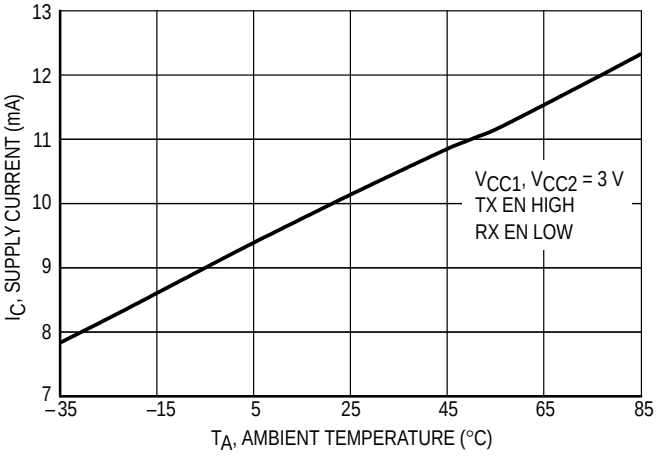


Figure 7. Supply Current versus Ambient Temperature

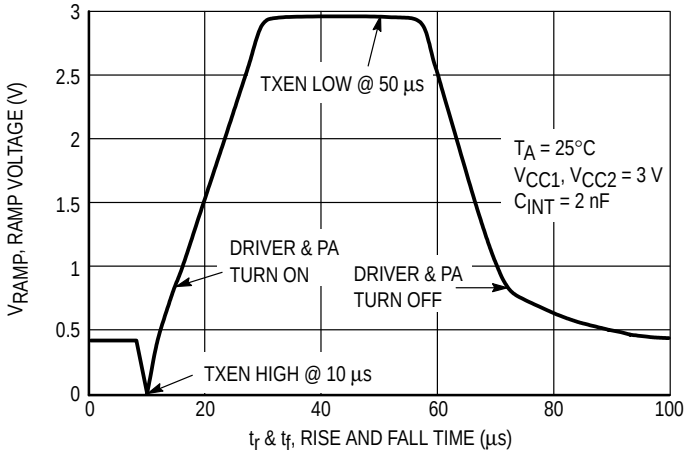


Figure 8. Ramp Voltage versus Rise & Fall Time

APPLICATIONS INFORMATION

DESIGN PHILOSOPHY

The MRFIC2004 was designed as a support IC for a CT2 chip-set. The other chips making up the chip-set are the MRFIC2001 downconverter, the MRFIC2002 transmit mixer, the MRFIC2003 antenna switch and the MRFIC2006 PA. A complete CT2 front-end solution requires a ramp for burst control, an inverter for complementary antenna switch control and gain control (or an attenuator) for the transmitter low power mode. In order to keep the other chips in the chip-set relatively general purpose, yet provide the system designer with an easily controlled solution, these functions were combined with a driver amplifier into one IC, the MRFIC2004.

THEORY OF OPERATION

The driver is a cascode design that exits the IC open-collector. Impedance matching must be done externally. Since the output requires a bias inductor and DC blocking capacitor, the output can be matched with these two elements. To keep the driver unconditionally stable, it is recommended that a 300–400 ohm resistor be placed in parallel with the bias inductor as close to the IC as possible. Since the output impedance of the driver by itself is very high, the resistor sets the output impedance. The input can be matched with a series inductor followed by a shunt capacitor. Alternatively, a series transmission line followed by a shunt capacitor can be used. A DC block is also required on the input.

Gain control is provided to meet the CT2 low power mode requirement. The CT2 Common Air Interface specification requires the transmitter to be capable of dropping the output power by 16 ± 4.0 dB. Although the driver has 34 dB of small signal gain control, it can be reduced by adding a resistor in series with the gain control pin. The value of the resistor depends on the logic levels being used and the amount of gain compression after the driver. Also, the amount of gain control is a function of the driver input power level. The input power should be kept less than –10 dBm to allow for sufficient gain control to achieve the low power mode. The gain control can also be used for PA output power trimming. However, this is not an efficient method.

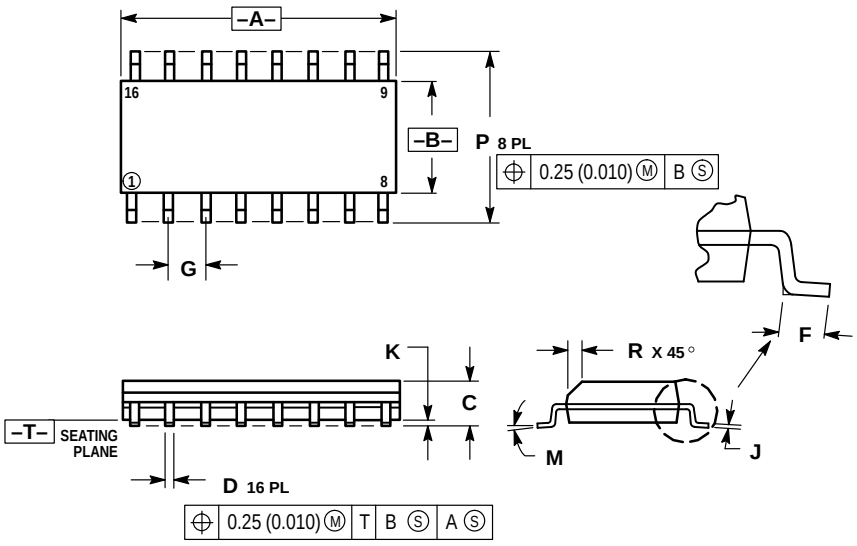
The ramp is an integrator which is used to slow down the driver and PA turn-on and turn-off times to reduce AM splatter. By applying a pulse waveform to the input, a linear ramp waveform is created at the output which is then applied to the current mirrors of the driver and PA. An external integrating capacitor is used so that the rise/fall time can be programmed externally. A minimum value of 2.0–2.4 nF is needed to meet the CT2 Common Air Interface splatter specification. For non-TDD/TDMA systems the ramp reverts to an enable/disable function.

The inverter is CMOS/TTL compatible and was included to provide complementary control for an antenna switch such as the MRFIC2003. By applying the receiver enable control line, RXEN, to the inverter the inverse RXEN will be created. RXEN and RXEN can then be used to control the MRFIC2003 antenna switch.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B–05
ISSUE J

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