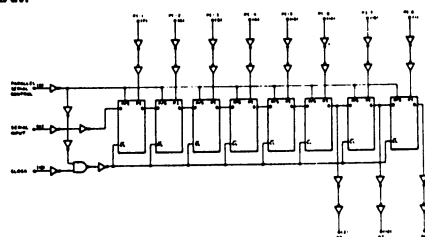
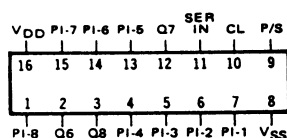


SCL4021B

EIGHT STAGE STATIC SHIFT REGISTER

LOGIC DIAGRAM

**STATIC CHARACTERISTICS: ($V_{SS} = 0\text{ V}$)**

PARAMETER	CONDITIONS	V_{DD} (Vdc)	T_{LOW}^* MIN	T_{LOW}^* MAX	+25°C TYP	MAX	T_{HIGH}^{**} MIN	T_{HIGH}^{**} MAX	UNIT
QUIESCENT DEVICE CURRENT I_{DD}	$V_{IN} = V_{SS}$ OR V_{DD}	5		5	0.05	5		150	μA_{dc}
		10		10	0.1	10		300	
		15		20	0.2	20		600	

Note: * $T_{LOW} = -55^\circ\text{C}$ for C / H devices, -40°C for E / S devices, ** $T_{HIGH} = +125^\circ\text{C}$ for C / H devices, $+85^\circ\text{C}$ for E / S devices.

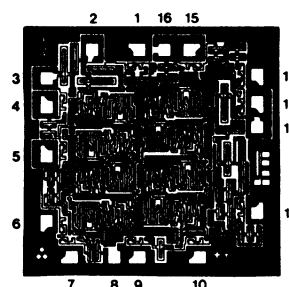
DYNAMIC CHARACTERISTICS: ($C_L = 50\text{pF}$, $T_A = 25^\circ\text{C}$)

PARAMETER	V_{DD} (Vdc)	MINIMUM	TYPICAL	MAXIMUM	UNIT
PROPAGATION DELAY TIME t_{PLH} , t_{PHL} (FROM CLOCK OR P/S OUTPUT)	5		180		ns
	10		90		
	15		75		
OUTPUT TRANSITION TIME t_{TLH} , t_{THL}	5		100		ns
	10		50		
	15		40		
CLOCK PULSE WIDTH MINIMUM PW_{CL}	5		90		ns
	10		40		
	15		25		
CLOCK FREQUENCY MAXIMUM f_{CL}	5	3	5		MHz
	10	6	12		
	15	8	16		
CLOCK RISE & FALL TIME MAXIMUM t_{rCL} t_{fCL}	5	15			μs
	10	15			
	15	15			
P/S PULSE WIDTH MINIMUM PW	5		80	160	ns
	10		40	80	
	15		25	50	
SETUP TIME MINIMUM t_{set} (PARALLEL OR SERIAL INPUTS)	5		60	120	ns
	10		40	80	
	15		30	60	
HOLD TIME MINIMUM t_{hold} (PARALLEL OR SERIAL INPUTS)	5		100	200	ns
	10		30	60	
	15		20	40	
P/S REMOVAL TIME t_{rem}	5		140	280	ns
	10		70	140	
	15		50	100	

DIE DRAWING

SCL4021B

80 x 77 mils



Note: Refer to "SCL4000B SERIES FAMILY SPECIFICATIONS" for remaining Dynamic and Static Characteristics, and, for recommended and maximum operating conditions.