

SN55LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SGLS084B – MARCH 1995 – REVISED SEPTEMBER 1999

- Meets Standard EIA-485
- Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments
- Supports Data Rates up to and Exceeding Ten Million Transfers Per Second
- Common-Mode Output Voltage Range of -7 V to 12 V
- Positive- and Negative-Current Limiting
- Low Power Consumption . . . 1.5 mA Max (Output Disabled)

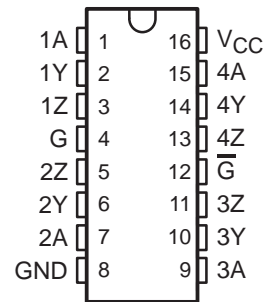
description

The SN55LBC172 is a monolithic quadruple differential line driver with 3-state outputs. This device is designed to meet the requirements of the Electronics Industry Association (EIA) standard RS-485. The SN55LBC172 is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry, making it suitable for party-line applications in noisy environments. The device is designed using the LinBiCMOS™ process, facilitating ultralow power consumption and inherent robustness.

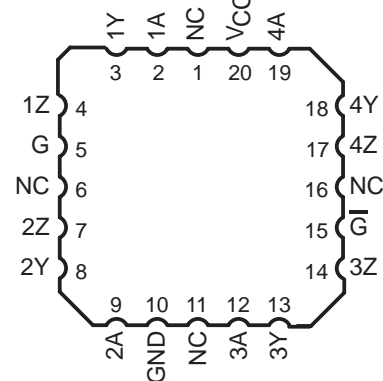
The SN55LBC172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. This device offers optimum performance when used with the SN55LBC173M quadruple line receiver. The SN55LBC172 is available in the 16-pin CDIP package (J), the 16-pin CPAK package (W), or the 20-pin LCCC package (FK).

The SN55LBC172 is characterized for operation over a military temperature range of -55°C to 125°C .

**J OR W PACKAGE
(TOP VIEW)**



**FK PACKAGE
(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE
(each driver)**

INPUT A	ENABLES		OUTPUTS	
	G	\bar{G}	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)



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**TEXAS
INSTRUMENTS**

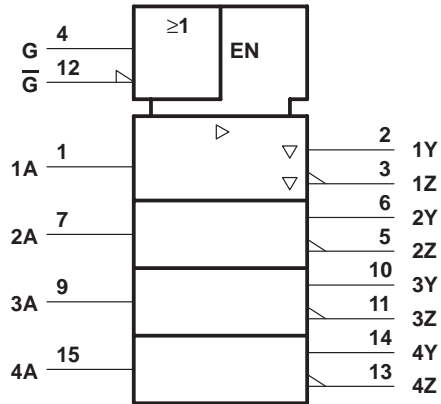
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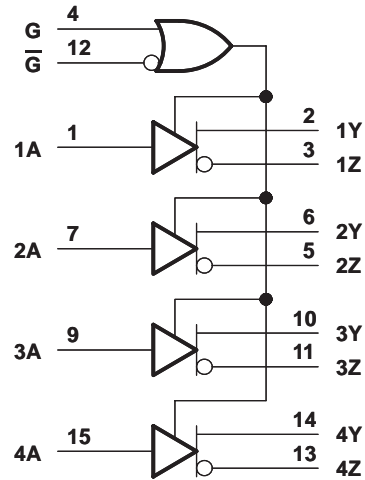
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logic symbol†



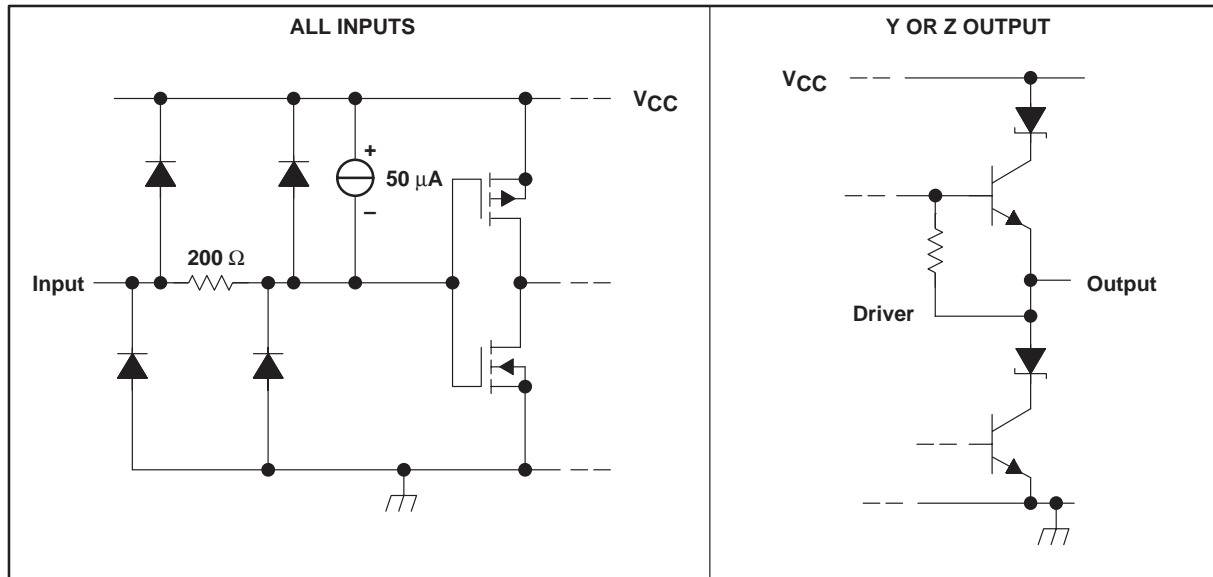
logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J or W package.

schematic diagrams of inputs and outputs



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Output voltage range, V_O	–10 V to 15 V
Input voltage range, V_I	–0.3 V to 7 V
Continuous power dissipation	Internally limited‡
Operating free-air temperature range, T_A	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A=125^\circ\text{C}$	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Output voltage at any bus terminal (separately or common mode), V_O	Y or Z			12	V
				–7	
High-level output current, I_{OH}	Y or Z			–60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A		–55		125	°C



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = -18 mA			-1.5	V
V _{OD}	Differential output voltage‡	R _L = 54 Ω, See Figure 1	1.1	1.8	5	V
		R _L = 60 Ω, See Figure 2	1.1	1.7	5	
Δ V _{OD}	Change in magnitude of differential output voltage§				±0.2	V
V _{OC}	Common-mode output voltage	R _L = 54 Ω, See Figure 1			3 -1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage§					±0.2
I _O	Output current with power off	V _{CC} = 0, V _O = -7 V to 12 V			±100	μA
I _{OZ}	High-impedance-state output current	V _O = -7 V to 12 V			±100	μA
I _{IH}	High-level input current	V _I = 2.4 V			-100	μA
I _{IL}	Low-level input current	V _I = 0.4 V			-100	μA
I _{OS}	Short-circuit output current	V _O = -7 V to 12 V			±250	mA
I _{CC}	Supply current (all drivers)	No load	Outputs enabled		7	mA
			Outputs disabled		1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.

§ Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	T _A		MIN	TYP	MAX	UNIT
t _{d(OD)}	Differential output delay time	R _L = 54 Ω, See Figure 3	25°C		2	11	20	ns
			-55°C to 125°C		2		40	
t _{t(OD)}	Differential output transition time	R _L = 54 Ω, See Figure 3	25°C		10	15	25	ns
			-55°C to 125°C		4		60	
t _{pZH}	Output enable time to high level	R _L = 110 Ω, See Figure 4	25°C				30	ns
			-55°C to 125°C				40	
t _{pZL}	Output enable time to low level	R _L = 110 Ω, See Figure 5	25°C				30	ns
			-55°C to 125°C				40	
t _{pHZ}	Output disable time from high level	R _L = 110 Ω, See Figure 4	25°C				60	ns
			-55°C to 125°C				115	
t _{pLZ}	Output disable time from low level	R _L = 110 Ω, See Figure 5	25°C				30	ns
			-55°C to 125°C				55	



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PARAMETER MEASUREMENT INFORMATION

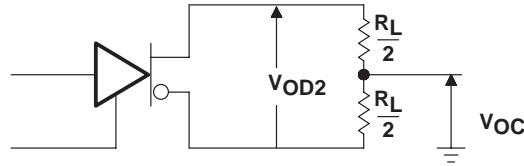


Figure 1. Differential and Common-Mode Output Voltages

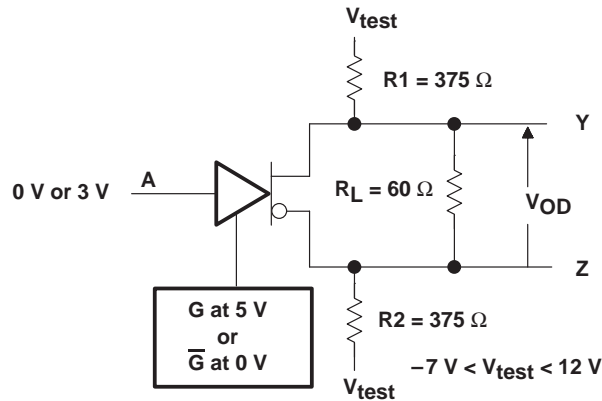
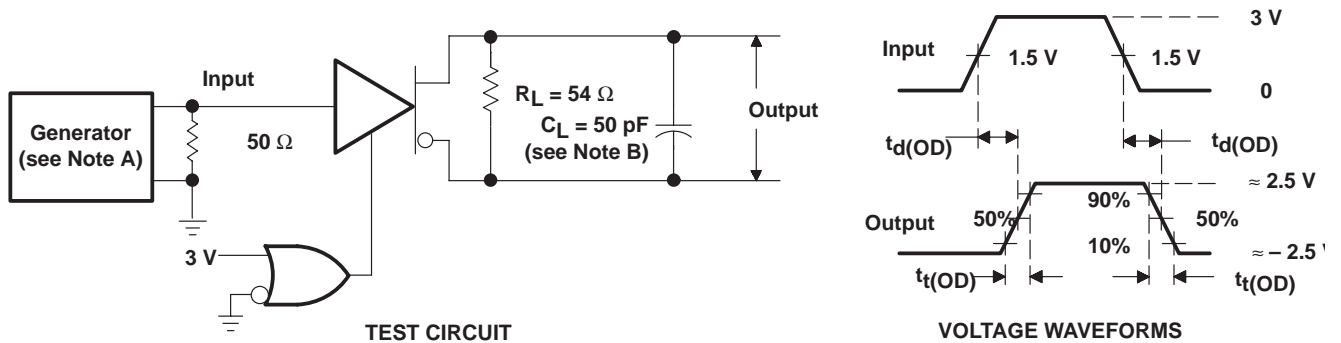


Figure 2. Driver V_{OD} Test Circuit



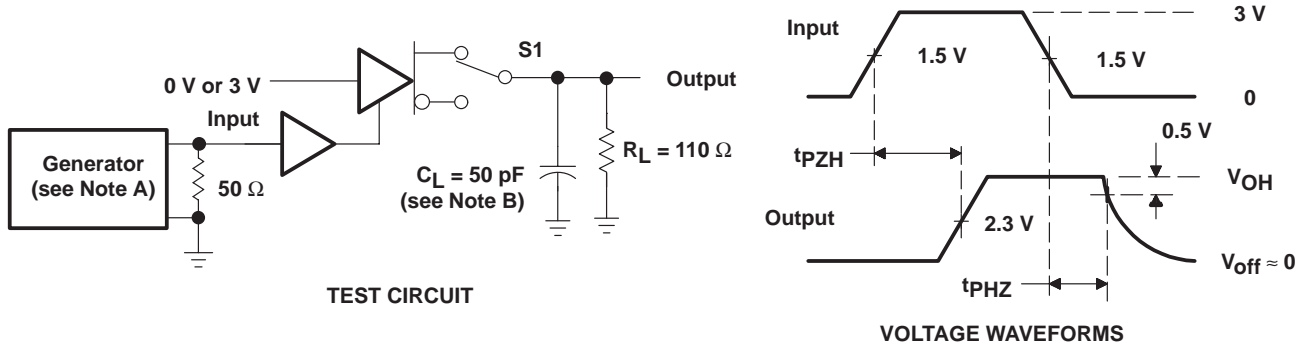
- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle $\leq 50\%$, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and stray capacitance.

Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

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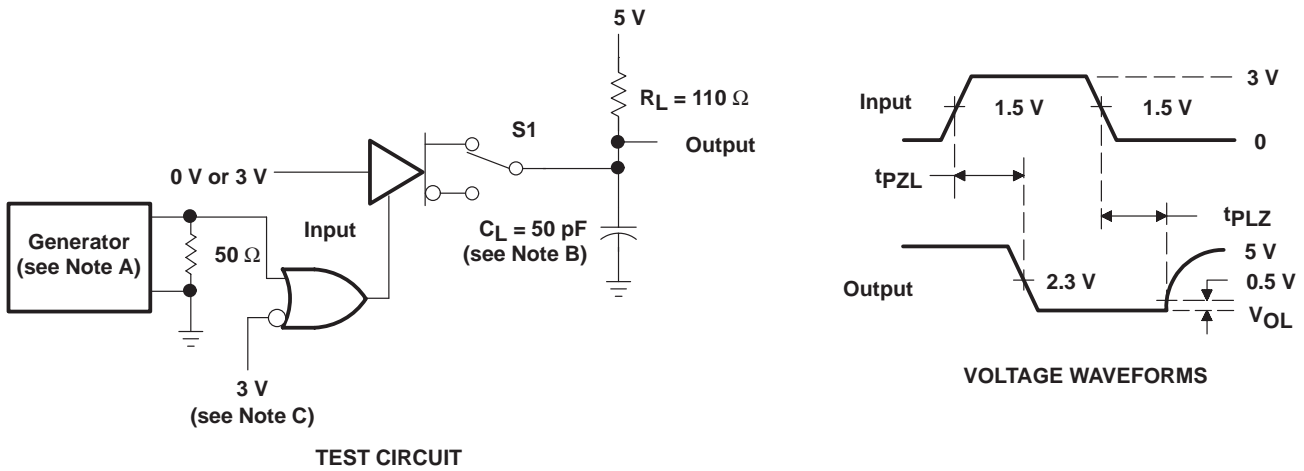
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.

Figure 4. t_{pZH} and t_{pHZ} Test Circuit and Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and stray capacitance.
 C. To test the active-low enable \overline{G} , ground G and apply an inverted waveform to \overline{G} .

Figure 5. t_{pZL} and t_{pLZ} Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

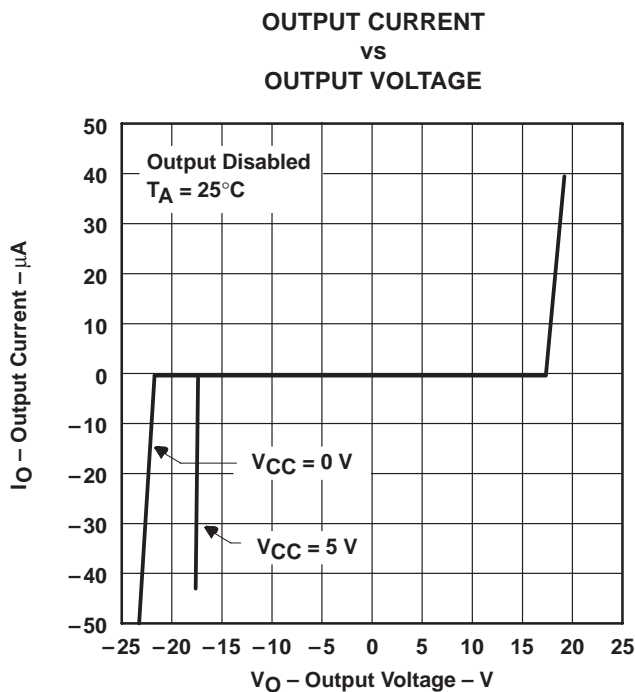


Figure 6

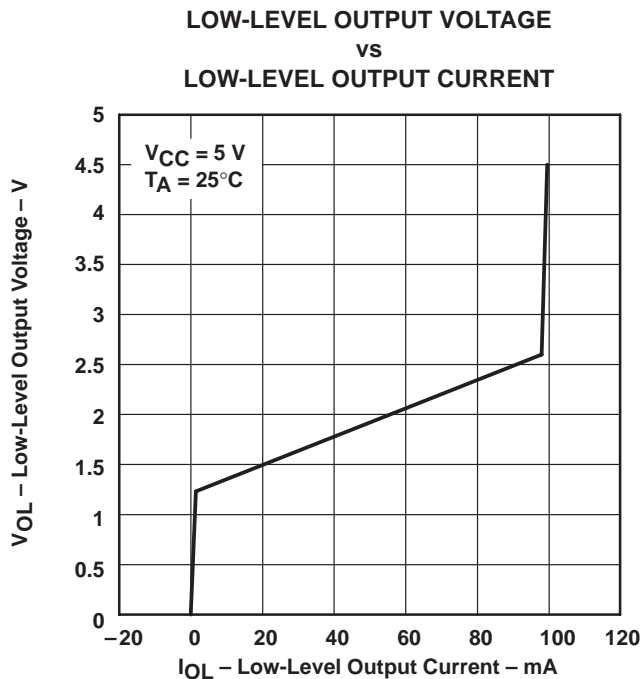


Figure 7

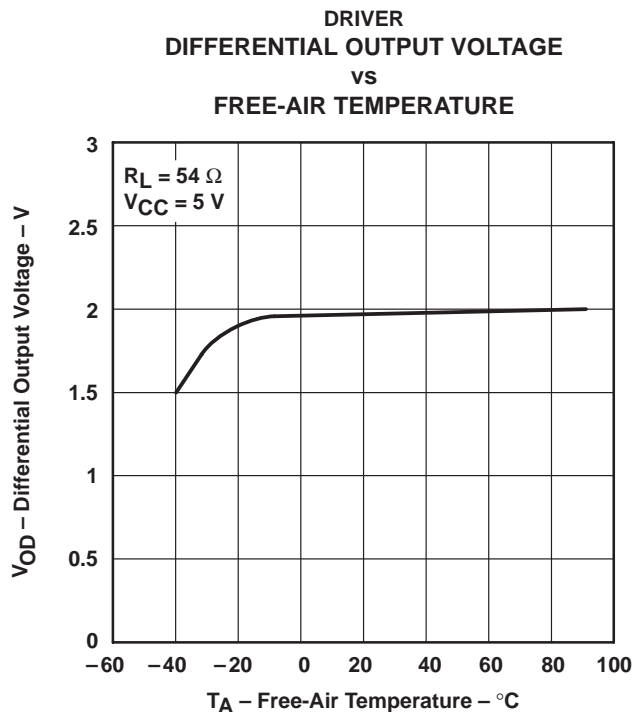


Figure 8

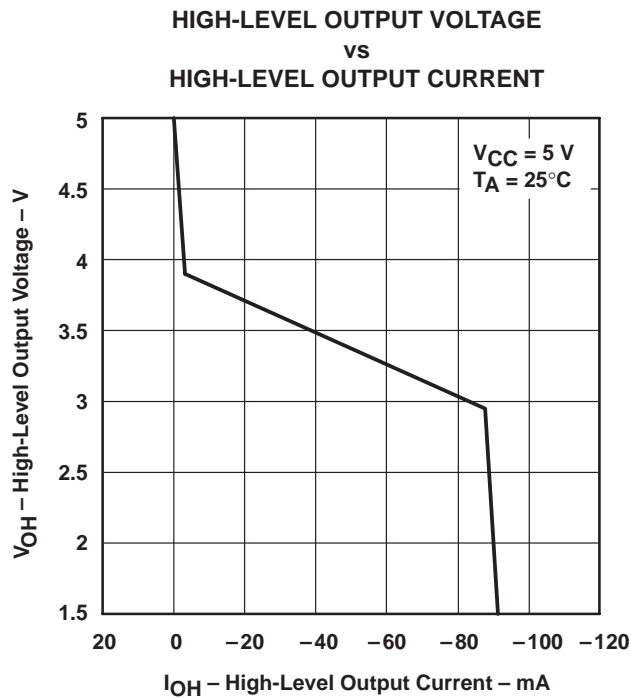
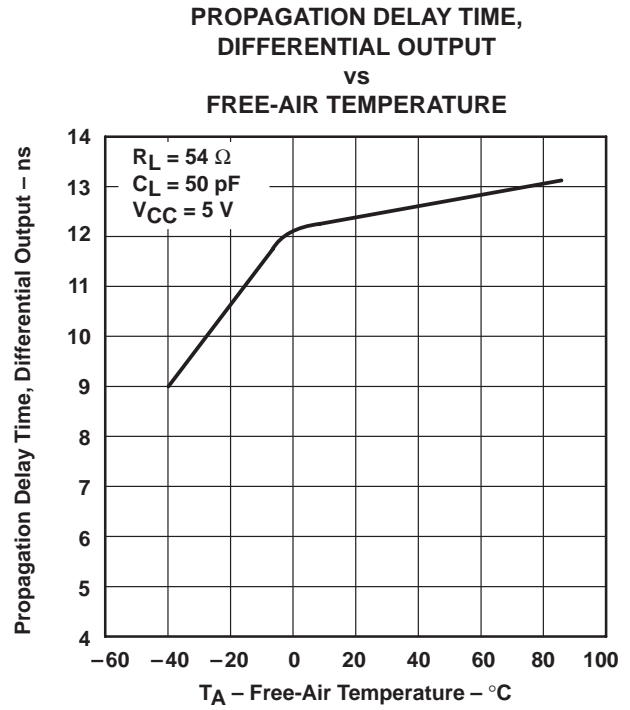
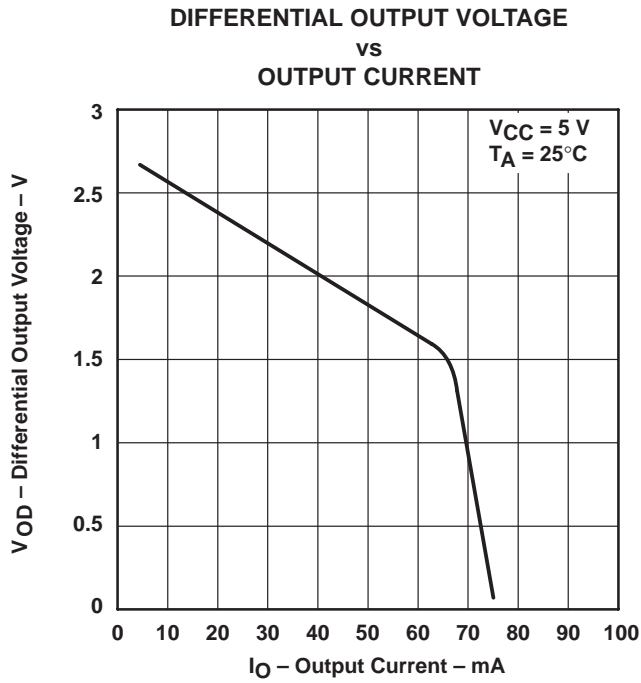


Figure 9

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TYPICAL CHARACTERISTICS



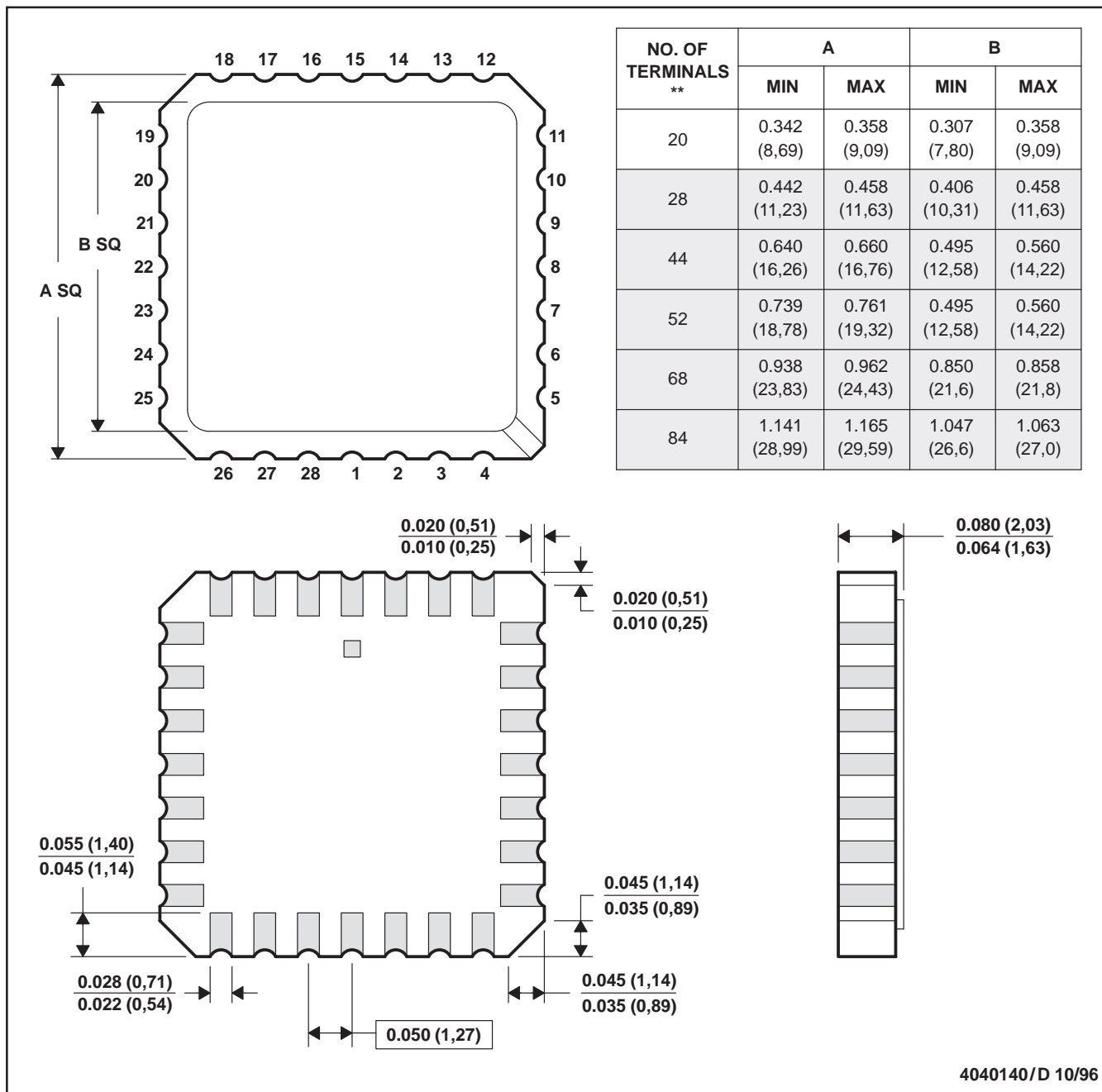
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FK (S-CQCC-N)**

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

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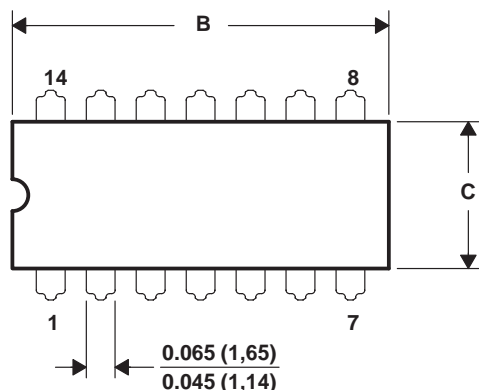
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MECHANICAL DATA

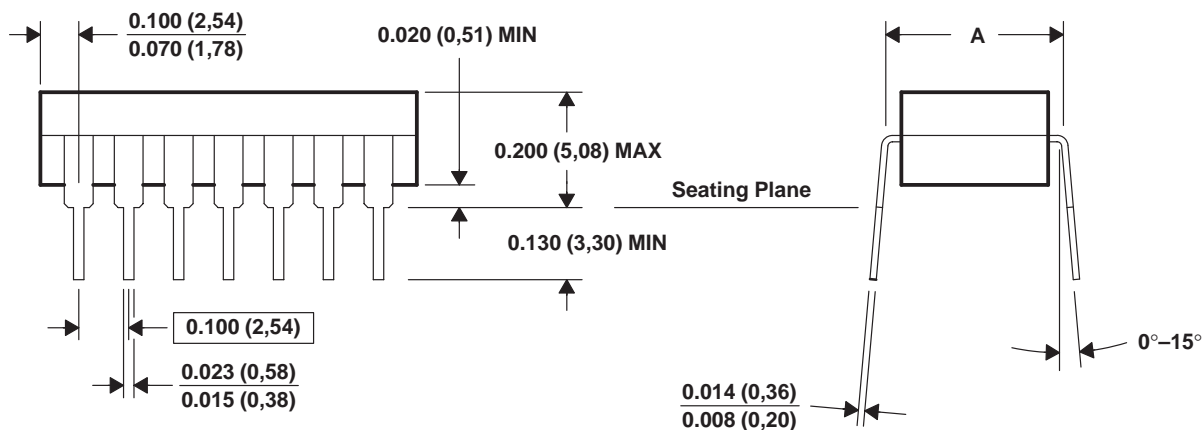
J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



DIM	PINS **			
	14	16	18	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)



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- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

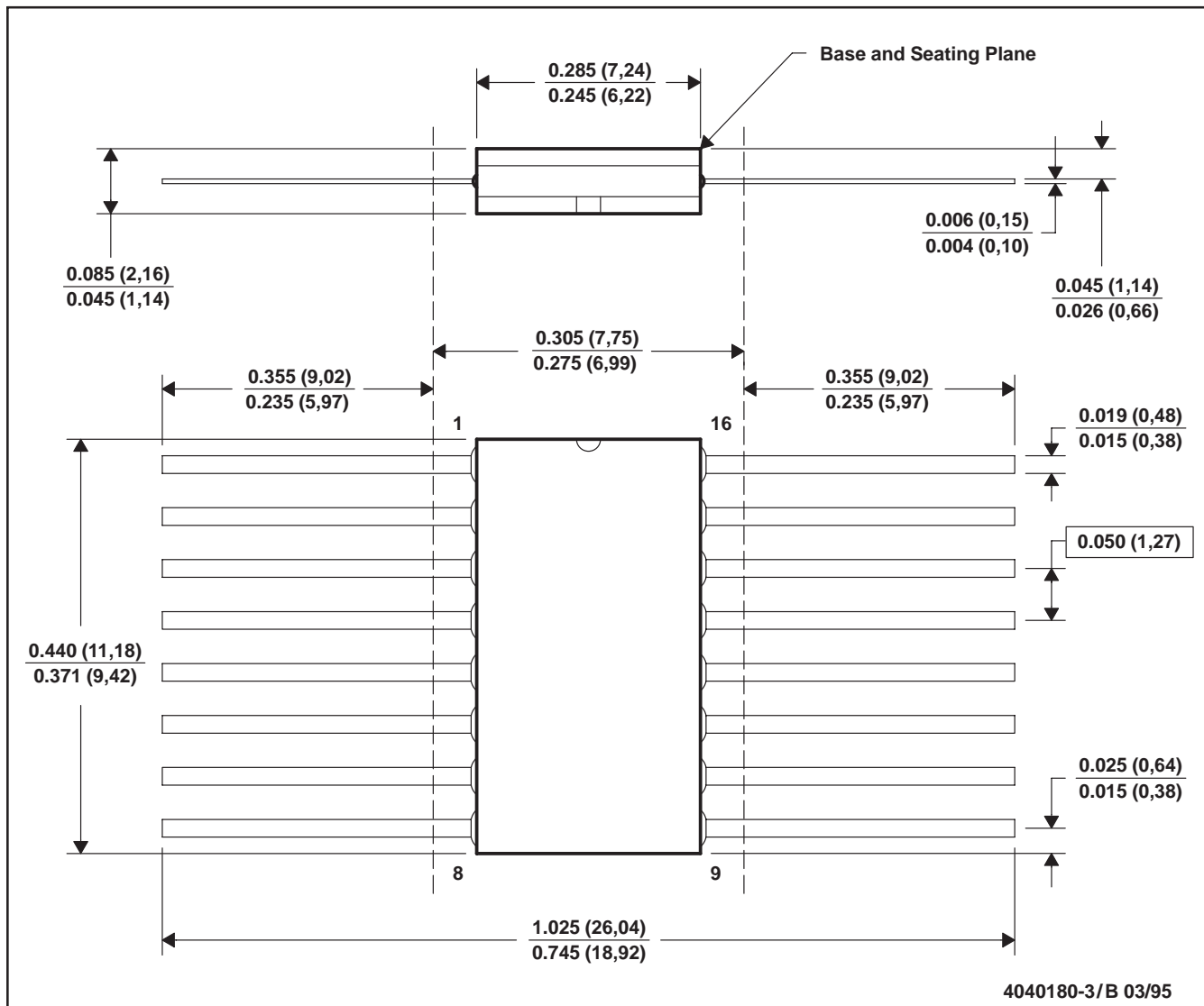
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MECHANICAL DATA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC

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