

# SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS417F – JUNE 1998 – REVISED NOVEMBER 2002

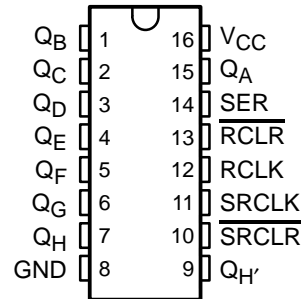
- Inputs Are TTL-Voltage Compatible
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## description/ordering information

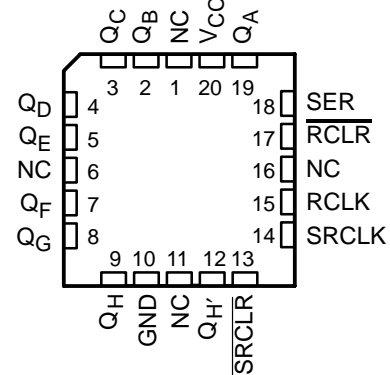
The 'AHCT594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ( $\overline{\text{SRCLR}}$ ,  $\overline{\text{RCLR}}$ ) inputs are provided on both the shift and storage registers. A serial ( $Q_H$ ) output is provided for cascading purposes.

Both the shift register (SRCLK) and storage register (RCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register always is one count pulse ahead of the storage register.

SN54AHCT594 . . . J OR W PACKAGE  
SN74AHCT594 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHCT594 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHCT594N	SN74AHCT594N
	SOIC – D	Tube	SN74AHCT594D	AHCT594
		Tape and reel	SN74AHCT594DR	
	SOP – NS	Tape and reel	SN74AHCT594NSR	AHCT594
	SSOP – DB	Tape and reel	SN74AHCT594DBR	HB594
TSSOP – PW	Tape and reel	SN74AHCT594PWR	HB594	
–55°C to 125°C	CDIP – J	Tube	SNJ54AHCT594J	SNJ54AHCT594J
	CFP – W	Tube	SNJ54AHCT594W	SNJ54AHCT594W
	LCCC – FK	Tube	SNJ54AHCT594FK	SNJ54AHCT594FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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**SN54AHCT594, SN74AHCT594**  
**8-BIT SHIFT REGISTERS**  
**WITH OUTPUT REGISTERS**

SCLS417F – JUNE 1998 – REVISED NOVEMBER 2002

**FUNCTION TABLE**

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift-register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift-register data is stored in the storage register.
X	X	X	↓	H	Storage-register state is not changed.

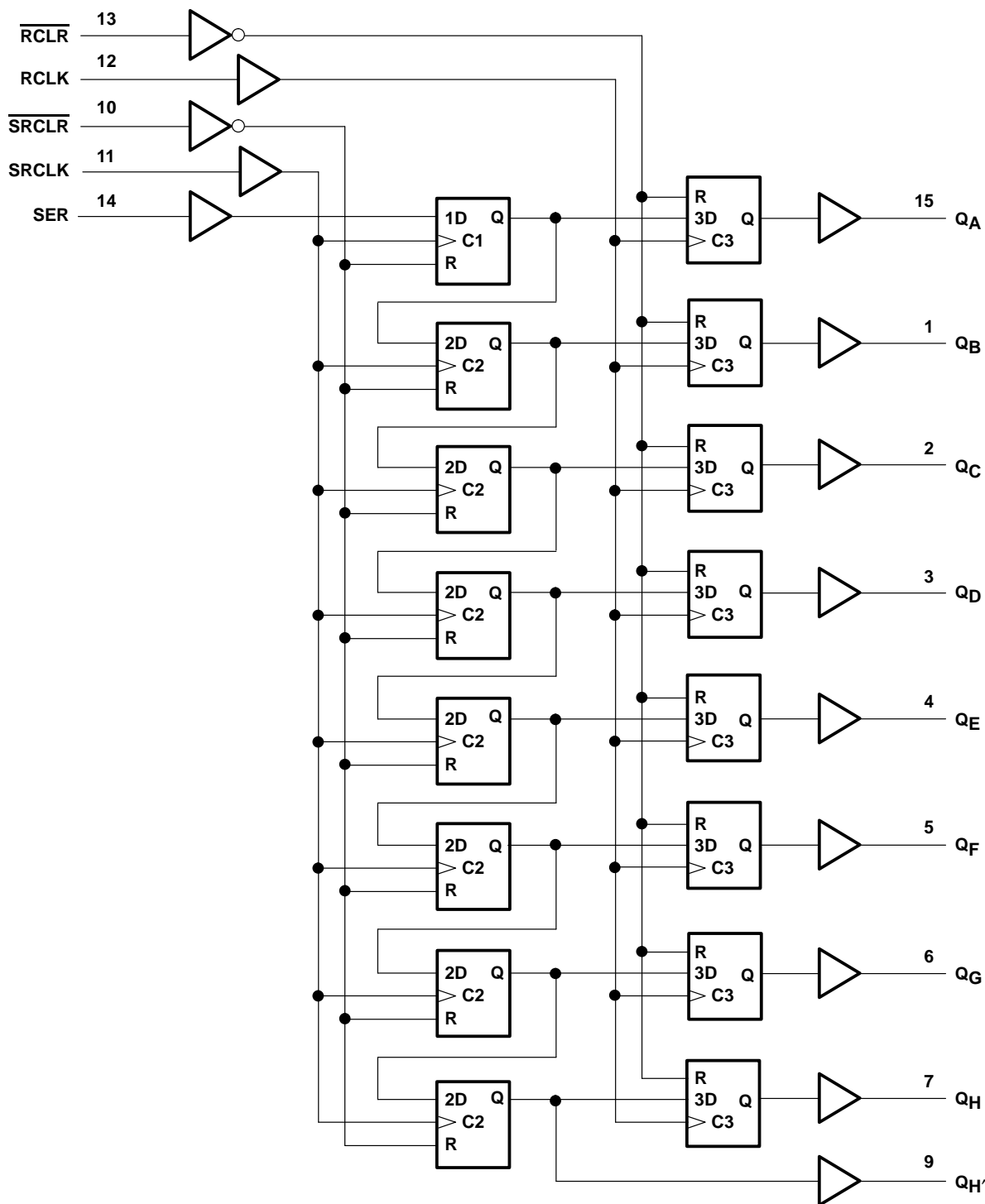


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SCLS417F – JUNE 1998 – REVISED NOVEMBER 2002

## logic diagram (positive logic)

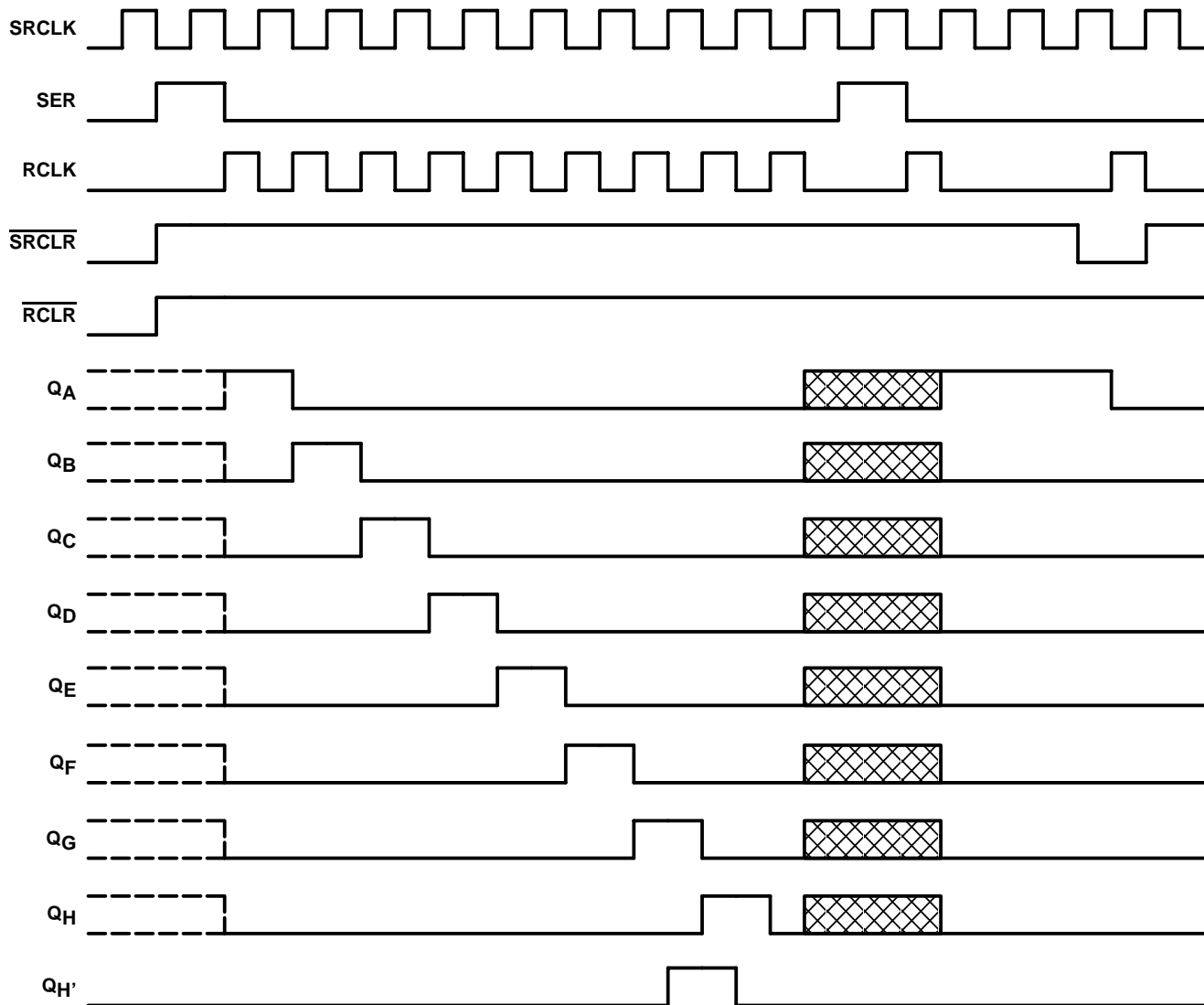


Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

# SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS417F – JUNE 1998 – REVISED NOVEMBER 2002

## timing diagram



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 75$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	73°C/W
DB package .....	82°C/W
N package .....	67°C/W
NS package .....	64°C/W
PW package .....	108°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

	SN54AHCT594		SN74AHCT594		UNIT
	MIN	MAX	MIN	MAX	
$V_{CC}$ Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		2		V
$V_{IL}$ Low-level input voltage		0.8		0.8	V
$V_I$ Input voltage	0	5.5	0	5.5	V
$V_O$ Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$ High-level output current		-8		-8	mA
$I_{OL}$ Low-level output current		8		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20		20	ns/V
$T_A$ Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54AHCT594, SN74AHCT594

## 8-BIT SHIFT REGISTERS

### WITH OUTPUT REGISTERS

SCLS417F – JUNE 1998 – REVISED NOVEMBER 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHCT594		SN74AHCT594		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I <sub>OH</sub> = -8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1			0.1	V	
	I <sub>OL</sub> = 8 mA				0.36		0.44	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1			±1*	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2		20	20	μA	
ΔI <sub>CC</sub> †	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			2		2.2	2.2	mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10			10	pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		SN54AHCT594		SN74AHCT594		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	RCLK or SRCLK high or low	5		5.5		5.5	ns
		RCLR or SRCLR low	5.2		5.5		5.5	
t <sub>su</sub>	Setup time	SER before SRCLK↑	3		3		3	ns
		SRCLK↑ before RCLK↑‡	5		5		5	
		SRCLR low before RCLK↑	5		5		5	
		SRCLR high (inactive) before SRCLK↑	2.9		3.3		3.3	
		RCLR high (inactive) before RCLK↑	3.4		3.8		3.8	
t <sub>h</sub>	Hold time	SER after SRCLK↑	2		2		2	ns

‡ This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

# SN54AHCT594, SN74AHCT594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS417F – JUNE 1998 – REVISED NOVEMBER 2002

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT594		SN74AHCT594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	135*	170*		115*		115		MHz
			$C_L = 50\text{ pF}$	120	140		95		95		
$t_{\text{PLH}}$	RCLK	$Q_A-Q_H$	$C_L = 15\text{ pF}$		3.3*	6.2*	1*	6.5*	1	6.5	ns
$t_{\text{PHL}}$					3.7*	6.5*	1*	6.9*	1	6.9	
$t_{\text{PLH}}$	SRCLK	$Q_H$	$C_L = 15\text{ pF}$		3.7*	6.8*	1*	7.2*	1	7.2	ns
$t_{\text{PHL}}$					4.1*	7.2*	1*	7.6*	1	7.6	
$t_{\text{PHL}}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	$C_L = 15\text{ pF}$		4.5*	7.6*	1*	8.2*	1	8.2	ns
$t_{\text{PHL}}$	$\overline{\text{SRCLR}}$	$Q_H$	$C_L = 15\text{ pF}$		4.1*	7.1*	1*	7.6*	1	7.6	ns
$t_{\text{PLH}}$	RCLK	$Q_A-Q_H$	$C_L = 50\text{ pF}$		4.9	7.8	1	8.3	1	8.3	ns
$t_{\text{PHL}}$					5.8	8.9	1	9.7	1	9.7	
$t_{\text{PLH}}$	SRCLK	$Q_H$	$C_L = 50\text{ pF}$		5.5	8.6	1	9.1	1	9.1	ns
$t_{\text{PHL}}$					6	9.2	1	10.1	1	10.1	
$t_{\text{PHL}}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	$C_L = 50\text{ pF}$		6.6	10	1	10.7	1	10.7	ns
$t_{\text{PHL}}$	$\overline{\text{SRCLR}}$	$Q_H$	$C_L = 50\text{ pF}$		6	9.2	1	10.1	1	10.1	ns

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER		SN74AHCT594			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		1		V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.8		V
$V_{IH(D)}$	High-level dynamic input voltage		2		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

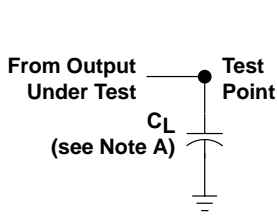
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	112	pF

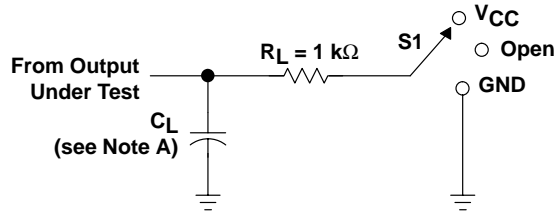
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SCLS417F – JUNE 1998 – REVISED NOVEMBER 2002

## PARAMETER MEASUREMENT INFORMATION

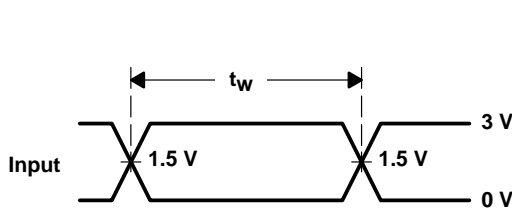


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

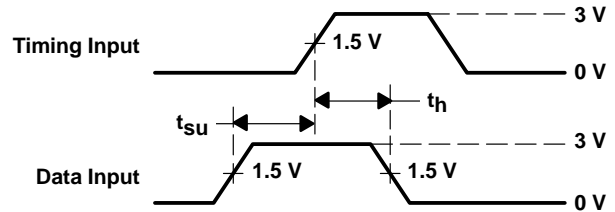


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

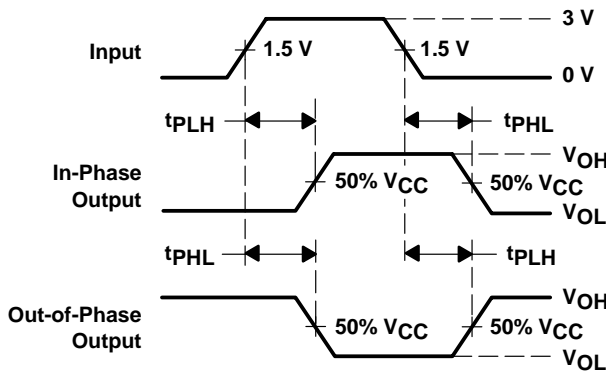
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	VCC
$t_{PHZ}/t_{PZH}$	GND
Open Drain	VCC



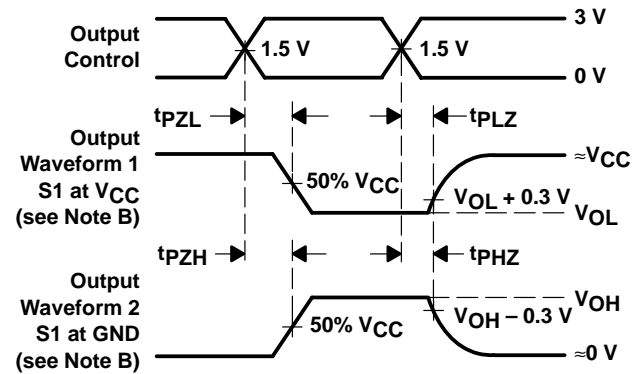
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

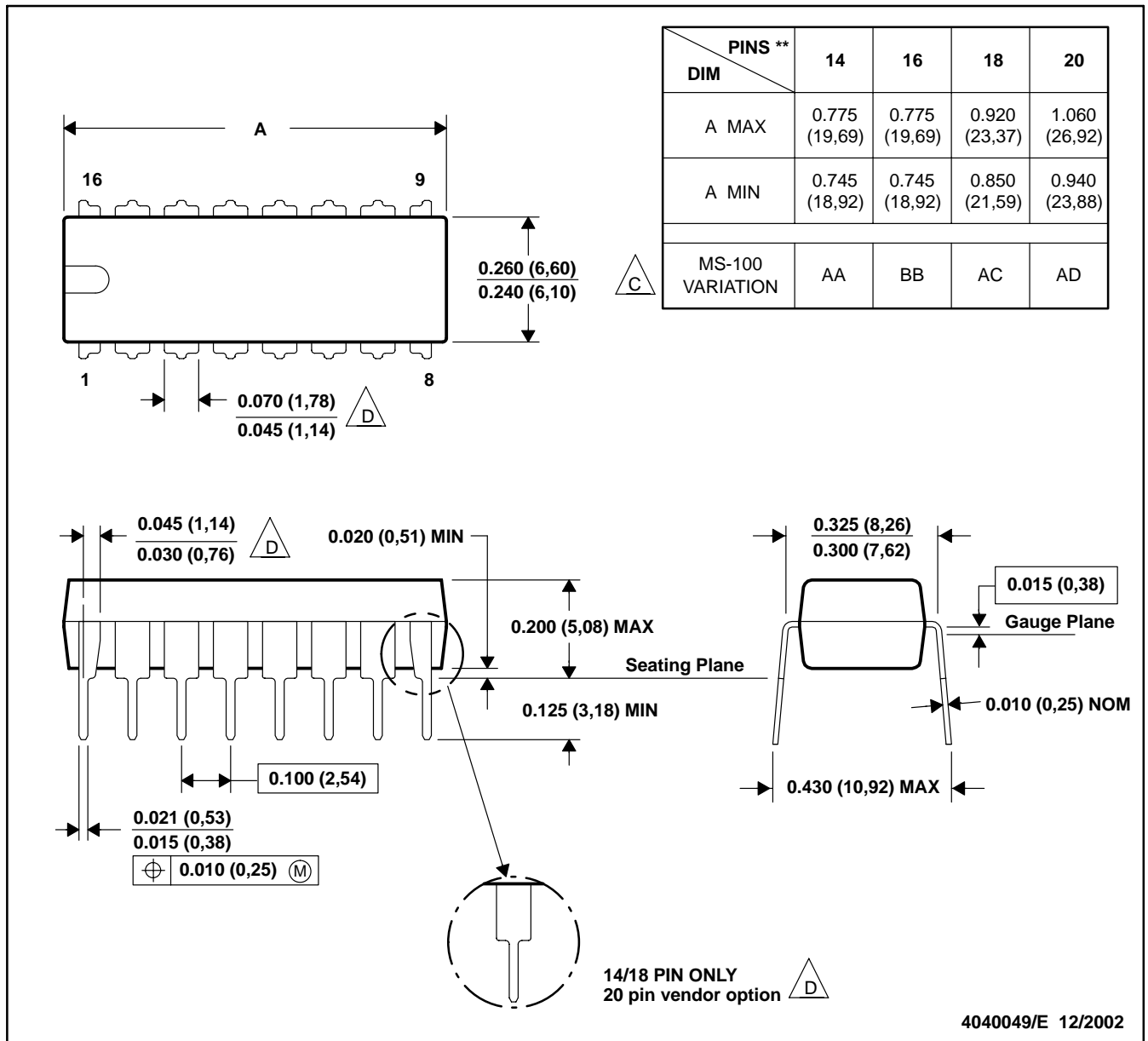
Figure 1. Load Circuit and Voltage Waveforms



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

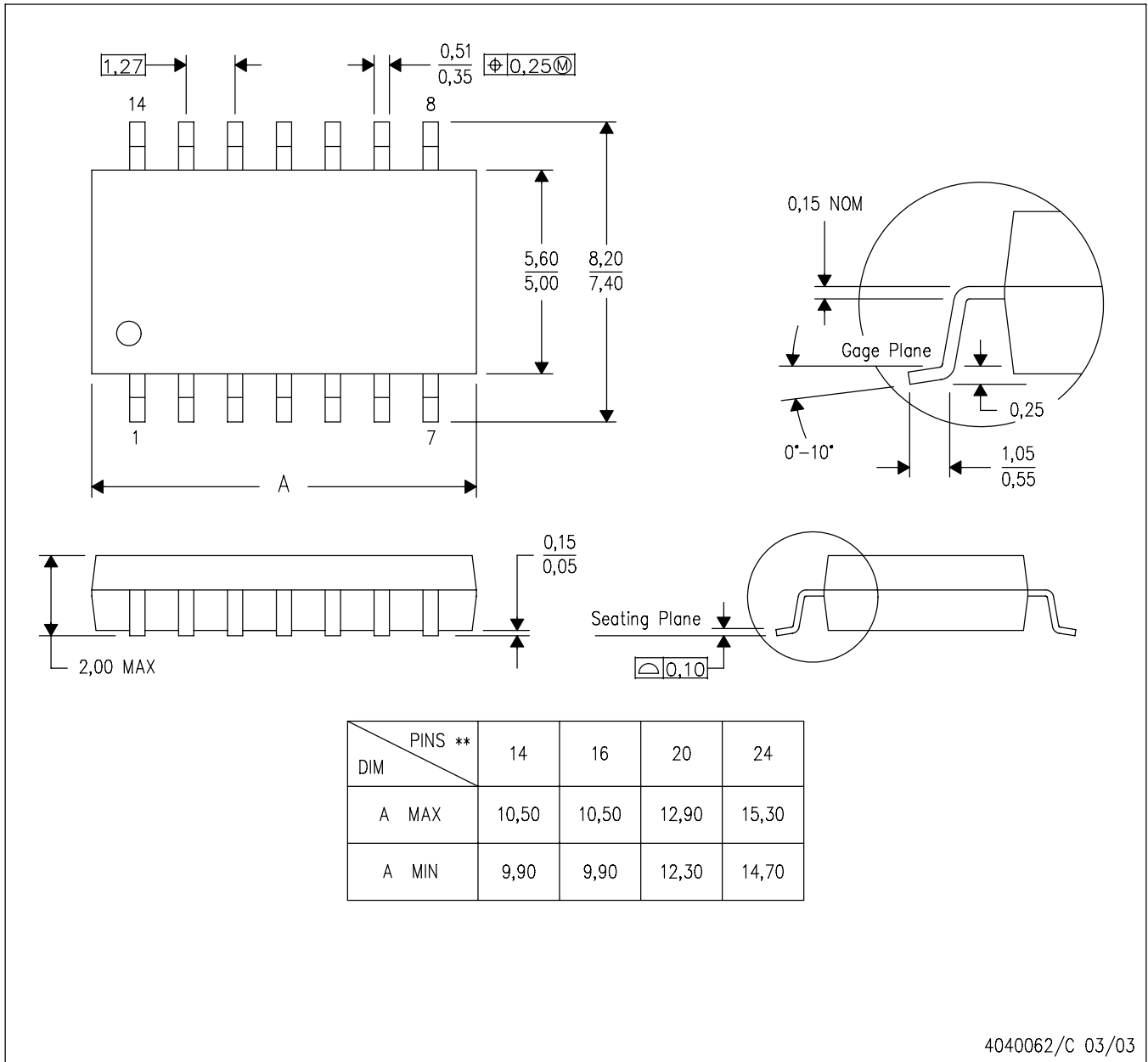


4040047/E 09/01

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

NS (R-PDSO-G\*\*)   
 14-PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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