3.3V DUAL DIFFERENTIAL LVPECL-TO-LVTTL TRANSLATOR

Precision Edge™
SY89323L

FEATURES

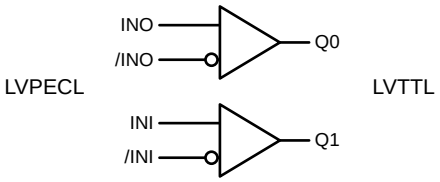
- **3.3V power supply**
- **1.9ns typical propagation delay**
- **Maximum frequency > 275MHz**
- **Differential LVPECL inputs**
- **24mA LVTTL outputs**
- **Flow-through pinouts**
- **Internal input resistors: pull-down on IN, pull-down and pull-up on /IN**
- **Q output will default LOW with inputs open**
- **Available in ultra-small 8-pin MLF™ (2mm × 2mm) package**

Precision Edge™

DESCRIPTION

The SY89323L is a dual differential LVPECL-to-LVTTL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The SY89323L is functionally equivalent to the SY100EPT23L, but in an ultra-small 8-lead MLF™ package that features a 70% smaller footprint. The ultra-small package and the dual gate design of the SY89823L make it ideal for applications that require the translation of a clock and data signal in a minimal space. The inputs are compatible with 10k and 100k input levels and any standard differential LVPECL input referenced to a V_{CC} of 3.3V.

BLOCK DIAGRAM



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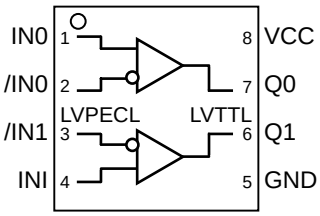
PACKAGE/ORDERING INFORMATION



8-Pin MLF™
Ultra-Small Outline (2mm x 2mm)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY89323LMITR(Note 1)	MLF-8	Industrial	323L

Note 1. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1, 4	IN0, IN1	100k ECL Input	Differential PECL/ECL Input: Internal 75kΩ pull-down resistor. If left open, pin defaults LOW. Q output will be LOW. See *"Input Interface Applications"* section for single-ended inputs.
2, 3	/IN0, /IN1	100k ECL Input	Differential PECL/ECL Input: Internal 75kΩ pull-up and pull-down resistors. If left floating, pin defaults to $V_{CC}/2$. When not used, this input can be left open. See *"Input Interface Applications"* section for single-ended inputs.
7, 6	Q0, Q1	LVTTL Output	Single-ended LVTTL Outputs: Default to LOW if IN inputs left open.
8	VCC	VCC Power	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.
5	GND, Exposed Pad	Ground	GND and exposed pad must be tied to ground plane.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to +3.8V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on IN, /IN ..... ±50mA
Lead Temperature (soldering, 10 sec.) ..... +220°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage (V_{CC}) ..... 3.0V to 3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance, **Note 3**
MLF™ (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF™ (Ψ_{JB})
  Junction-to-Board ..... 60°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

LVTTL DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0mA	2.0	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 24mA	—	—	0.5	V
I_{CC}	Power Supply Current		—	—	30	mA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	–80	—	–240	mA

LVPECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V±10%; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CC}–1.230	–	V_{CC}–0.735	V
V_{IL}	Input LOW Voltage		V_{CC}–1.950	–	V_{CC}–1.475	V
V_{IHCMR}	Input HIGH Common Mode Range	**Note 4**	V_{EE}+1.5	–	V_{CC}	V
V_{PP}	Minimum Peak-to-Peak Input		200			mV
I_{IH}	Input HIGH Current		–	–	150	µA
I_{IL}	Input LOW Current IN		0.5	–	–	µA
	/IN		–300	–	–	µA

Note 4. V_{IHCMR} (min) varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V±10%; C_L = 20pF, T_A = –40°C to +85°C, unless otherwise noted. All parameters guaranteed by design and characterization.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Input Frequency	**Notes 1, 2**	275	—	—	MHz
t_{pd}	Propagation Delay		1.5	—	2.5	ns
t_{skpp}	Part-to-Part Skew	**Notes 3**	—	—	0.5	ns
t_{skew++}	Within-Device Skew	**Notes 4**	—	—	0.3	ns
t_{skew--}	Within-Device Skew	**Notes 5**	—	—	0.3	ns
t_{jitter}	Cycle-to-Cycle	**Note 6**			2	ps^{rms}
	Total Jitter	**Note 7**			25	ps^{pk-pk}
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V		0.5	—	1.0	ns

Note 1. Frequency at which guaranteed for functionality. V_{OH} and V_{OL} levels are guaranteed at DC only.

Note 2. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

Note 3. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.

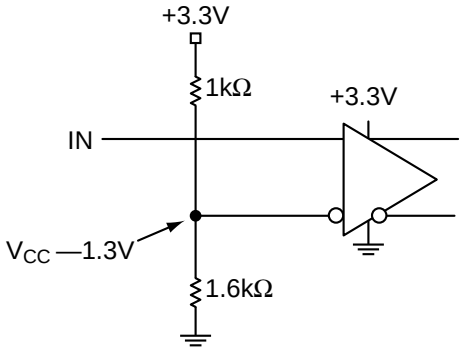
Note 4. Within-Device Skew considering HIGH-to -HIGH transitions at common V_{CC} level.

Note 5. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.

Note 6. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n - T_{n-1}$,where T is the time between rising edges of the output signal.

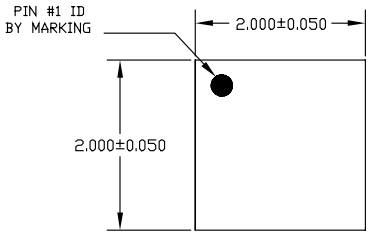
Note 7. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edge will deviate by more than the specified peak-to-peak jitter value.

INPUT INTERFACE APPLICATIONS

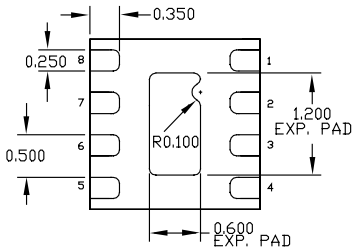


Single-Ended Input
(Terminating unused input)

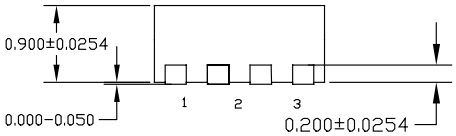
8 LEAD ULTRA-SMALL EPAD-*Micro*LeadFrame™ (MLF-8)



TOP VIEW

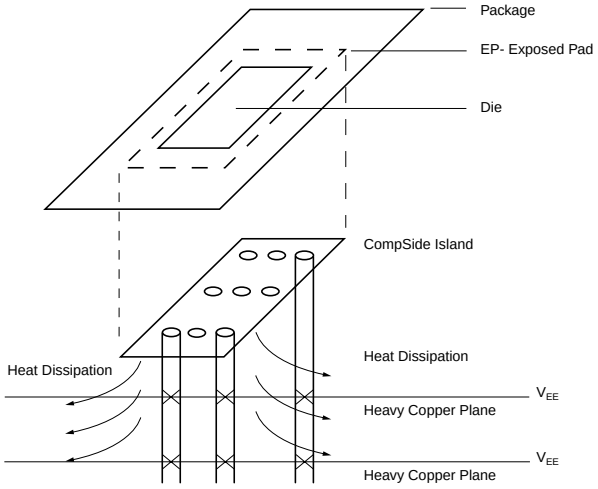


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 8-Pin MLF™ Package

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com