



SY89473U

Precision LVPECL 2:1 Multiplexer with 1:2 Fanout and Internal Termination

General Description

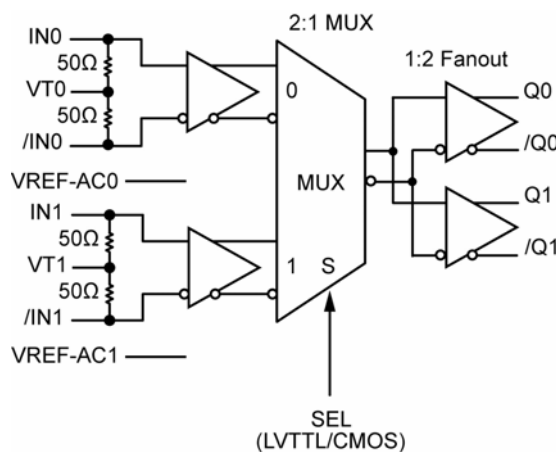
The SY89473U is a 2.5V/3.3V precision, high-speed 2:1 differential MUX capable of processing clocks up to 2.5GHz and data up to 2.5Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV (200mV_{PP}) without any level shifting or termination resistor networks in the signal path. The output is 800mV, 100K-compatible, LVPECL with fast rise/fall times guaranteed to be less than 190ps.

The SY89473U operates from a 2.5V $\pm 5\%$ or 3.3V $\pm 10\%$ supply and is guaranteed over the full industrial temperature range of -40°C to $+85^{\circ}\text{C}$. The SY89473U is part of Micrel's high-speed, Precision Edge[®] product line. For multiple-clock switchover solutions, please refer to the SY89840–SY89843U family.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Precision Edge[®]

Features

- Selects between two input channels and provides two copies of the selected output
- Guaranteed AC performance over temperature and supply voltage:
 - DC to 2.5Gbps data throughput
 - DC to 2.5GHz f_{MAX} (clock)
 - $<500\text{ps}$ In-to-Out t_{pd}
 - $<190\text{ps}$ t_r/t_f
 - $<20\text{ps}$ Output-to-output skew
- Unique patented input isolation design minimizes crosstalk
- Ultra-low Jitter Design:
 - $<1\text{ps}_{\text{RMS}}$ random jitter
 - $<1\text{ps}_{\text{RMS}}$ cycle-to-cycle jitter
 - $<10\text{ps}_{\text{PP}}$ total jitter (clock)
 - $<0.7\text{ps}_{\text{RMS}}$ crosstalk induced jitter
- Unique patent-pending input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- 800mV (100K) LVPECL output swing
- 2.5V $\pm 5\%$ or 3.3V $\pm 10\%$ supply voltage
- -40°C to $+85^{\circ}\text{C}$ industrial temperature range
- Available in 24-pin (4mm x 4mm) MLF[™] package

Applications

- Clock switchover
- Data distribution

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

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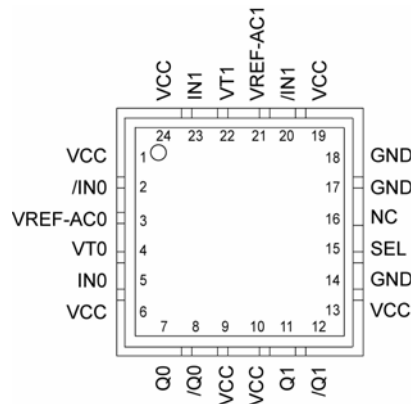
Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|-----------------------------|--------------|-----------------|--|-------------------|
| SY89473UMG | MLF-24 | Industrial | SY89473U with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY89473UMGTR ⁽²⁾ | MLF-24 | Industrial | SY89473U with Pb-Free bar-line indicator | NiPdAu Pb-Free |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals Only.
2. Tape and Reel.

Pin Configuration



24-Pin MLF™ (MLF-24)

Pin Description

| Pin Number | Pin Name | Pin Function |
|----------------------------|------------------------|---|
| 5, 2, 23, 20 | IN0, /IN0 IN1, /IN1 | Differential Inputs: These input pairs are the differential signal inputs to the device. They accept AC or DC-coupled signals as small as 100mV (200mV _{PP}). Note that these inputs will default to an indeterminate state if left open. Each pin of a pair internally terminates to a VT pin through 50Ω. Please refer to the "Input Interface Applications" section for more details. |
| 3, 21 | VREF-AC0, VREF-AC1 | Reference Voltage: These outputs bias to V _{CC} -1.2V. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01μF low ESR capacitor to VCC. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Please refer to the "Input Interface Applications" section for more details. |
| 4, 22 | VT0, VT1 | Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. Please refer to the "Input Interface Applications" section for more details. |
| 1, 6, 9, 10, 13, 19, 24 | VCC | Positive Power Supply: Connect to +2.5V or +3.3V power supply. Bypass with 0.1μF//0.01μF low ESR capacitors as close to VCC pins as possible. |
| 7, 8 11, 12 | Q0, /Q0 Q1, /Q1 | Differential Outputs: These differential LVPECL output pairs are a logic function of the IN0, IN1, and SEL inputs. Please refer to the truth table below for details. Unused output pairs can be left floating with no impact on jitter. |
| 15 | SEL | This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. V _{TH} = V _{CC} /2. Please refer to the "Timing Diagram" section for more details. |
| 14, 17, 18 | GND, Exposed Pad | Ground: Ground pins and exposed pad must be connected to the same ground plane. |

Truth Table

| INPUTS | | | | | OUTPUTS | |
|--------|------|-----|------|-----|---------|----|
| IN0 | /IN0 | IN1 | /IN1 | SEL | Q | /Q |
| 0 | 1 | X | X | 0 | 0 | 1 |
| 1 | 0 | X | X | 0 | 1 | 0 |
| X | X | 0 | 1 | 1 | 0 | 1 |
| X | X | 1 | 0 | 1 | 1 | 0 |

Absolute Maximum Ratings⁽¹⁾

| | |
|---------------------------------------|-------------------|
| Supply Voltage (V_{CC}) | -0.5V to +4.0V |
| Input Voltage (V_{IN}) | -0.5V to V_{CC} |
| LVPECL Output Current (I_{OUT}) | |
| Continuous | ±50mA |
| Surge | ±100mA |
| Input Current | |
| Source/sink Current on IN, /IN | ±50mA |
| Source/sink Current on V_T | ±100mA |
| V_{REF-AC} Current | |
| Source/sink Current on V_{REF-AC} | ±2mA |
| Lead Temperature (soldering, 20 sec.) | +260°C |
| Storage Temperature (T_S) | -65°C to 150°C |

Operating Ratings⁽²⁾

| | |
|---|--------------------|
| Supply Voltage (V_{CC}) | +2.375V to +2.625V |
| | +3.0V to +3.6V |
| Ambient Temperature (T_A) | -40°C to +85°C |
| Package Thermal Resistance ⁽³⁾ | |
| MLF™ (θ_{JA}) | |
| Still-Air | 50°C/W |
| MLF™ (Ψ_{JB}) | |
| Junction-to-Board | 30°C/W |

DC Electrical Characteristics⁽⁴⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|---|-------------------------|--------------|--------------|--------------|----------|
| V_{CC} | Power Supply | | 2.375 | 2.5 | 2.625 | V |
| | | | 3.0 | 3.3 | 3.6 | V |
| I_{CC} | Power Supply Current | No load, max V_{CC} . | | 45 | 65 | mA |
| R_{IN} | Input Resistance (IN-to- V_T) | | 45 | 50 | 55 | Ω |
| R_{DIFF_IN} | Differential Input Resistance (IN-to-/IN) | | 90 | 100 | 110 | Ω |
| V_{IH} | Input High Voltage (IN, /IN) | | 1.2 | | V_{CC} | V |
| V_{IL} | Input Low Voltage (IN, /IN) | | 0 | | $V_{IH}-0.1$ | V |
| V_{IN} | Input Voltage Swing (IN, /IN) | See Figure 1a. Note 5 | 0.1 | | V_{CC} | V |
| V_{DIFF_IN} | Differential Input Voltage Swing IN-/IN | See Figure 1b. | 0.2 | | | V |
| V_{T_IN} | IN-to- V_T (IN, /IN) | | | | 1.28 | V |
| V_{REF-AC} | Output Reference Voltage | | $V_{CC}-1.3$ | $V_{CC}-1.2$ | $V_{CC}-1.1$ | V |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IN} (max) is specified when V_T is floating.

LVPECL Outputs DC Electrical Characteristics⁽⁶⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 50\Omega$ to $V_{CC}-2V$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|--|----------------|----------------|------|----------------|-------|
| V_{OH} | Output HIGH Voltage Q, /Q | | $V_{CC}-1.145$ | | $V_{CC}-0.895$ | V |
| V_{OL} | Output LOW Voltage Q, /Q | | $V_{CC}-1.945$ | | $V_{CC}-1.695$ | V |
| V_{OUT} | Output Voltage Swing Q, /Q | See Figure 1a. | 550 | 800 | | mV |
| $V_{DIFF-OUT}$ | Differential Output Voltage Swing Q, /Q | See Figure 1b. | 1100 | 1600 | | mV |

LVTTL/CMOS DC Electrical Characteristics⁽⁶⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------|--------------------|-----------|------|-----|-----|---------|
| V_{IH} | Input HIGH Voltage | | 2.0 | | | V |
| V_{IL} | Input LOW Voltage | | | | 0.8 | V |
| I_{IH} | Input HIGH Current | | -125 | | 30 | μA |
| I_{IL} | Input LOW Current | | -300 | | | μA |

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$, $R_L = 50\Omega$ to $V_{CC}-2V$, unless otherwise stated.

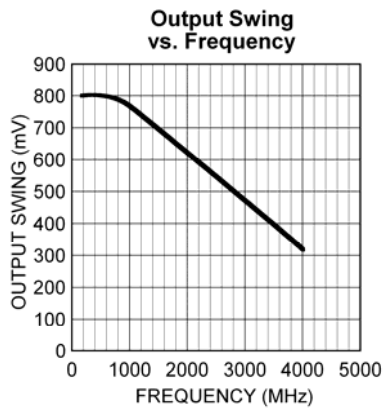
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------------|---|----------------------------|-----|-----|-----|-------------------|
| f_{MAX} | Maximum Operating Frequency | NRZ Data | 2.5 | 3.2 | | Gbps |
| | | $V_{OUT} \geq 400mV$ Clock | 2.5 | 3.0 | | GHz |
| t_{pd} | Differential Propagation Delay In-to-Q | | 250 | 320 | 500 | ps |
| | SEL-to-Q | $V_{TH} = V_{CC}/2$ | 250 | 360 | 600 | ps |
| T_{pd} Tempco | Differential Propagation Delay Temperature Coefficient | | | 158 | | fs/ $^\circ C$ |
| t_{SKEW} | Output-to-Output Skew | Note 8 | | 5 | 20 | ps |
| | Part-to-Part Skew | Note 9 | | | 200 | ps |
| t_{Jitter} | Clock Random Jitter | Note 10 | | | 1 | ps _{RMS} |
| | Cycle-to-Cycle Jitter | Note 11 | | | 1 | ps _{RMS} |
| | Total Jitter (TJ) | Note 12 | | | 10 | ps _{PP} |
| | Crosstalk-Induced Jitter | Note 13 | | | 0.7 | ps _{RMS} |
| t_r, t_f | Output Rise/Fall Time (20% to 80%) | At full output swing. | 70 | 130 | 190 | ps |

Notes:

- High-frequency AC-parameters are guaranteed by design and characterization.
- Output-to-output skew is measured between two different outputs under identical transitions.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- Random Jitter is measured with a K28.7 pattern, measured at $<f_{MAX}$.
- Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
- Total Jitter definition: With an ideal clock input of frequency $<f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
- Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

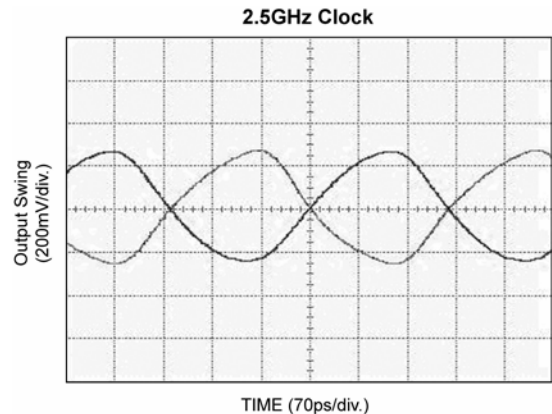
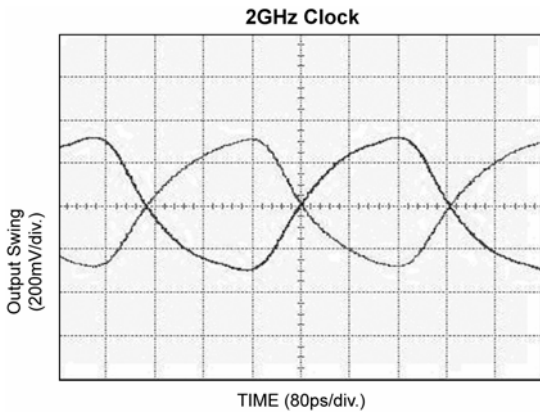
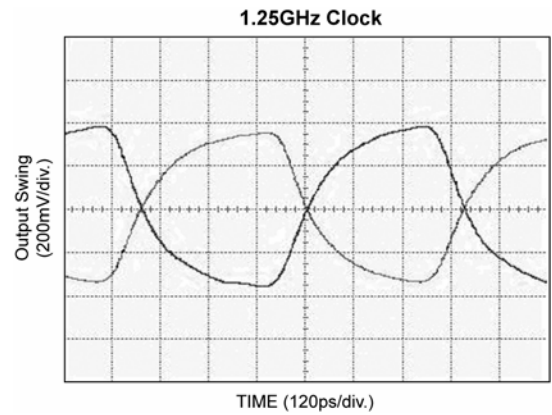
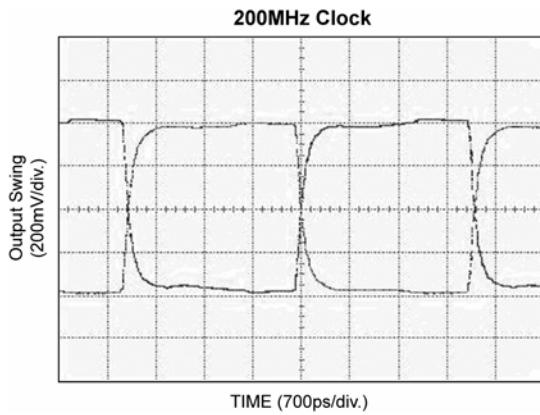
Typical Operating Characteristics

$V_{CC} = 3.3V$; $V_{IN} > 400mV$; $T_A = 25^\circ C$, $R_L = 50\Omega$ to $V_{CC}-2V$, unless otherwise stated.



Functional Characteristics

$V_{CC} = 3.3V$; $V_{IN} > 400mV$; $T_A = 25^\circ C$, $R_L = 50\Omega$ to $V_{CC}-2V$, unless otherwise stated.



Single-Ended and Differential Swings

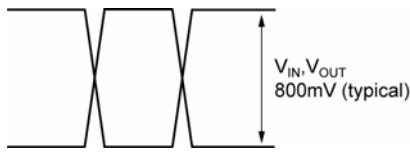


Figure 1a. Single-Ended Voltage Swing

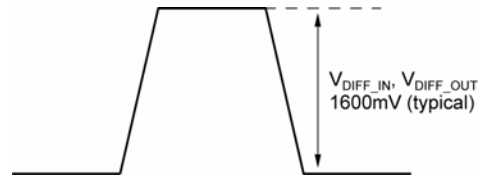
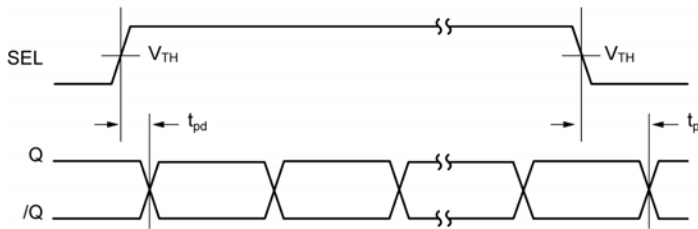
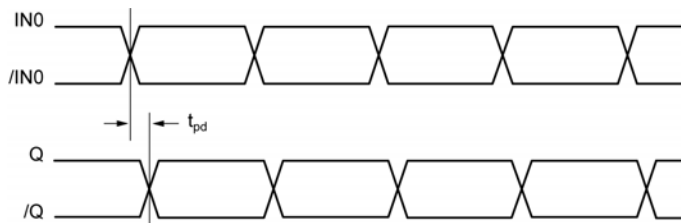


Figure 1b. Differential Voltage Swing

Timing Diagrams



Input and Output Stages

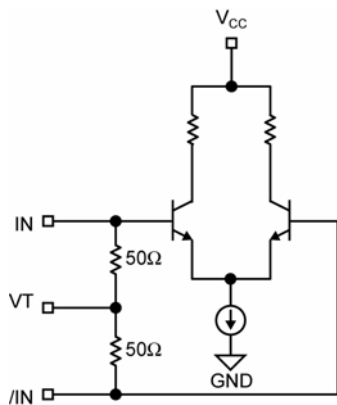


Figure 2a. Simplified Differential Input Stage

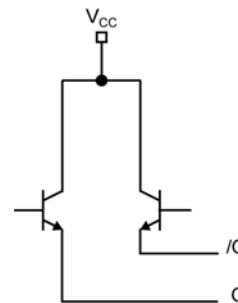


Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications

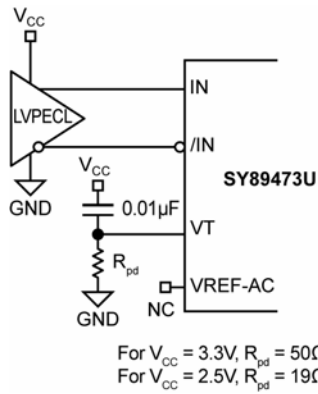


Figure 3a. LVPECL Interface (DC-Coupled)

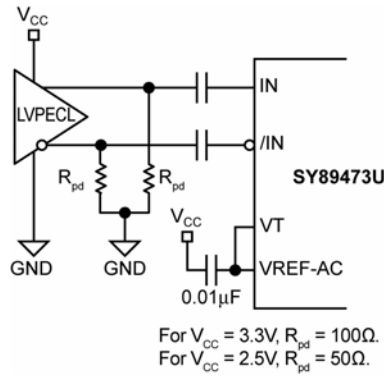
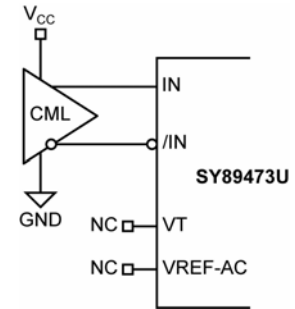


Figure 3b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

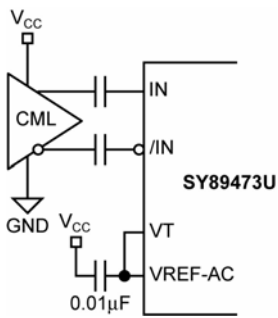


Figure 3d. CML Interface (AC-Coupled)

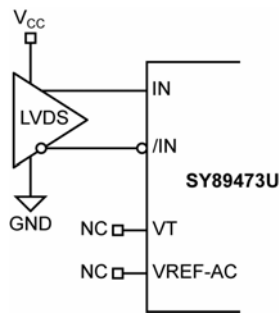
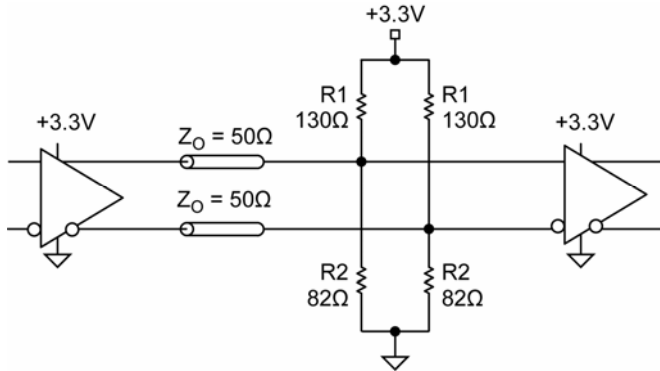


Figure 3e. LVDS Interface (DC-Coupled)

LVPECL Output Interface Applications

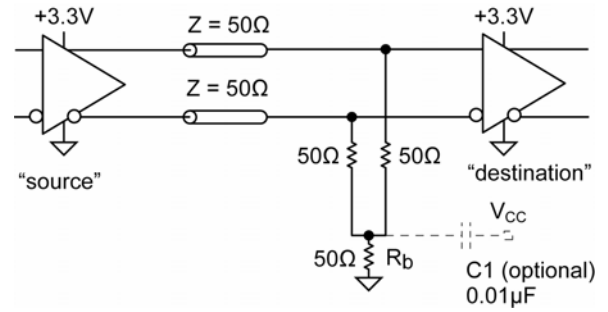
LVPECL has a high input impedance, a very low output impedance (open emitter), and a small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω- and 100Ω-controlled impedance transmission lines. There are several techniques for terminating the LVPECL output including: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-resistor), and AC-coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.



Note:

1. For +2.5V systems, R1 = 250Ω, R2 = 62.5Ω.

Figure 4a. Parallel Termination-Thevenin Equivalent



Note:

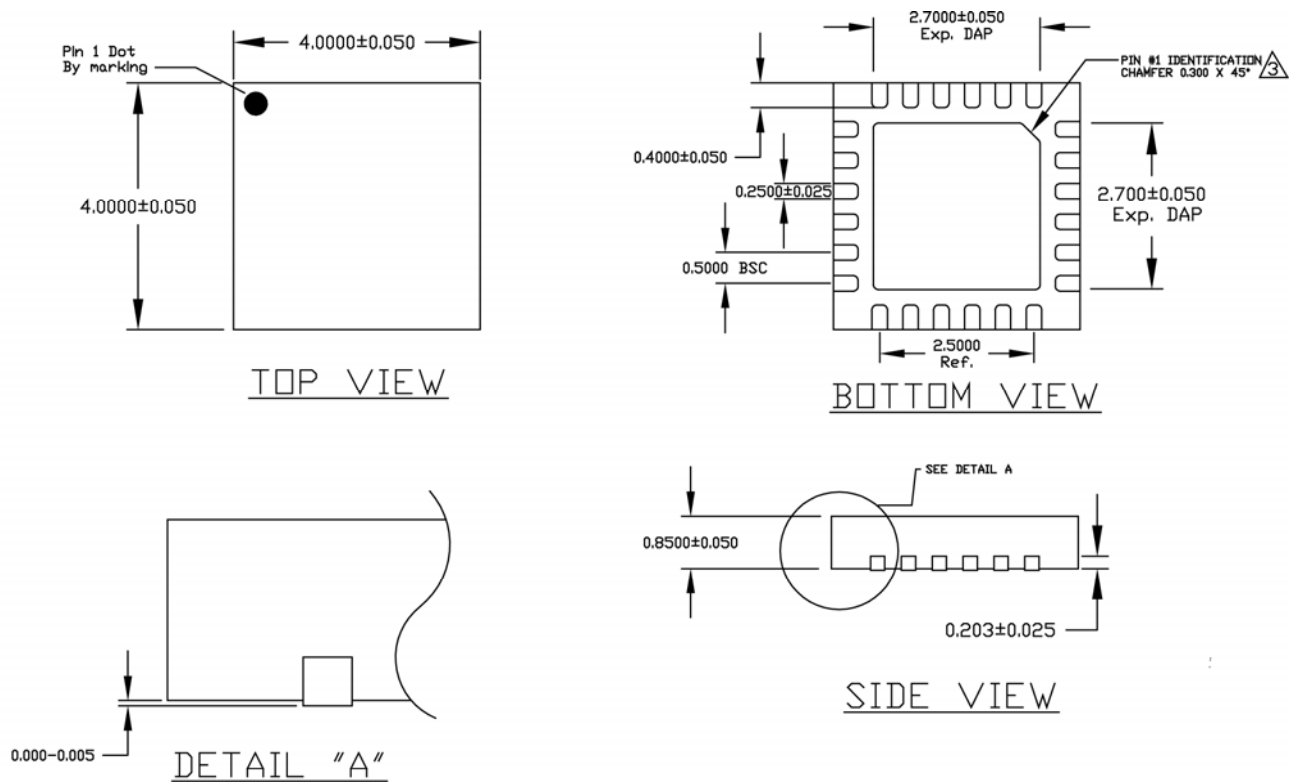
1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. Rb resistor sets the DC bias voltage, equal to V_T .
4. For 2.5V systems, Rb = 19Ω.

Figure 4b. Parallel Termination (3-Resistor)

Related Product and Support Information

| Part Number | Function | Data Sheet Link |
|---------------|---|--|
| SY89474U | Precision LVDS 2:1 Multiplexer with 1:2 Fanout and Internal Termination | www.micrel.com/product-info/products/sy89474u.shtml |
| SY89475U | Precision CML 2:1 Multiplexer with 1:2 Fanout and Internal Termination | www.micrel.com/product-info/products/sy89475u.shtml |
| | MLF™ Application Note | www.amkor.com/products/notes_papers/MLFAppNote.pdf |
| HBW Solutions | New Products and Applications | www.micrel.com/product-info/products/solutions.shtml |

Package Information



- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
 2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin MicroLeadFrame™ (MLF-24)

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