Preliminary

SZA-6044

5.1 – 5.9 GHz ¼ Watt
Power Amplifier with Active Bias

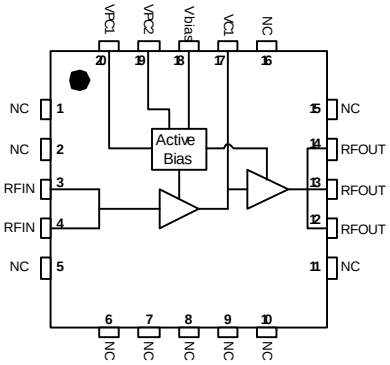
4mm x 4mm
QFN Package

Product Description

Sirenza Microdevices' SZA-6044 is a high linearity Class A GaAs Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. These HBT amplifiers are fabricated using molecular beam epitaxial growth technology which produces reliable and consistent performance from wafer to wafer and lot to lot.

This product is specifically designed as a driver or final stage amplifier for equipment in the 5.1 - 5.9 GHz band. It can run from a 3V to 5V supply. Load line optimization for target band is possible outside the package. Its high linearity makes it an ideal choice for multicarrier and digital applications.

Functional Block Diagram



Product Features

- **Single 3V to 5V operation**
- **High Linearity Class A OIP3 = 39dBm @ 5V**
- **802.11a 54Mb/s Pout = 17dBm @ 3% EVM**
- **P1dB 24dBm @ 5V, 21dBm @ 3.3V**
- **Surface Mount Plastic Package**
- **Power up/down control < 1μs**

Applications

- **OFDM**
- **Multicarrier applications**
- **802.11a WLAN Driver Stage**
- **Fixed Wireless, UNII**

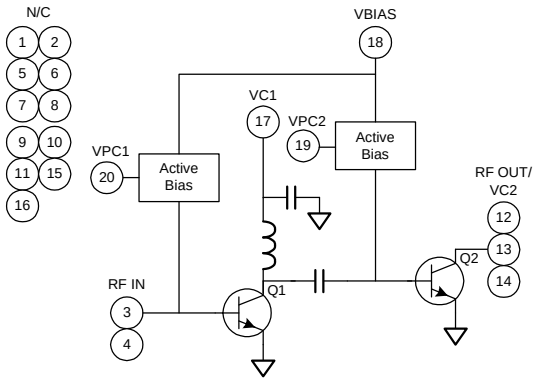
Key Specifications

Symbol	Parameters: Test Conditions, With App Circuit Z_0 = 50Ω, V_{CC} = 5.0V, I = 165mA, T_{BP} = 30ºC)	Unit	Min.	Typ.	Max.
f_O	Frequency of Operation	MHz	5100		5900
P_{1dB}	Output Power at 1dB Compression – 5.1 GHz	dBm		24.9	
	Output Power at 1dB Compression – 5.5 GHz			24.6	
	Output Power at 1dB Compression – 5.9 GHz		22.5	24.0	26.0
S_{21}	Small Signal Gain – 5.1 GHz	dB	17.0	18.5	20.0
	Small Signal Gain – 5.5 GHz			17.3	
	Small Signal Gain – 5.9 GHz		14.9	16.4	17.9
IRL	Worst Case Input Return Loss 5.1-5.9GHz	dB	8	11	
ORL	Worst Case Output Return Loss 5.1-5.9GHZ	dB	12	17	
OIP_3	Output IP3, Pout per tone = +8dBm @ 5.9 GHz	dBm	37	39	
Pout	802.11a 54Mb/s Pout @ 3% EVM @ 5.9GHz, I = 165mA	dBm		17	
NF	Noise Figure @ 5.9 GHz	dB		7.8	9.8
I_{SUPPLY}	Total Device Current, I_{VBIAS} + I_{CTOTAL} = 150mA I_{VPC12} = 15mA	mA	145	165	185
$R_{th, j-l}$	Thermal Resistance (junction - lead)	ºC/W		56	

Pin Out Description

Pin #	Function	Description
1,2,5,6, 7,8,9,10, 11,15,16	N/C	Pins are not used. May be grounded, left open or connected to adjacent pin.
19	VPC2	VPC2 is the bias control pin for the stage 2 active bias circuit. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value.
20	VPC1	VPC1 is the control pin for the stage 1 active bias circuits. An external series resistor is required for proper setting of bias levels. Refer to the evaluation board schematic for resistor value.
18	VBIAS	VBIAS is the active bias circuit supply voltage. Can be operated from 3V to 5V.
3,4	RFIN	RF input pin. This is DC grounded internal to the IC. Do not apply voltage to this pin. Both pins 3 and 4 must be used for proper operation.
12,13,14	RFOUT/ VC2	RF output and second stage collector supply voltage pin. VC2 in the range of 3V to 5V voltage should be supplied to this pin through an external RF choke. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see evaluation board schematic). The supply side of the bias network should be well bypassed. The output network and board layout specified in the app circuit is recommended for optimum performance. All pins 12-14 are required to be wired together at lead foot for proper operation.
17	VC1	VC1 is the first stage collector supply voltage. Can be operated over the range of 3V to 5V.
EPAD	Gnd	Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern (page 5).

Simplified Device Schematic



Absolute Maximum Ratings

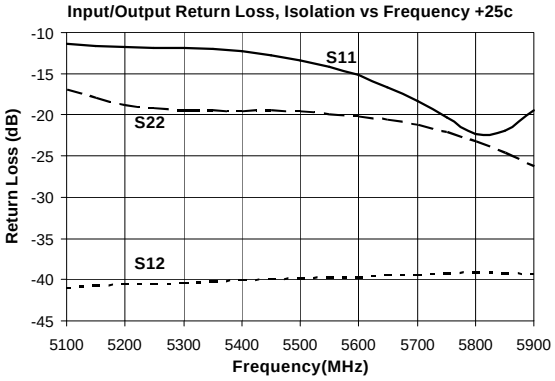
Parameters	Value	Unit
1st Stage Collector Bias Current (I_{VC1})	100	mA
2nd Stage Collector Bias Current (I_{VC2})	190	mA
Device Voltage (V_D)	6.0	V
Power Dissipation	1.5	W
Operating Lead Temperature (T_L)	-40 to +85	ºC
RF Input Power	20	dBm
Storage Temperature Range	-40 to +150	ºC
Operating Junction Temperature (T_J)	+150	ºC
ESD Human Body Model - Class 1B	500	V

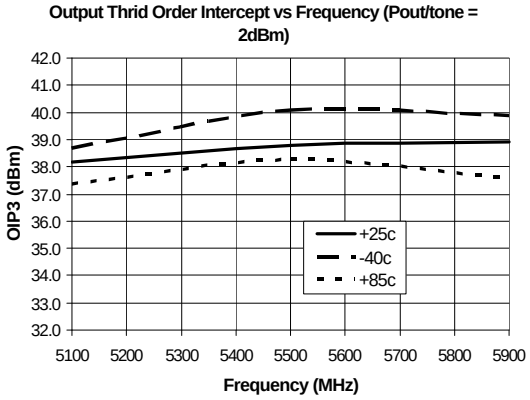
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation the device voltage and current must not exceed the maximum operating values specified in the table on page one.

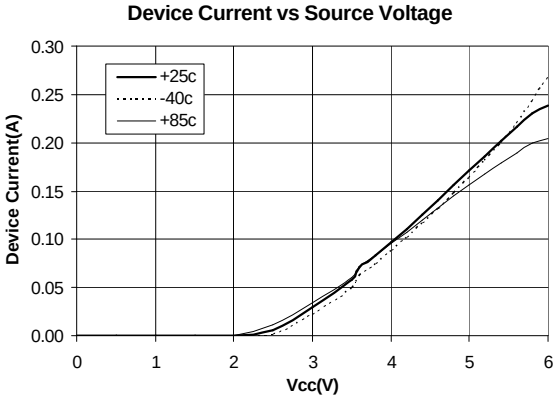
Bias conditions should also satisfy the following expression:
$I_D V_D < (T_J - T_L) / R_{TH, j-l}$

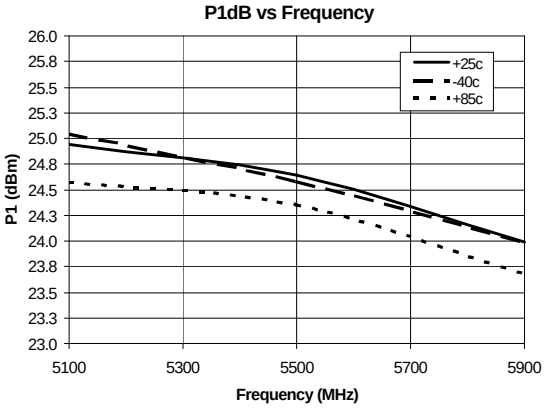
Caution: ESD Sensitive - Class 1B
Appropriate precaution in handling, packaging and testing devices must be observed.

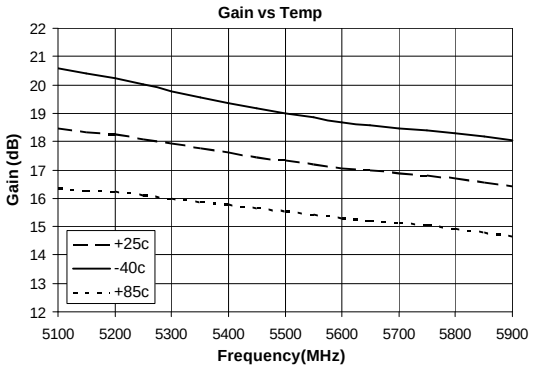
5.1 - 5.9 GHz Evaluation Board Data (V_{BIAS} = 5.0V, I_{BIAS} = 165mA)

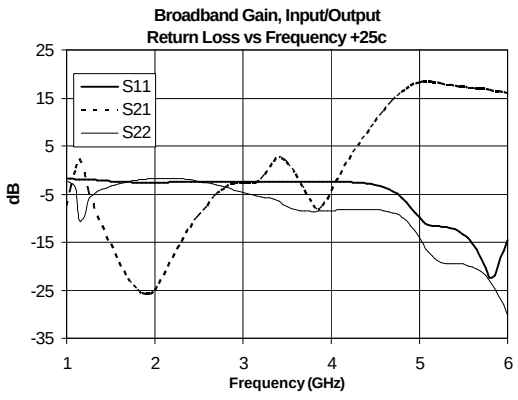






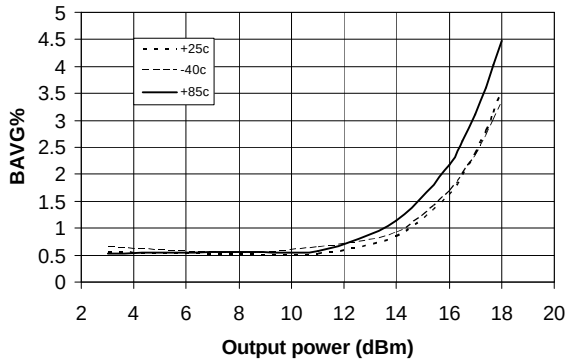




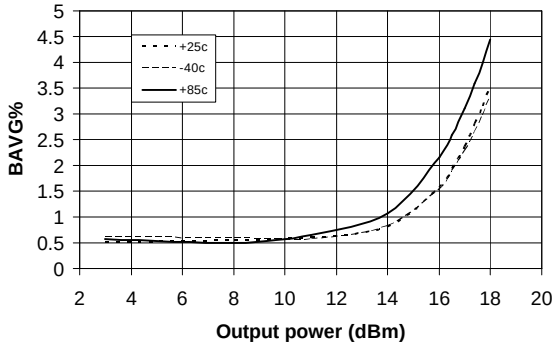


802.11a 64QAM 54Mb/s Error Vector Magnitude Data (V_{BIAS} = 5.0V, I_{BIAS} = 165mA)

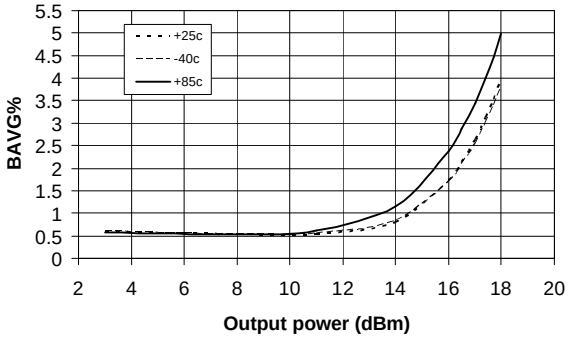
EVM Burst Average% vs Output Power (dBM)
Freq = 5.15GHz



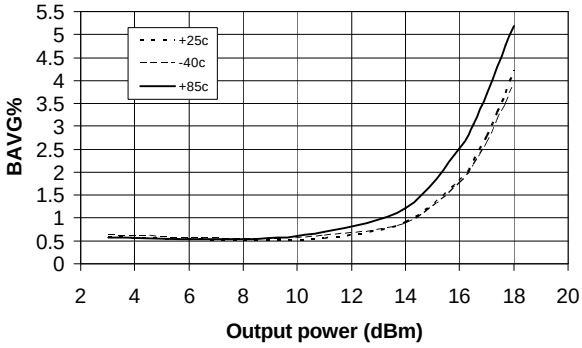
EVM Burst Average% vs Output Power (dBM)
Freq = 5.35GHz



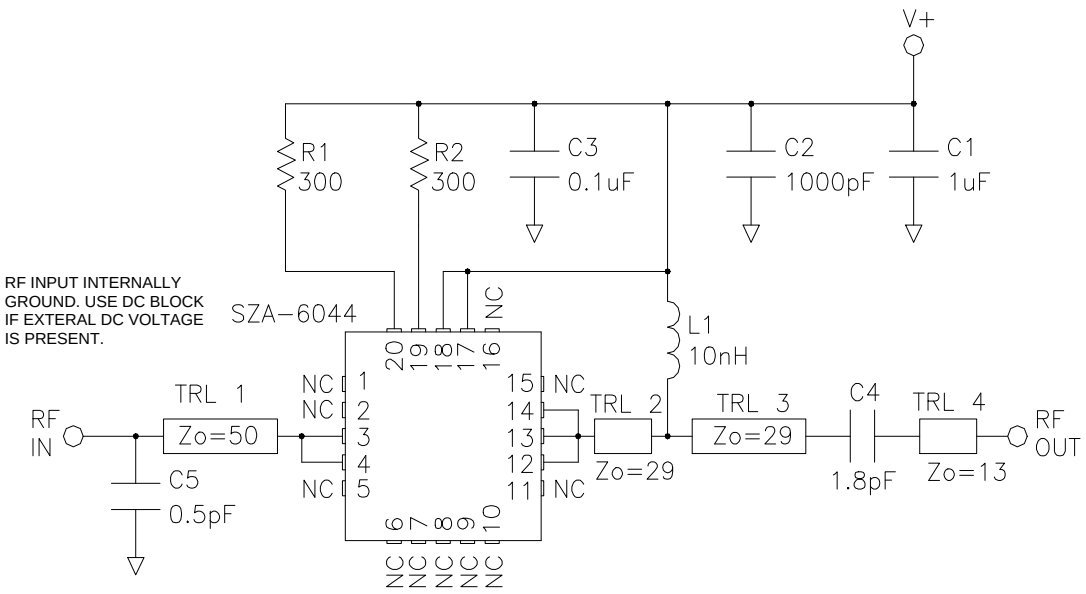
EVM Burst Average% vs Output Power (dBM)
Freq = 5.725GHz



EVM Burst Average% vs Output Power (dBM)
Freq = 5.875GHz

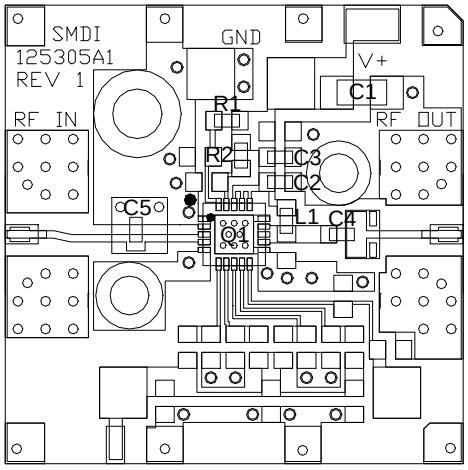


5.1 - 5.9 GHz Evaluation Board Schematic For 5V Supply



5.1 - 5.9 GHz Evaluation Board Layout For 5V - Board material GETEK, 31mil thick, Dk=3.9, 2 oz. copper

DESG	DESCRIPTION
Q1	SZA-6044
R1,2	300 OHM, 0603
C1	1uF CERAMIC CAP
C2	1000pF CAP, 0603
C3	0.1uF CAP, 0603
C4	1.8pF CAP, 0603
C5	0.5pF CAP, 0603
L1	10nH INDUCTOR, 0603 Toko LL1608-FS10NJ
TRL 1	Zo=50Ω ,54.2° @ 5.5GHz
TRL 2	Zo=29Ω ,22.3° @ 5.5GHz
TRL 3	Zo=29Ω ,38.4° @ 5.5GHz
TRL 4	Zo=13Ω ,16° @ 5.5GHz



Note: For 3.3V 140mA operation, lower V+ to 3.3V and change R1 and R2 to 50 ohm.
RF Performance at 3.3V, 140mA: Gain increases 0.5dB, IP3 drops ~ 3dB and P1dB drops ~3dB relative to 5V data.
Return loss is essentially unchanged relative to 5V data. Contact factory for more details.

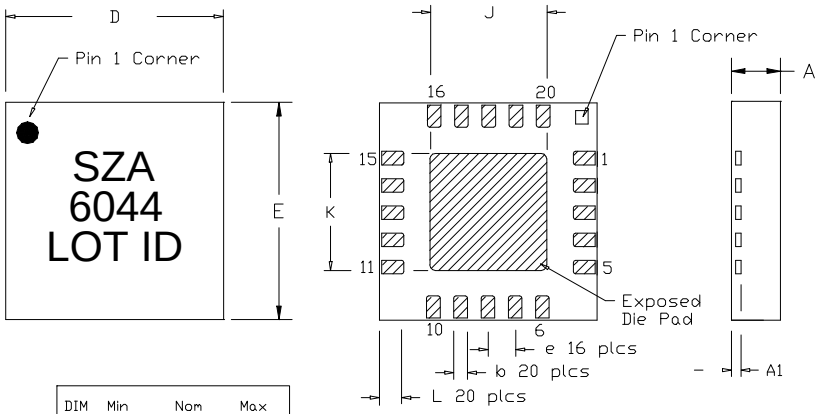
Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SZA-6044	13”	3000

Part Symbolization

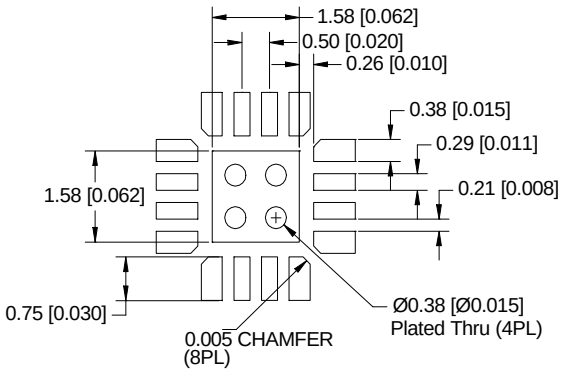
The part will be symbolized with an “SZA-6044” marking designator on the top surface of the package.

Package Outline Drawing



DIM	Min	Nom	Max
A	.80		1.00
A1	.19		.21
b	.20	.25	.30
D		4.0 BSC	
e		0.5 BSC	
E		4.0 BSC	
J	2.04		2.24
K	2.04		2.24
L	.34	.44	.54

Recommended Land Pattern (dimensions in mm[in]):



Recommended PCB Soldermask (SMBOC) for Land Pattern (dimensions in mm[in]):