

TC74VHCT00AF, TC74VHCT00AFN, TC74VHCT00AFT

QUAD 2-INPUT NAND GATE

The TC74VHCT00A is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The input voltage are compatible with TTL output voltage. This device may be used as a level converter for interfacing 3.3V to 5V system.

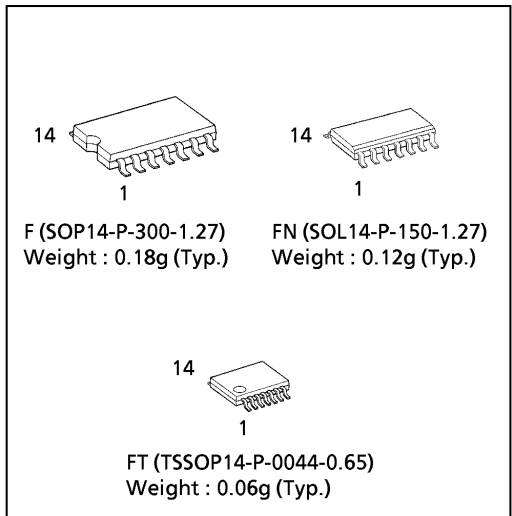
Input protection and output circuit ensure that 0 to 5.5V can be applied to the input and output*1 pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

*1: V_{cc}=0V

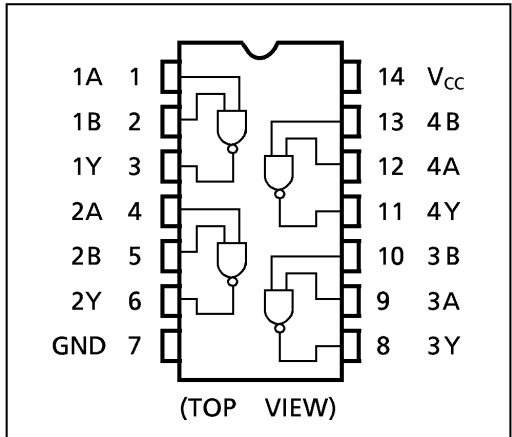
FEATURES :

- High Speed.....t_{pd} = 5.0ns(typ.) at V_{CC} = 5V
- Low Power Dissipation.....I_{CC} = 2μA(Max.) at Ta = 25°C
- Compatible with TTL outputs....V_{IL} = 0.8V (Max.)
V_{IH} = 2.0V (Min.)
- Power Down Protection is provided on all inputs and outputs.
- Balanced Propagation Delays.....t_{pLH} ≈ t_{pHL}
- Low NoiseV_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with the 74 series (74AC / HC / F / ALS / LS etc.) 00 type.

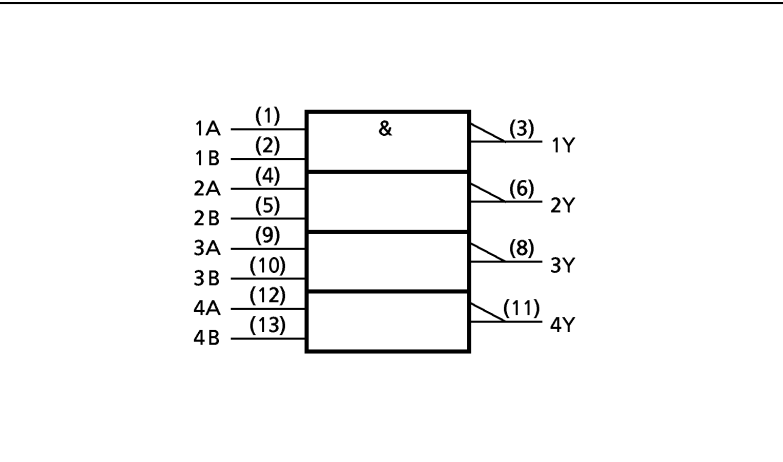
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

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● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~7.0 (Note 1)	V
		-0.5~ $V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20 (Note 3)	mA
DC Output Current	I_{OUT}	±25	mA
DC Vcc/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

(Note 1) $V_{CC} = 0V$

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.

(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~5.5 (Note 4)	V
		0~ V_{CC} (Note 5)	
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt / dV	0~20	ns / V

(Note 4) $V_{CC} = 0V$

(Note 5) High or Low State

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITON		Ta = 25°C			Ta = -40~85°C		UNIT	
				V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
High - Level Input Voltage	V _{IH}			4.5~5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V _{IL}			4.5~5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	4.5	4.40	4.50	—	4.40	—	V
			I _{OH} = -8mA	4.5	3.94	—	—	3.80	—	V
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I _{OL} = 8mA	4.5	—	—	0.36	—	0.44	V
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	2.0	—	20.0	
	I _{CCT}	PER INPUT : V _{IN} = 3.4V OTHER INPUT : V _{CC} or GND		5.5	—	—	1.35	—	1.50	
Output Leakage Current	I _{OPD}	V _{OUT} = 5.5V		0	—	—	0.5	—	5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.		MIN.
Propagation Delay Time	t _{pLH}	5.0 ± 0.5	15	—	5.0	6.9	1.0	8.0	ns
	t _{pHL}		50	—	5.5	7.9	1.0	9.0	
Input Capacitance	C _{IN}		—	4	10	—	10	pF	
Power Dissipation Capacitance	C _{PD}	(Note 6)	—	17	—	—	—		

(Note 6) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

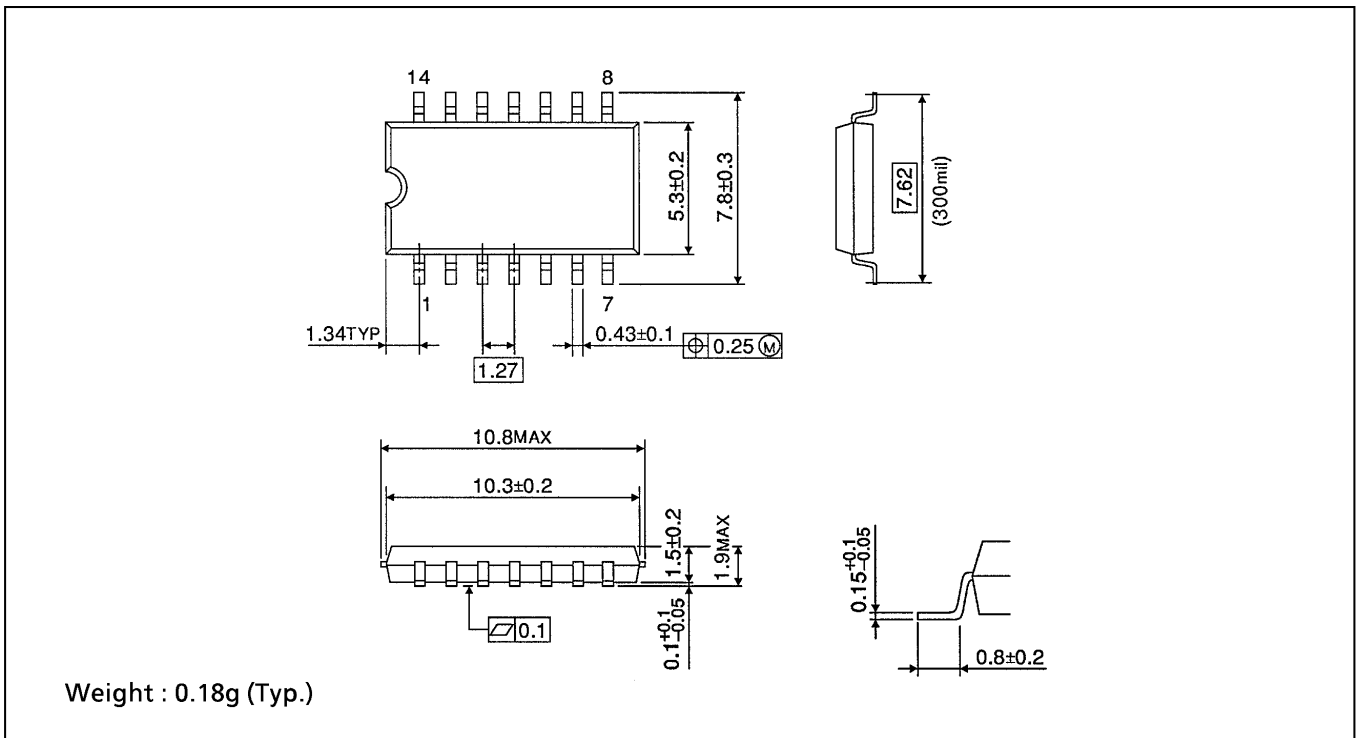
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.4	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.4	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	0.8	V

SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

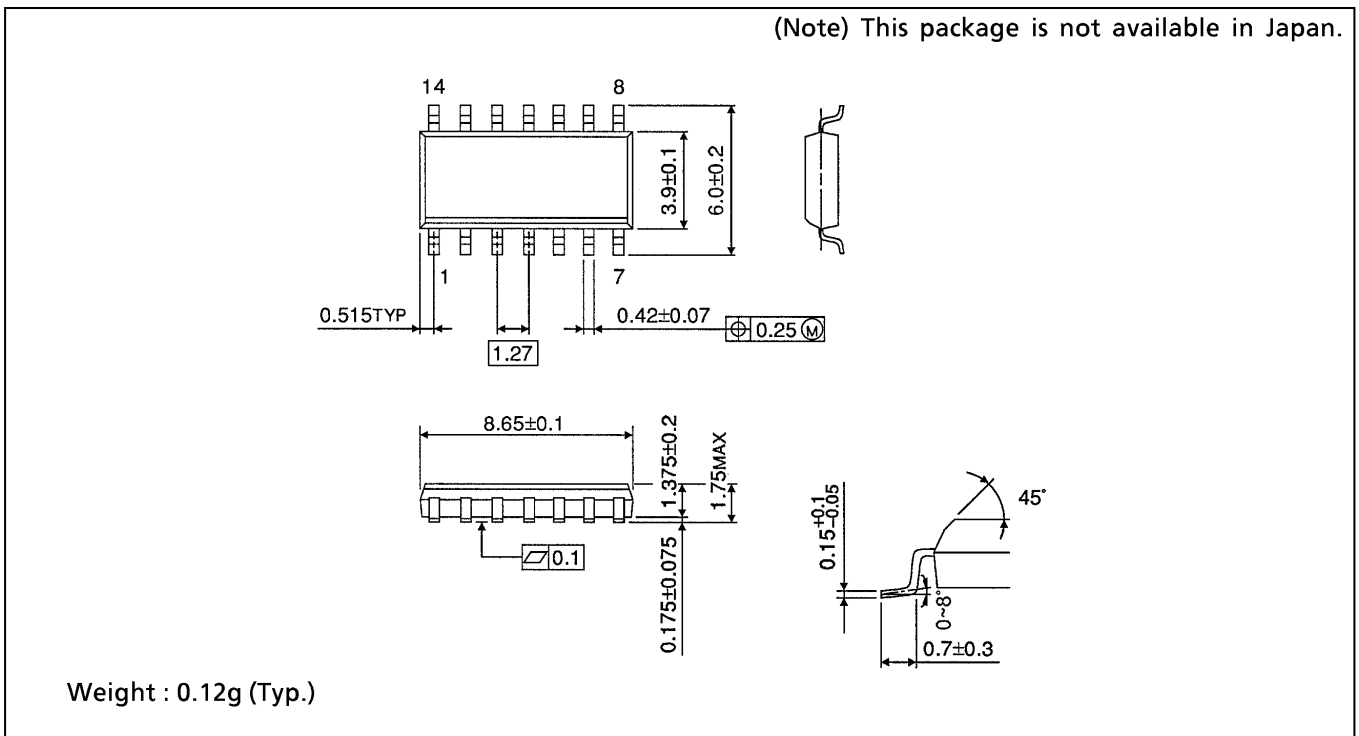
Unit in mm



SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOP14-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



TSSOP 14PIN OUTLINE DRAWING (TSSOP14-P-0044-0.65)

Unit in mm

