

Crystal Clock Oscillator



TCO-743TH7

FULL DIP Double-Sealed TTL

Features

- TTL logic output
- DIP-14 pin package compatible
- Tight stability (± 10 ppm)
- Enable/Disable feature

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating
Supply voltage	V_{CC}	-0.5 to +7.0 V
Input voltage	V_{IN}	-0.5 to $V_{CC}+0.5$ V
Output voltage	V_O	-0.5 to $V_{CC}+0.5$ V
Input current	I_{IN}	± 10 mA
Output current	I_O	± 25 mA
Storage temperature	T_{stg}	-40 to +80 °C

Parameter		TCO-743TH7	Conditions
Frequency	f_o	1.5 to 60 MHz	
Frequency Stability	$\Delta f/f_o$	± 10 ppm max.	(*1)
Operating Temperature	T_{opr}	0 °C to +70 °C	
Supply Voltage	V_{CC}	+5.0 V ± 10 %	DC
Supply Current	I_{CC}	See Table A (max.)	$V_{CC}=+5.5V$
Input Voltage	V_{IH} V_{IL}	$V_{IH}=+3.5$ V min. / $V_{IL}=+1.5$ V max.	#1: V_{IH} or OPEN ... Enable #1: V_{IL} or GND ... Disable
Output Voltage	V_{OH} V_{OL}	$V_{OH}=+4.0$ V min. / $V_{OL}=+0.4$ V max.	$I_{OH}=-4mA$, $I_{OL}=+16mA$
Symmetry	SYM	45 to 55 %	at +1.4V
Rise/Fall time	t_r/t_f	See Table A (max.)	at +0.4 to +2.4V
Fanout	n	10 max.	1.6mA/gate
Start-up time	t_{st}	4 ms max. 10 ms max.	1.5 $\leq f_o \leq 26$ MHz (*2) 26 < $f_o \leq 60$ MHz (*2)

*1 Inclusive of calibration tolerance at +25°C, operating temperature.

*2 Rise time (0 to +4.5V) of $V_{CC} > 150\mu s$

Package Outlines [Dimensions in mm]

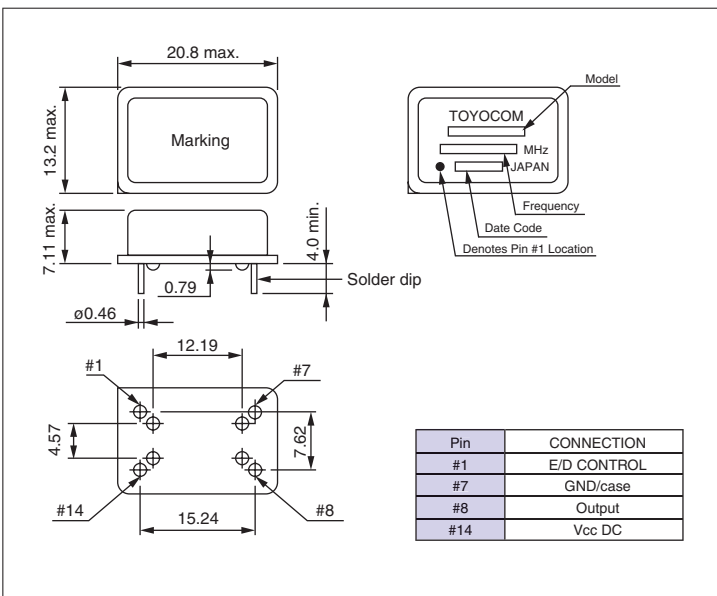


Table A

Freq. (MHz)	1.5 $\leq f_o$ $f_o \leq 10$	10 < f_o $f_o \leq 26$	26 < f_o $f_o \leq 60$
I_{CC} (mA)	15	20	40
t_r, t_f (ns)	5	5	5

Test Circuit

See Test Circuit page TEST-2