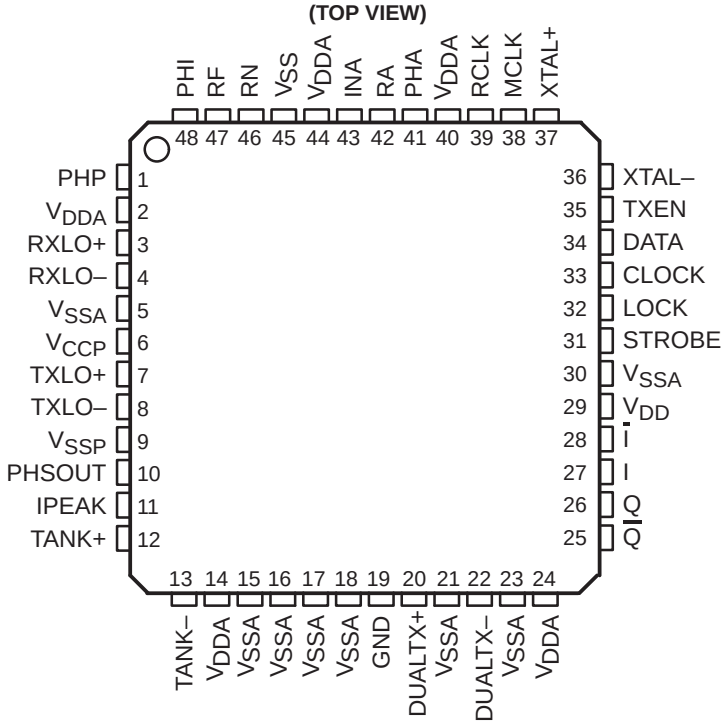
- 2-GHz Main Synthesizer, Which Incorporates a Dual-Mode 32/33 and 64/65 Prescaler for Fractional-N Operation
- 200-MHz Auxiliary Synthesizer, Which Incorporates an 8/9 Prescaler
- Separate Supply Terminals for Main and Auxiliary Charge Pumps
- Internal Compensation for Fractional Spurs
- Low Phase Noise
- Normal and Integral Charge Pump Outputs
- Fully Programmable Main and Auxiliary Dividers
- Serial Data Interface
- Direct I/Q Modulator
- Control Logic for Power-Down Modes
- Single-Sideband Suppressed Carrier (SSBSC) Converter to Generate TX Carrier
- 200-MHz TXIF Synthesizer and Oscillator
- Variable Gain Amplifier (VGA) With 50 dB of Dynamic Range
- 900-MHz Power Amplifier (PA) Driver With 9 dBm Typical Output Power
- Reference and Clock Buffers
- 158 mA Typical Total Operating Current at 3.75 V Supply
- 48-Pin Quad Flatpack (LQFP)

PT PACKAGE
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description

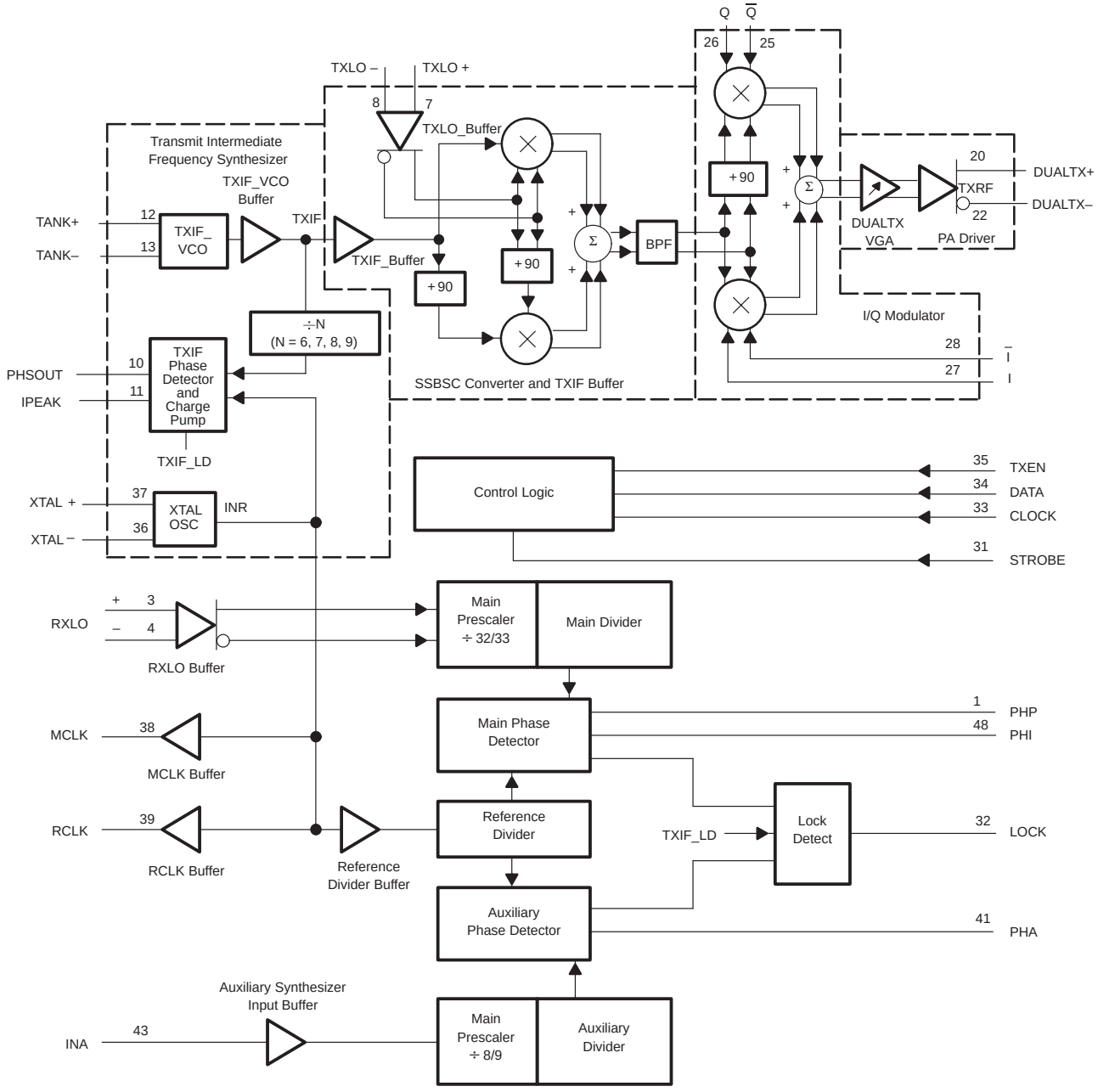
The TRF3040 is an integrated transmit modulator/synthesizer circuit suitable for 900-MHz analog and digital cellular telephones. It consists of a transmit intermediate frequency (TXIF) synthesizer and oscillator, a single-sideband suppressed carrier (SSBSC) converter, a direct conversion I/Q modulator, a variable gain amplifier (VGA) with a power amplifier (PA) driver, a main channel fractional-N synthesizer, an auxiliary channel synthesizer, a crystal oscillator reference buffer, and clock buffers in a small surface-mount package. Very few external components are required.

The TXIF synthesizer produces the offset signal, TXIF, needed to translate the external local oscillator (TXLO) signal to the correct transmission frequency. The TXIF_VCO (voltage controlled oscillator) can operate from 90 MHz to 200 MHz, depending on the component values chosen for the external tank circuit. The TXLO signal may be differential or single-ended input.

The direct conversion I/Q modulator places the modulation signal (π/4-DQPSK, FM) directly on top of the transmit carrier frequency.

The VGA has an output range of –41 dBm to 9 dBm into a 200-Ω differential load. The balanced output signal simplifies the board layout making it easier to meet isolation requirements.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLOCK	33	I	Serial clock input
DATA	34	I	Serial data input
DUALTX+	20†	O	Differential RF power amplifier driver
DUALTX–	22†	O	Differential RF power amplifier driver
GND	19		Substrate (GND)
$\overline{I}$	28	I	Baseband inverting in-phase modulation input
I	27	I	Baseband noninverting in-phase modulation input
INA	43	I	Auxiliary synthesizer input
IPEAK	11		TX offset loop charge pump current setting resistor
LOCK	32	O	Lock detect output
MCLK	38†	O	Buffered master clock output
PHA	41	O	Auxiliary charge pump output
PHI	48†	O	Main charge pump integral output
PHP	1	O	Main charge pump proportional output
PHSOUT	10	O	TX offset charge pump output
Q	25	I	Baseband inverting quadrature modulation input
Q	26	I	Baseband noninverting quadrature modulation input
RA	42		Auxiliary charge pump current setting resistor
RCLK	39†	O	Buffered reference clock output
RF	47		Fractional compensation charge pump current setting resistor
RN	46		Main charge pump current setting resistor
RXLO+	3	I	Differential main synthesizer positive input
RXLO–	4	I	Differential main synthesizer negative input
STROBE	31	I	Data strobe input
TANK+	12	I	Differential TXIF_VCO tank positive input
TANK–	13	I	Differential TXIF_VCO tank negative input
TXEN	35	I	Transmit enable
TXLO+	7	I	Differential transmit LO positive input
TXLO–	8	I	Differential transmit LO negative input
V_{CCP}	6		Main charge pump and bandgap supply voltage
V_{DD}	29		Digital supply voltage
V_{DDA}	2		Main prescaler and bandgap supply voltage
	14		TX offset loop supply voltage
	24†		RF modulator supply voltage
	40		Oscillator and buffers supply voltage
	44		Auxiliary charge pump supply voltage
V_{SSA}	17, 18		RF modulator ground
	5		Main prescaler and bandgap ground
	15		TX offset loop ground
	16		TX offset loop and charge pump ground
	21, 23		PA driver ground
	30		Oscillator, MCLK, and RCLK ground
V_{SS}	45		Digital ground
V_{SSP}	9		Main charge pump ground
XTAL+	37	I	Crystal oscillator base input
XTAL–	36	O	Crystal oscillator emitter input

† Pins have limited ESD protection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Power supply voltage range , V_{CCP}, V_{DD}, V_{DDA} (see Note 1) . . . . . –0.3 V to 4.5 V
Voltage applied to any other terminal, V_{IN} . . . . . –0.3 V to V_{CC}/V_{DD} + 0.3 V
Operation junction temperature, T_{Jmax} . . . . . 150°C
Operating temperature, T_A . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device, at these or any other conditions beyond those indicated under “recommended operating conditions”, is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are in respect to V_{SSA} ($V_{SSA} = V_{SSP} = V_{SS}$ = GND)

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CCP}, V_{DD}, V_{DDA}	3.6	3.75	3.9	V
High-level input voltage, V_{IH} (CLOCK, DATA, STROBE, TXEN)	$0.7\times V_{DD}$		$V_{DD}+0.3$	V
Low-level input voltage, V_{IL} (CLOCK, DATA, STROBE, TXEN)	–0.3		$0.3\times V_{DD}$	V
Main synthesizer input frequency, $f_{IN(RXLO\pm)}$			2000	MHz
Main synthesizer input power, $P_{IN(RXLO\pm)}$, (AC coupled, 50-Ω single ended, 100-Ω differential)		–17		dBm
Transmit LO input frequency, $f_{IN(TXLO\pm)}$			1050	MHz
Transmit LO input power, $P_{IN(TXLO\pm)}$, (AC coupled, 50-Ω single ended, 100-Ω differential)		–10		dBm
TXIF_VCO tank differential input frequency, $f_{IN(TANK\pm)}$			200	MHz
Crystal oscillator input frequency, $f_{IN(XTAL+)}$			25	MHz
Auxiliary synthesizer input frequency, $f_{IN(INA)}$			200	MHz
Auxiliary synthesizer input voltage, $V_{IN(INA)}$, (AC coupled)	0.2			V_{PP}
In-phase differential input, I/$\overline{I}$ (quiescent)		$V_{DDA}/2$		V
Quadraphase differential input, Q/$\overline{Q}$ (quiescent)		$V_{DDA}/2$		V
Operating free-air temperature, T_A	–40	25	85	°C

dc electrical characteristics $V_{CCP} = V_{DD} = V_{DDA}$ = 3.75 V, T_A = 25°C (unless otherwise noted)

supply current I = $I_{CCP} + I_{DD} + I_{DDA}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SLEEP}	Sleep mode supply current			2	3	mA
$I_{STANDBY}$	Standby mode supply current			22		mA
I_{OPER_ANA}	Operating supply current – full power analog mode (MODE=0)			142		mA
I_{OPER_DIG}	Operating supply current – full power digital mode (MODE=1)			158		mA

dc electrical characteristics $V_{CCP} = V_{DD} = V_{DDA}$ = 3.75 V, T_A = 25°C (unless otherwise noted) (continued)

digital interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output voltage, low	I_O = 1 µA			0.050	V
		I_O = 2 mA			0.4	V
V_{OH}	Output voltage, high	I_O = –1 µA	V_{DD} – 0.050			V
		I_O = –2 mA	V_{DD} – 0.4			V

charge pump PHA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHA}	Output current at PHA	R_A = 100 kΩ, $V_{PHA} = V_{DDA}/2$	200	250	300	μA
$\frac{\Delta I_{PHA}}{\lvert I_{PHA}\rvert}$	Relative output current variation (see Figure 1)			2%	10%	
ΔI_{PHA}	Output current matching PHA (see Figure 1)				10%	

charge pump PHP, normal mode, $V_{RF} = V_{DDA}$ (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHP}	Output current at PHP	CN = 128, $V_{PHP} = V_{DDA}/2$, RN = 120 kΩ	±250	±288	±320	μA
$\frac{\Delta I_{PHP}}{\lvert I_{PHP}\rvert}$	Relative output current variation (see Figure 1)			2%	10%	
ΔI_{PHP}	Output current matching PHP (see Figure 1)				10%	

NOTE 2: When a serial input word A is programmed, the main charge pump on the PHP and PHI is in the speed-up mode as long as STROBE is high in standard programming or until the speed-up mode counter reaches its terminal count. When this is not the case, the main charge pumps are in normal mode.

charge pump PHP, speed-up mode, $V_{RF} = V_{DDA}$ (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHP}	Output current at PHP	CN = 128, $V_{PHP} = V_{DDA}/2$, RN = 120 kΩ	±1.2	±1.6	±1.9	mA
$\frac{\Delta I_{PHP}}{\lvert I_{PHP}\rvert}$	Relative output current variation (see Figure 1)			2%	10%	
ΔI_{PHP}	Output current matching PHP (see Figure 1)				10%	

NOTE 2: When a serial input word A is programmed, the main charge pump on the PHP and PHI is in the speed-up mode as long as STROBE is high in standard programming or until the speed-up mode counter reaches its terminal count. When this is not the case, the main charge pumps are in normal mode.

charge pump PHI, speed-up mode, $V_{RF} = V_{DDA}$ (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PHI}	Output current at PHI	CN = 128, RN = 120 kΩ, CK = 3, $V_{PHA} = V_{DDA}/2$, CL = 1	±3.3	±4	±4.5	mA
$\frac{\Delta I_{PHI}}{\lvert I_{PHI}\rvert}$	Relative output current variation (see Figure 1)			2%	10%	
ΔI_{PHI}	Output current matching PHI (see Figure 1)				10%	

NOTE 2: When a serial input word A is programmed, the main charge pump on the PHP and PHI is in the speed-up mode as long as STROBE is high in standard programming or until the speed-up mode counter reaches its terminal count. When this is not the case, the main charge pumps are in normal mode.

dc electrical characteristics V_{CCP} = V_{DD} = V_{DDA} = 3.75 V, T_A = 25°C (unless otherwise noted) (continued)

fractional compensation PHP, normal mode, V_{RN} = V_{DDA} (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{PHP–FR}$	Output current PHP vs. fractional numerator	FMOD = 1, CN = 128, CK = 3,	RF = 120 kΩ, V_{PHP} = V_{DDA}/2, CL = 1	–340	–270	–170	nA
$\frac{\Delta I_{PHP–FR}}{\lvert I_{PHP–FR}\rvert}$	Relative output current (see Figure 1)					10%	

NOTE 2: When a serial input word A is programmed, the main charge pump on the PHP and PHI is in the speed-up mode as long as STROBE is high in standard programming or until the speed-up mode counter reaches its terminal count. When this is not the case, the main charge pumps are in normal mode.

fractional compensation PHP, speed-up mode, V_{RN} = V_{DDA} (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{PHP–FR}$	Output current PHP vs. fractional numerator	FMOD = 1, CN = 128, CK = 3,	RF = 120 kΩ, V_{PHP} =V_{DDA}/2, CL = 1	–1.7	–1.4	–1.1	µA
$\frac{\Delta I_{PHP–FR}}{\lvert I_{PHP–FR}\rvert}$	Relative output current (see Figure 1)					15%	

NOTE 2: When a serial input word A is programmed, the main charge pump on the PHP and PHI is in the speed-up mode as long as STROBE is high in standard programming or until the speed-up mode counter reaches its terminal count. When this is not the case, the main charge pumps are in normal mode.

fractional compensation PHI, speed-up mode, V_{RN} = V_{DDA} (see Note 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{PHI–FR}$	Output current PHI vs. fractional numerator	FMOD = 1, CN = 128, CK = 3,	RF = 120 kΩ, V_{PHI} = V_{DDA}/2, CL = 1	–5.1	–4	–2.9	µA
$\frac{\Delta I_{PHI–FR}}{\lvert I_{PHI–FR}\rvert}$	Relative output current (see Figure 1)					15%	

NOTE 2: When a serial input word A is programmed, the main charge pump on the PHP and PHI is in the speed-up mode as long as STROBE is high in standard programming or until the speed-up mode counter reaches its terminal count. When this is not the case, the main charge pumps are in normal mode.

charge pump leakage currents

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{PHI}	Output leakage current PHI	V_{RF} = V_{RN} = V_{DDA},	V_{PHP} = 0 to V_{DDA}		±0.1	±10	nA
I_{PHA}	Output leakage current PHA				±0.1	±10	nA

ac electrical characteristics V_{CCP} = V_{DD} = V_{DDA} = 3.75 V, T_A = 25°C (unless otherwise noted)

transmit intermediate frequency synthesizer, SSBSC converter and I/Q modulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TXLO±	Transmit LO input frequency		900		1100	MHz
TXLO±	Transmit LO input power	AC coupled; 50-Ω single-ended, 100-Ω differential	–13	–10		dBm
TANK±	TXIF_VCO tank differential input frequency range			155		MHz
PHSOUT	TXIF_PD charge pump output level		0.5		V_{DDA}–0.5	V
IPEAK	TXIF_PD charge pump current setting	R_{IPEAK} = 13 kΩ		2.3		mA
Kϕ	TXIF_PD phase gain	PLL in phase lock		1.46		mA/rad
XTAL+	XTAL oscillator input frequency		15		25	MHz
	XTAL negative resistance	With external capacitors		–100		Ω
RCLK, MCLK	Frequency range	RCLK, MCLK load circuit		20		MHz
	Output levels		0.7	1	1.4	V_{PP}
	Harmonic content		10			dBc
I/$\bar{I}$, Q/$\overline{Q}$	Differential input frequency				1.8	MHz
	Differential modulation level		0.8	0.9	1.0	V_{PEAK}
	Differential input impedance		10			kΩ
	DC bias point		1.65	1.7	2.0	V
TXRF	TX operating frequency range		820		920	MHz
DUALTX±	RF output frequency	SE = 1, TXEN = 1, AMPS/DAMPS	820		853	MHz
	Output power (I/Q set to typical conditions)	Open collector, matched to 200 Ω differential impedance		9		dBm
	Gain flatness			1		dB
	Linearity in DAMPS mode (I/Q in phase, levels set to nominal conditions Pout set to 8 dBm)	3rd order	33	36		dBc
		5th order	45	62		dBc
		7th order	53	70		dBc
	Carrier suppression, I & Q in quadrature	VGA set to Pout = 8 dBm	26	40		dBc
		VGA set to Pout = –38 dBm		33		
	Sideband suppression, I & Q in quadrature		25	43		dBc
	Adjacent channel noise power	Ar 30 kHz offset		–95		dBc/Hz
	Alternate channel noise power	At 60 kHz offset		–101		dBc/Hz
	TXLO conversion products (see Note 3)	TXLO	21	33		dBc
		Upper sideband	21	60		
		TXLO –2×TXIF	15			
		TXLO ±3×TXIF	36			
		Harmonics ≤ 10th	21			
	Broadband noise (0-dB VGA or 9-dBm output, whichever is less	869 to 894 MHz		–124		dBc/Hz

NOTE 3: Parameters may vary depending on external output matching circuit.

ac electrical characteristics V_{CCP} = V_{DD} = V_{DDA} = 3.75 V, T_A = 25°C (unless otherwise noted) (continued)

frequency synthesizers

main divider

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXLO±	Main synthesizer input frequency				2000	MHz
RXLO±	Main synthesizer input power	AC coupled, external shunt 50-Ω single-ended, 100 Ω differential		–17		dBm
RXLO±	Main synthesizer input harmonics and subharmonics	No multiclocking	30			dBc

reference divider

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INR	Operating frequency				25	MHz
	Harmonics	No multiclocking	10			dBc

auxiliary divider

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INA	Auxiliary synthesizer input frequency		No multiclocking		110		MHz
	Auxiliary synthesizer input signal amplitude			0.2			V_{PP}
	Auxiliary synthesizer input harmonics			10			dBc
Z_{INA}	Auxiliary synthesizer input impedance	Resistance		5	100		kΩ
		Capacitance				3	pF

timing requirements, serial data interface (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA	Serial data input rate				10	MHz
CLOCK	Serial data clock input				10	MHz
STROBE	Serial data strobe input			10		
TXEN	Transmit enable	Transmit enable		TXEN=1		Logic
		Transmit disable		TXEN=0		
t_{su}	Setup time: Data to CLOCK, CLOCK to STROBE		30			ns
t_k	Hold time. CLOCK to DATA		30			ns
t_{sw}	Pulse width	CLOCK	30			ns
		STROBE (B-G words)	100			
		A-word, PR = 01	$1/f_{VCO} \times (NM2 \times 65) + t_W$			
		A-word, PR = 10	$1/f_{VCO} \times (NM2 \times 65) + (NM3+1) \times 72) + t_W$			

PARAMETER MEASUREMENT INFORMATION

charge-pump current output definitions

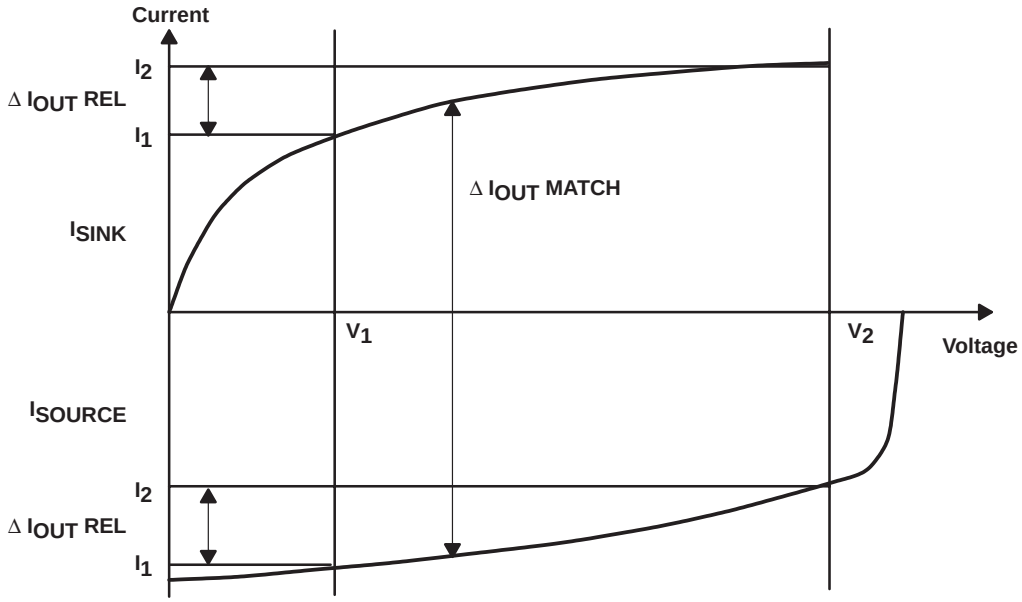


Figure 1. Charge-Pump Output Current Definitions

The relative output current variation is defined as the percent difference between charge-pump current output at two charge-pump output voltages and the mean charge-pump current output (see Figure 1):

$$\frac{\Delta I_{OUT\ REL}}{\left|I_{OUT\ MEAN}\right|} = 2 \times \frac{\left(I_2 - I_1\right)}{\left|\left(I_2 + I_1\right)\right|} \times 100\%;\ \text{with}\ V_1 = 0.7\ V,\ V_2 = V_{DDA} - 0.8\ V.$$

Output current matching is defined as the difference between charge-pump sinking current output and charge-pump sourcing current output at a given charge-pump output (see Figure 1).

$\Delta I_{OUT\ MATCH} = I_{SINK} - I_{SOURCE}$; with $V_1 \le \text{Voltage} \le V_2$.

APPLICATION INFORMATION

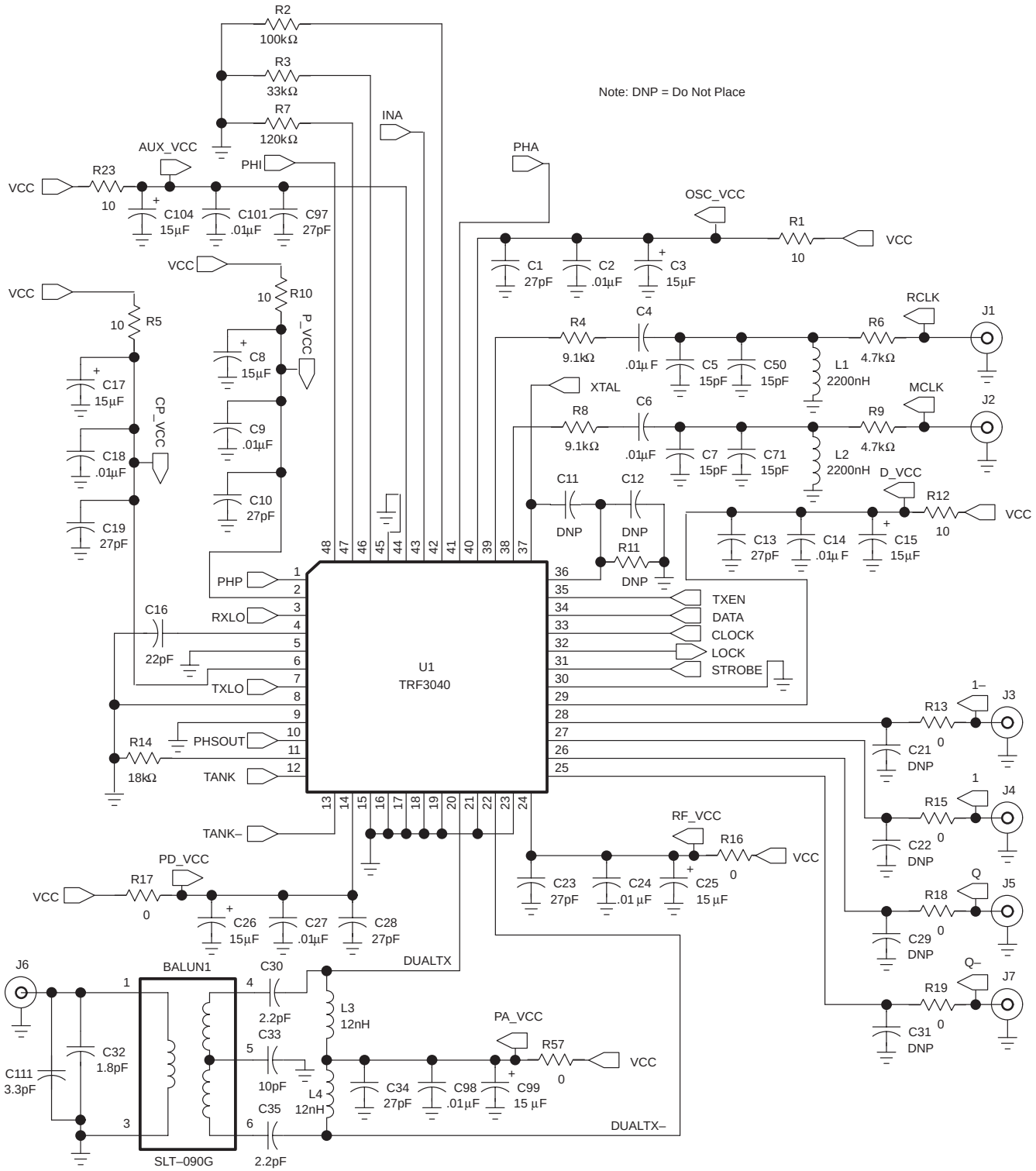


Figure 2. Evaluation Board Schematic

APPLICATION INFORMATION

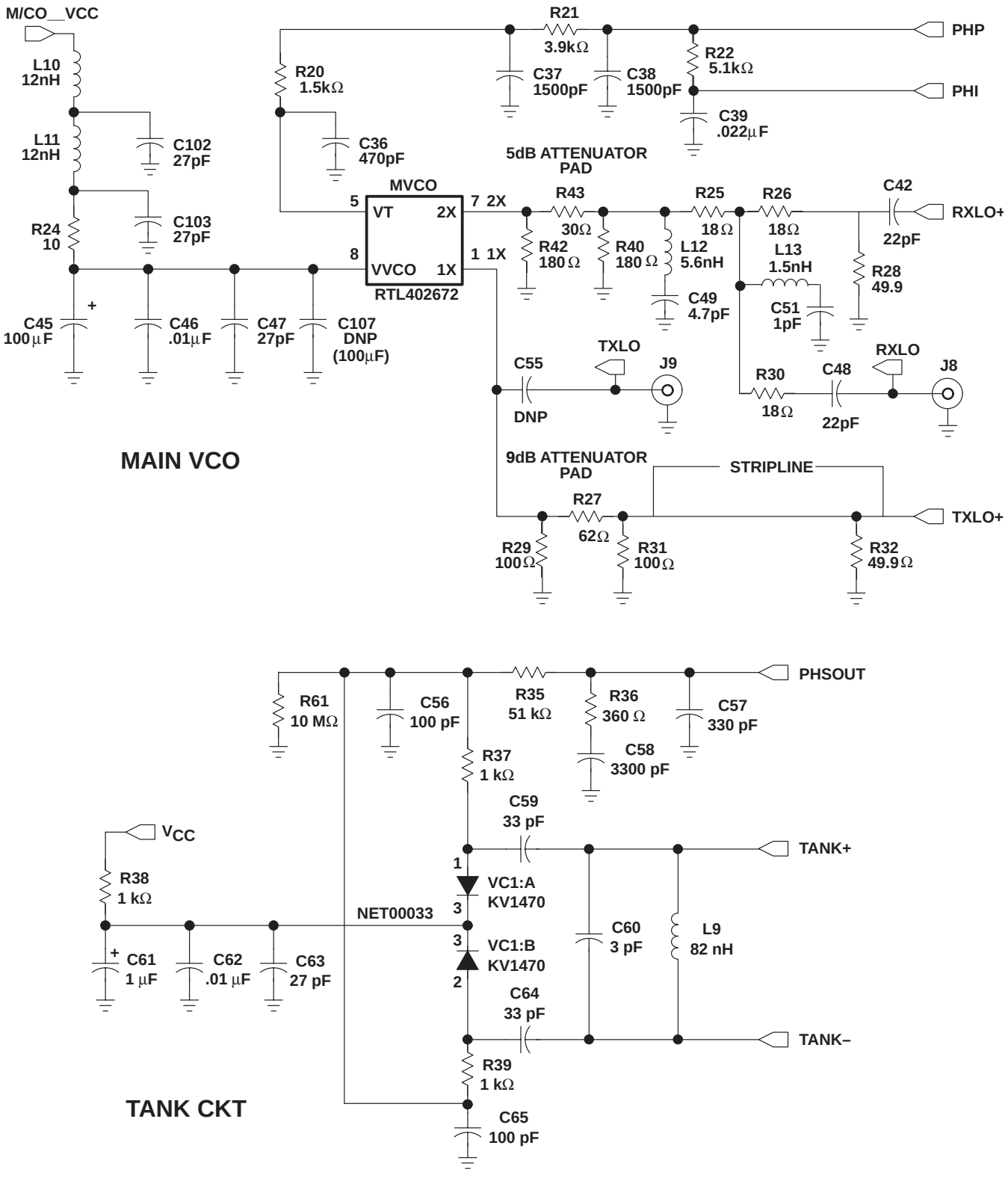


Figure 2. Evaluation Board Schematic (continued)

APPLICATION INFORMATION

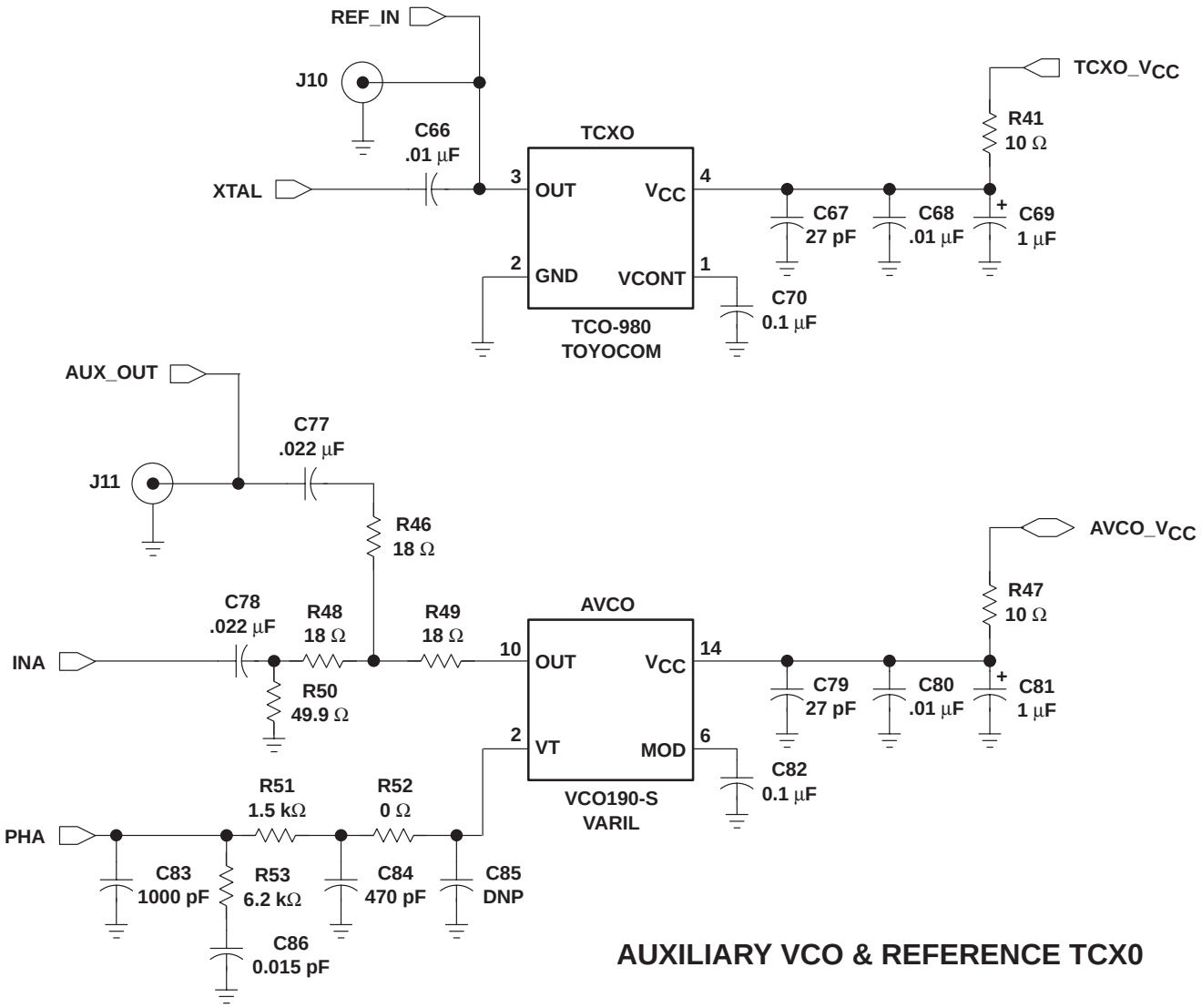


Figure 2. Evaluation Board Schematic (continued)

APPLICATION INFORMATION

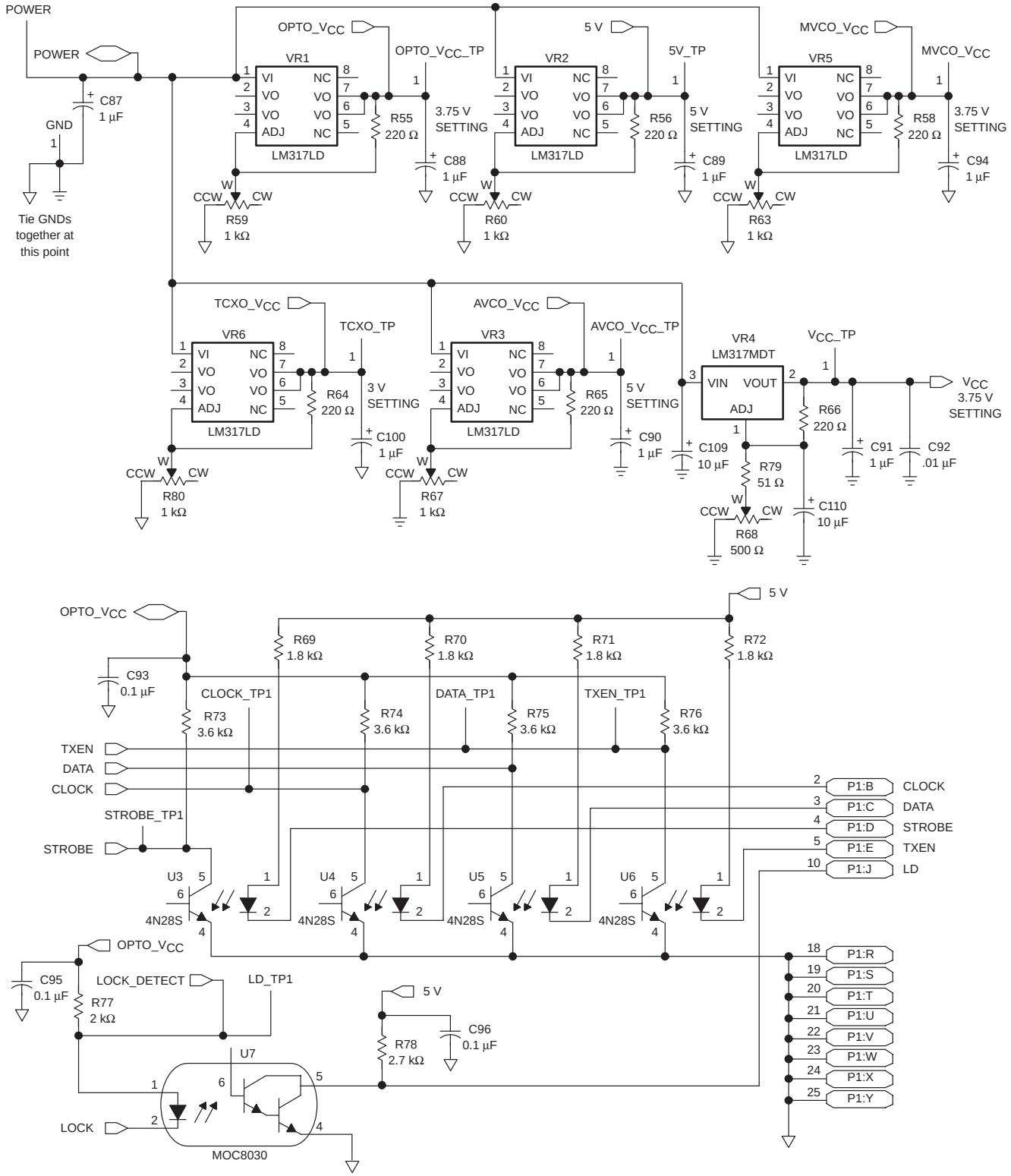


Figure 2. Evaluation Board Schematic
(PC Interface and Evaluation Board DC Supply Circuitry Only) (continued)

APPLICATION INFORMATION

Table 1. TRF3040 Evaluation Board Parts List

DESIGNATORS	DESCRIPTION	VALUE	QTY	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
C 1, 10, 13, 19, 23, 28, 34, 47, 63, 67,79, 97, 102, 103	Capacitor	27 pF	14	0603	Murata	GRM39COG series
C 2, 4, 6, 9, 14, 18, 24, 27,46, 62, 66, 68, 80, 92, 98, 101	Capacitor	0.01 µF	16	0603	Murata	GRM39COG series
C 3, 8, 15, 17, 25, 26, 99, 104	Tantalum capacitor	15 µF	8	6032–C	Venkel	TA010TCM series
C 5, 7, 50, 71	Capacitor	15 pF	4	0603	Murata	GRM39COG series
C 11, 12, 21, 22, 29, 31, 55, 85, 107	Capacitor	DNP	9			
C 16, 42, 48	Capacitor	22 pF	3	0402	Murata	GRM39COG series
C 30, 35	Capacitor	2.2 pF	2	0603	Murata	GRM39COG series
C 32	Capacitor	1.8 pF	1	0603	Murata	GRM39COG series
C 33	Capacitor	10 pF	1	0603	Murata	GRM39COG series
C 36, 84	Capacitor	470 pF	2	0603	Murata	GRM39COG series
C 37, 38	Capacitor	1500 pF	2	0603	Murata	GRM39COG series
C 39, 77, 78	Capacitor	0.022 µF	3	0603	Murata	GRM39COG series
C 45	Tantalum capacitor	100 µF	1	6032-C	Venkel	TA010TCM series
C 49, C51	Capacitor	3.9 pF	1	0603	Murata	GRM39COG series
C 55	Capacitor	DNP	1	0402		
C 56, 65	Capacitor	100 pF	2	0603	Murata	GRM39COG series
C 57	Capacitor	330 pF	1	0603	Murata	GRM39COG series
C 58	Capacitor	3300 pF	1	0603	Murata	GRM39COG series
C 59, 64	Capacitor	33 pF	2	0603	Murata	GRM39COG series
C 60	Capacitor	3 pF	1	0603	Panasonic	ECU-V1 series
C 61, 69, 81, 87, 88, 89, 90, 91, 94, 100	Tantalum capacitor	1 µF	10	3216-A	Venkel	TA010TCM series
C 70, 82, 93, 95, 96	Capacitor	0.1 µF	5	0603	Murata	GRM39COG series
C 83	Capacitor	1000 pF	1	0603	Murata	GRM39COG series
C 86	Capacitor	0.015 µF	1	0603	Murata	GRM39COG series
C 109, 110	Tantalum capacitor	10 µF	2	3216-A	Venkel	TA010TCM series
C 111	Capacitor	3.3 pF	1	0603	Murata	GRM39COG series
J 8	SMA-V		1		EF Johnson	142-0701-201
L 1, 2	Inductor	2200 nH	2	1008	Coilcraft	0603HS series
L 3, 4, 10, 11	Inductor	12 nH	4	0603	Coilcraft	0603HS series
L 12, 13	Inductor	4.7 nH	1	0603	Coilcraft	0603HS series
L 9	Inductor	82 nH	1	0603	Coilcraft	0603HS series
R 1, 5, 10, 12, 23, 24, 41, 47	Resistor	10	8	0603	Panasonic	ERJ-3GSYJ series
R 2	Resistor	100K	1	0603	Panasonic	ERJ-3GSYJ series
R 3	Resistor	33K	1	0603	Panasonic	ERJ-3GSYJ series
R 4, 8	Resistor	9.1K	2	0603	Panasonic	ERJ-3GSYJ series
R 6, 9	Resistor	4.7K	2	0603	Panasonic	ERJ-3GSYJ series
R 7	Resistor	120K	1	0603	Panasonic	ERJ-3GSYJ series
R 11	Resistor	DNP	1	0603	Panasonic	ERJ-3GSYJ series

APPLICATION INFORMATION

Table 1. TRF3040 Evaluation Board Parts List (continued)

DESIGNATORS	DESCRIPTION	VALUE	QTY	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
R 13, 15, 16, 17, 18, 19, 52, 57	Resistor	0	8	0603	Panasonic	ERJ-3GSYJ series
R 14	Resistor	18K	1	0603	Panasonic	ERS-36SYJ series
R 20, 51	Resistor	1.5K	2	0603	Panasonic	ERJ-3GSYJ series
R 22	Resistor	5.1K	1	0603	Panasonic	ERJ-3GSYJ series
R 25, 26, 30	Resistor	18	3	0402	Panasonic	ERJ-2GEJ series
R 27	Resistor	62	1	0402	Panasonic	ERJ-2GEJ series
R 28, 32	Resistor	49.9	2	0402	Panasonic	ERJ-2GEJ series
R 29, 31	Resistor	100	2	0402	Panasonic	ERJ-2GEJ series
R 40, 42	Resistor	430	2	0402	Panasonic	ERJ-2GEJ series
R 46, 48, 49	Resistor	18	3	0603	Panasonic	ERJ-3GSYJ series
R 50	Resistor	49.9	1	0603	Panasonic	ERJ-3GSYJ series
R 35, 79	Resistor	51	2	0603	Panasonic	ERJ-3GSYJ series
R 36	Resistor	360	1	0603	Panasonic	ERJ-3GSYJ series
R 37, 38, 39	Resistor	1K	3	0603	Panasonic	ERJ-3GSYJ series
R 43	Resistor	10	1	0402	Panasonic	ERJ-2GEJ series
R 53	Resistor	6.2K	1	0603	Panasonic	ERJ-3GSYJ series
R 55, 56, 58, 64, 65, 66	Resistor	220	6	0603	Panasonic	ERJ-3GSYJ series
R 59, 60, 63, 67, 80	Trimpot	1K	5	3313J	Bourns	3313J-1-102E
R 61	Resistor	10M	1	0805	Panasonic	ERJ-3GSYJ series
R 68	Trimpot	500	1	3313J	Bourns	3313J-1-102E
R 69, 70, 71, 72	Resistor	1.8K	4	0603	Panasonic	ERJ-3GSYJ series
R 73, 74, 75, 76	Resistor	3.6K	4	0603	Panasonic	ERJ-3GSYJ series
R 77	Resistor	2K	1	0603	Panasonic	ERJ-3GSYJ series
R 78	Resistor	2.7K	1	0603	Panasonic	ERJ-3GSYJ series
U 1	Integrated circuit		1		Texas Instruments	TRF3040
U 3, 4, 5, 6	Opto-coupler		4		Motorola	4N28S
U 7	Opto-coupler		1		Motorola	MOC8030
VC 1	Varactor		1		Toko	KV1470
VR 1, 2, 3, 5, 6	Voltage regulator		5		Motorola	LM317LD
VR 4	Voltage regulator		1		Motorola	LM317MDT
BALUN 1	Transformer	4:1	1		Hitachi	SLT-090G
P 1	DB25M		1		AMP	747238-4
J 1, 2, 6, 9, 10, 11	SMA_H		7		EF Johnson	142-0701-831
J 3, 4, 5, 7	BNC-90		4		AMP	413631-1
MVCO	Voltage-controlled oscillator		1		Panasonic	RTL402672
AVCO	Voltage-controlled oscillator		1		Vari–L	VCO190-S

APPLICATION INFORMATION

Table 1. TRF3040 Evaluation Board Parts List (continued)

DESIGNATORS	DESCRIPTION	VALUE	QTY	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
TCXO	Temperature-Compensated Crystal Oscillator		1		Toyocom	TCO-980 series
CLOCK_TP1 DATA_TP1 LD_TP1 TXEN_TP1 STROBE_TP1 MVCO_TP OPTO_VCC_TP +5V_TP AVCO_VCC_TP TXCO_TP VCC_TP POWER GND	Test probe connector		13		Components Corporation	TP-105-01 series

PRINCIPLES OF OPERATION

operational modes

The TRF3040 has two separate operational modes: an advanced mobile phone system (AMPS) mode, and a digital advanced mobile phone system (DAMPS) mode, both of which are selected based on which cellular system is in use. In addition, the TRF3040 can be operated in different power-saving mode settings. The power-saving modes disable the circuitry that is not in use at the time in order to reduce power consumption. During sleep mode, only the circuitry required to provide a master clock to the digital portion of the system is active. In standby mode, the main synthesizer, the auxiliary synthesizer, and the master clock circuitries are enabled. In transmit mode, all functions of the device are enabled. Table 2 describes the functions that are enabled during each mode, and Table 3 describes the related programming control bit(s).

Table 2. TRF3040 Power-Mode Function Usage

FUNCTION ENABLED	AMPS/DAMPS		
	SLEEP	STANDBY	TRANSMIT
Crystal oscillator	X	X	X
TXIF phase detector			X
÷ N			X
TXIF buffer			X
TXIF_VCO			X
TXIF_VCO buffer			X
SSCSB converter			X
MCLK buffer	X	X	X
RCLK buffer		X	X
TXLO buffer			X
RXLO buffer		X	X
I/Q modulator			X
DUALTX VGA			X
Control logic	X	X	X
Reference divider buffer		X	X
Auxiliary divider buffer		X	X
Main phase detector		X	X
Auxiliary phase detector		X	X
Lock detect		X	X

Table 3. TRF3040 Programming Power-Mode Function

FIELD BIT(S)	SLEEP	STANDBY	TRANSMIT
SM	0:on	1:off	1:off
SE	0:off	0:off	1:on
EA	0:off	1:on	1:on
EM	0:off	1:on	1:on

frequency synthesizer

The frequency synthesizer consists of the serial data interface, the main channel synthesizer, and the auxiliary synthesizer. Figure 3 illustrates the functionality of the frequency synthesizer.

PRINCIPLES OF OPERATION

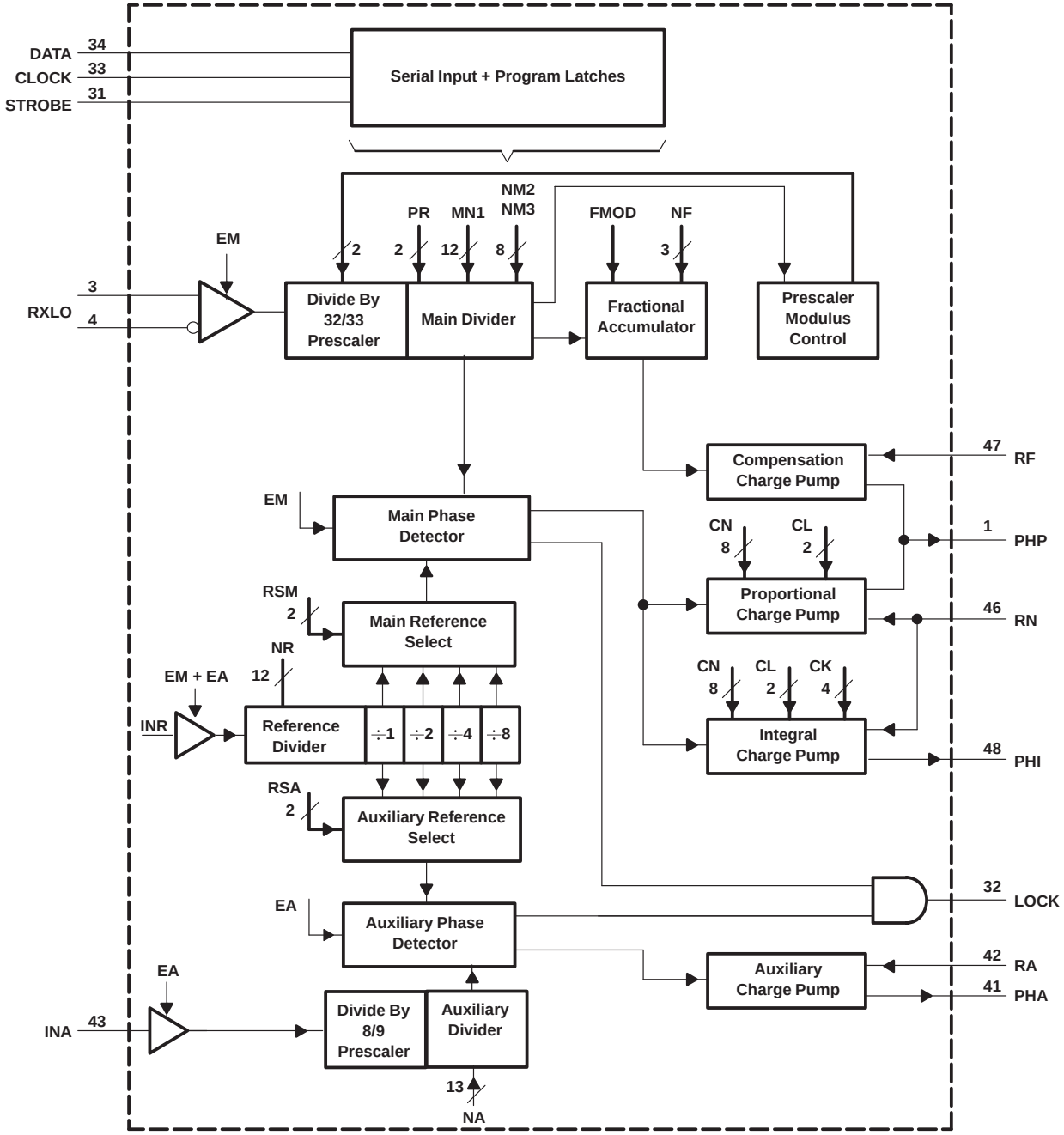


Figure 3. Frequency Synthesizer Functional Block Diagram

PRINCIPLES OF OPERATION

serial programming input

The TRF3040 operates using CLOCK, DATA, and STROBE pins of the serial data interface. The serial programming data is structured into 24-bit words, of which one or four bits are dedicated address bits.

Figure 4 shows the format and the content of each word. Table 4 lists the symbols, number of bits, and the function for each word used in the standard programming mode (ALT = 0). Similarly, the alternate programming mode (ALT = 1) is described in Figure 5 and Table 5.

Figure 6 shows the timing diagram for the serial input. When the STROBE goes low, the signal on the DATA input is clocked into a shift register on the positive edges of the CLOCK. When the STROBE goes high, depending on the 1 or 4 address bit(s), data is latched into different working or temporary registers. To fully program the modulator/synthesizer, five words must be sent: G, D, C, B, and A. The E-word is for testing purposes only.

The A-word contains new data for the main divider. The A-word is loaded into the working registers only when a main divider synchronization signal is active to avoid phase jumps when reprogramming the main divider.

The data for CN and PR is stored by the B-word in temporary registers. The data in these temporary registers is loaded into the work registers together with the A-word. This avoids false main-divider input when the A-word is loaded.

The value of the auxiliary divider ratio, NA, is defined by a 13-bit field, and the operational mode of the main synthesizer is determined by the least significant bit (LSB) of the C-word:

Standard mode: ALT = 0
Alternate mode: ALT = 1

The content of the D-word defines the operation of the reference divider. The OR function of bits EA and EM enables the buffer/amplifier input stage. The reference divider ratio is determined by the value of NR. The main and auxiliary synthesizer sections can individually select a reference postscaler division of 1, 2, 4, or 8 by selecting fields RSM and RSA, respectively.

The G-word programs all other functions: VGA power control, ÷ N (TXIF loop), SE (TXIF synthesizer loop enable), AMPS and DAMPS modes, and sleep mode.

The E-word is for testing purposes only and is reset when programming the D-word.

PRINCIPLES OF OPERATION

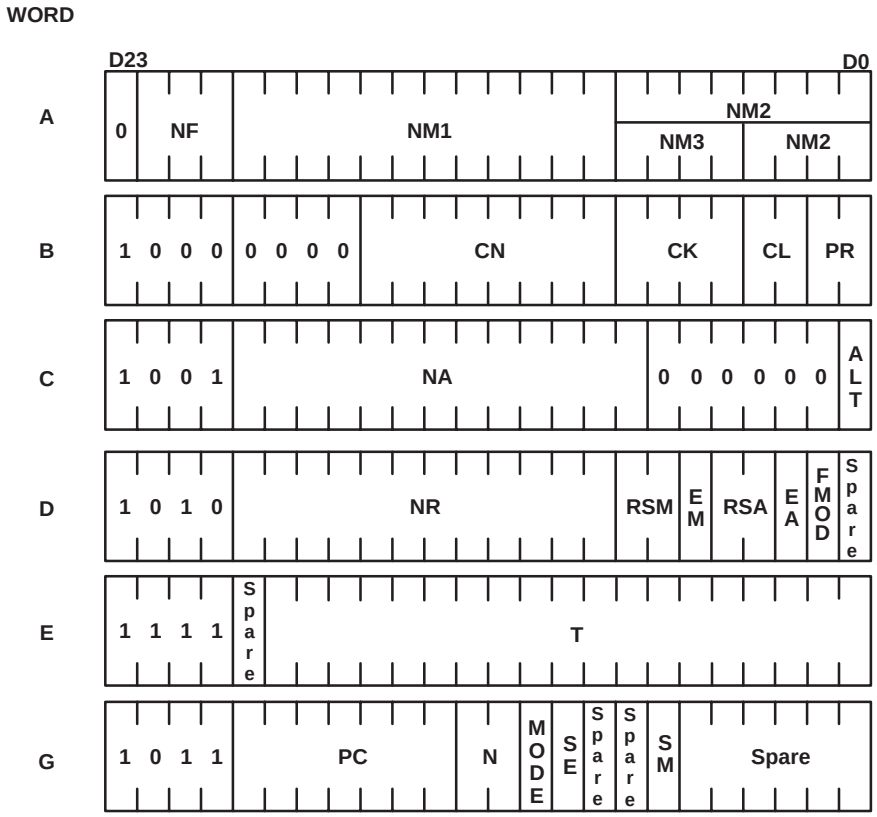


Figure 4. Serial Input Word Format (Standard Programming, ALT = 0)

PRINCIPLES OF OPERATION

Table 4. Standard Programming (ALT = 0) Function Table (see Notes 4 and 5)

SYMBOL	BITS	FUNCTION
NM1	12	Number of main divider cycles when the prescaler is programmed in ratio R1†
NM2	8 if PR = X1 4 if PR = X0	Number of main divider cycles when the prescaler is programmed in ratio R2†
NM3	4 if PR = X0 0 otherwise	Number of main divider cycles when the prescaler is programmed in ratio R3†
PR	2	Main synthesizer prescaler type in use: PR = X1: modulus 2 prescaler (64/65) PR = X0: modulus 3 prescaler (64/65/72)
NF	3	Main synthesizer fractional-N increment
FMOD	1	Main synthesizer fractional-N modulus selection flag: 1 = modulo 8 0 = modulo 5
CN	8	Current setting factor for main charge pumps
CL	2	Acceleration factor for proportional charge pump current
CK	4	Acceleration factor for integral charge pump current
EM	1	Main divider enable flag (see Table 11)
EA	1	Auxiliary divider enable flag (see Table 11)
RSM	2	Reference select for main phase detector
RSA	2	Reference select for auxiliary phase detector
NR	12	Reference divider ratio
NA	13	Auxiliary divider ratio
N	2	TXIF synthesizer divider ratio, ÷N, N = 6, 7, 8, 9 (see Note 6)
PC	7	Variable gain amplifier (VGA) power control function (see Table 14)
SE	1	TXIF synthesizer on/off. SE=1, TXIF synthesizer on; SE=0, TXIF synthesizer off
SM	1	Sleep mode bit; SM bit shuts down the synthesizers and the modulator section (see Table 3)
MODE	1	Mode control: MODE=1, digital (DAMPS); MODE=0, analog (AMPS) (see Note 7)
ALT	1	Alternate programming bit; ALT=0, standard (STD) mode; ALT=1, enhanced (ALT) mode (see Note 8)
T	19	Test mode connection of internal signals to lock pin: see *test modes* section

† Not including reset cycles and fractional-N effects. R1 = 64, R2 = 65, R3 = 72.

NOTES: 4. Data bits are shifted in on the leading clock edge, with the least significant bit (LSB) first in and the most significant bit (MSB) last.

5. On the rising edge of the strobe and with the address decoder output = 1, the contents of the input shift register are transferred to the working registers. The strobe rising edge comes one-half clock period after the clock edge on which the MSB of a word is shifted in.

6. Field bits setting for the TXIF synthesizer divider ratio

FIELD BIT		÷N
N1	N0	
0	0	6
0	1	7
1	0	8
1	1	9

7. The MODE bit allows a reduction in current for the DUALTX output driver while in AMPS mode.

8. The ALT programming bit allows the user to specify an enhanced programming scheme which allows for a fully programmable fractional modulus of 1 to 16 for the main synthesizer.

PRINCIPLES OF OPERATION

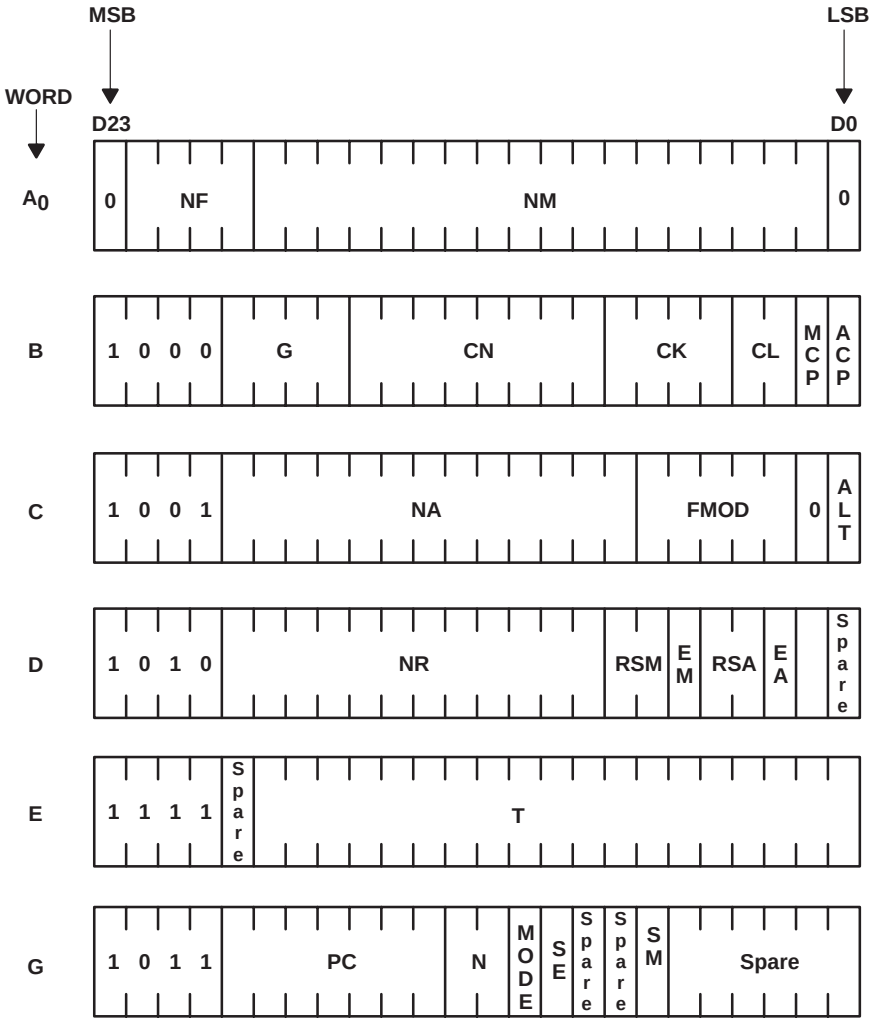


Figure 5. Serial Input Word Format (Alternate Programming, ALT = 1)

PRINCIPLES OF OPERATION

Table 5. Alternate Programming (ALT = 1) Function Table

SYMBOL	BITS	FUNCTION
NF	4	Main synthesizer fractional-N increment
NM	18	Overall main divider integer division ratio
CN	8	Binary current-setting factor for main charge pumps
G	4	Speed-up mode duration (number of reference divider cycles)
CK	4	Binary acceleration factor for integral charge pump current
CL	2	Binary acceleration factor for proportional charge pump current
MCP	1	Main charge pump polarity
ACP	1	Auxiliary charge polarity
NA	13	Auxiliary charge ratio
FMOD	5	Fraction accumulator modulus
NR	12	Reference divider ratio
RSM	2	Reference select for main phase detector
EM	1	Main divider enable flag (see Table 11)
RSA	2	Reference select for auxiliary phase detector
EA	1	Auxiliary divider enable flag (see Table 11)
N	2	TXIF synthesizer divider ratio, ÷N, N = 6, 7, 8, 9
PC	7	Variable gain amplifier (VGA) power control function (see Table 14)
SE	1	TXIF synthesizer on/off. SE=1, TXIF synthesizer on; SE=0, TXIF synthesizer off
SM	1	Sleep mode bit: SM bit shuts down the synthesizers and the modulator section (see Table 3)
MODE	1	Mode control: mode=1, digital (DAMPS); mode=0, analog (AMPS)
ALT	1	Alternate programming bit: ALT=0, standard (STD) mode; ALT=1, enhanced (ALT) mode
T	19	Test mode connection of internal signals to LOCK pin (see *test modes* section)

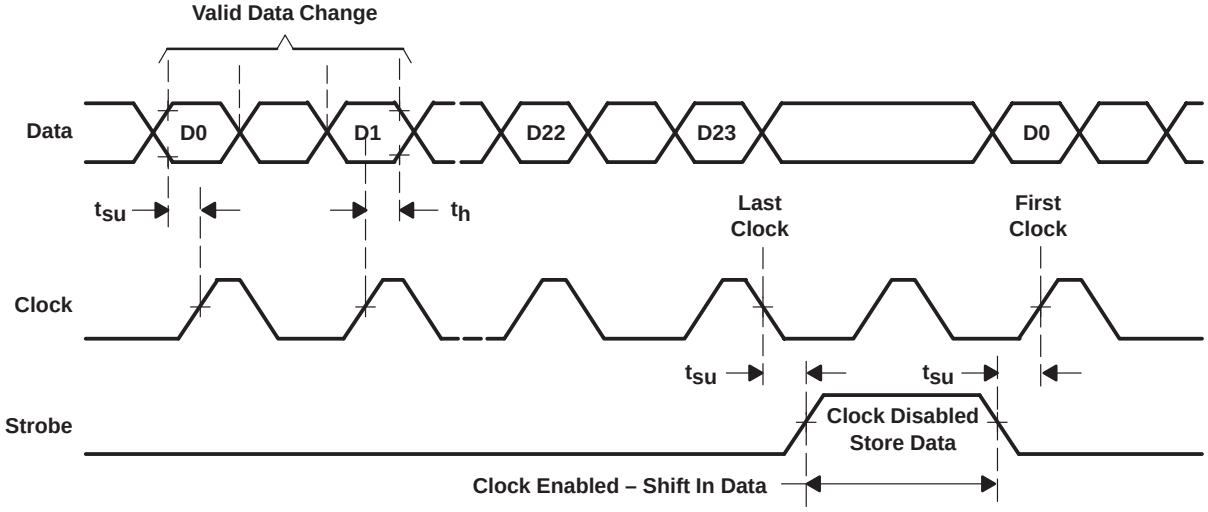


Figure 6. Serial Input Timing Sequence

PRINCIPLES OF OPERATION

reference variable divider

The internal reference signal INR, which is generated by the external crystal oscillator, is amplified to logic level by a single-ended input buffer. The OR function of the serial input bits EM an EA enables this input buffer. Subsequently, the output of the input buffer feeds the reference divider which consists of a 12-bit programmable divide-by-NR (NR = 4 to 4095) and a four-section postscaler. The main and auxiliary synthesizer sections can individually select a reference postscaler division of 1, 2, 4, or 8 by selecting RSM and RSA, respectively, as shown in Figure 7.

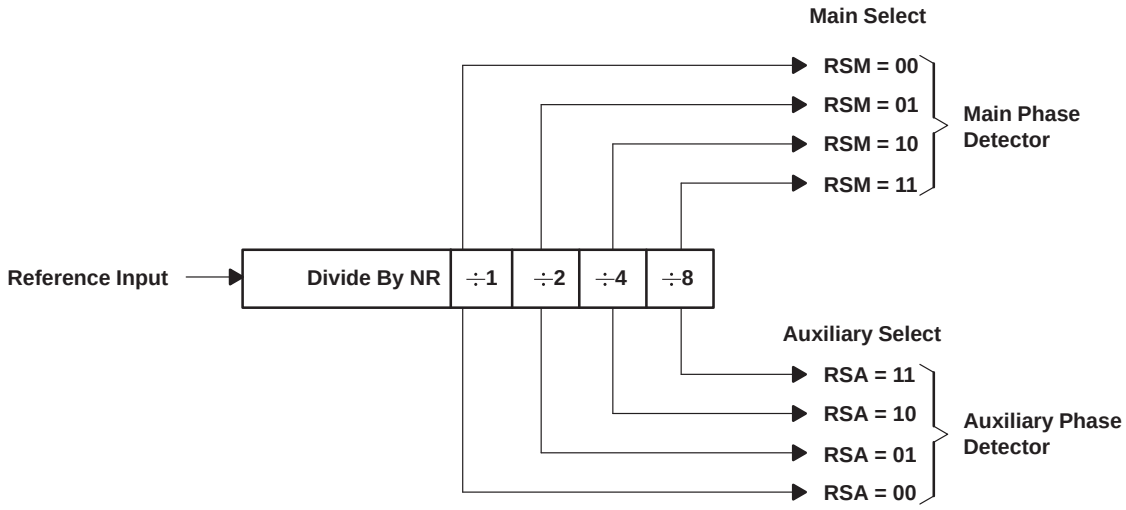


Figure 7. Reference Variable Divider

auxiliary variable divider

The input signal on INA is amplified to logic level by a single-ended input buffer, which has sufficient sensitivity for direct connection to a typical VCO (200 mVpp at 200 MHz). The input stage is enabled when the serial control bit EA = 1. The auxiliary divider consists of a 13-bit programmable divider with a 8/9 dual-modulus prescaler. The 13-bit field divider is composed of two separate counters: a 3-bit NA2 counter and a 10-bit NA1 counter. The total divider ratio value can be expressed as: NA = 8 $\times$ (NA1 – NA2) + 9 $\times$ NA2, where 7 $\leq$ NA1 $\leq$ 1023, and 0 $\leq$ NA2 $\leq$ 7. This results in a continuous integral divide range of 56 to 8191. The detail of the 13-bit field of the auxiliary divider is shown in Figure 8.

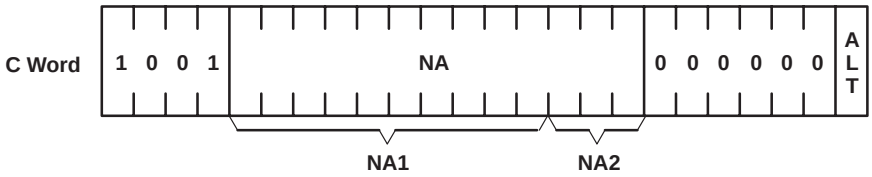


Figure 8. 13-Bit Field Divider

PRINCIPLES OF OPERATION

main variable divider – general

The input signal on RXLO is amplified to a logic level by a differential-input comparator giving a common mode rejection. The input stage is enabled by serial control bit EM = 1. Disabling means that all currents in the comparator are switched off. The main variable divider is programmed using two different schemes: standard and alternate.

The standard programming scheme (ALT=0) is referenced to a main divider section that implements a dual/triple-modulus prescaler [(64/65)/(64/65/72)] design. The dual/triple modulus prescaler is actually synthesized using a 32/33 dual-modulus prescaler with conversions that occur within the TRF3040 and are transparent to the user.

Depending on the value of the prescaler select PR, the bit capacity for NM1, NM2, and NM3 is defined, as listed in Table 6 (see also Figure 4).

Table 6. Main Variable Divider Bit Capacity

	BIT CAPACITY		
PR	NM1	NM2	NM3
00	12	8	0
01	12	8	0
10	12	4	4
11	12	4	4

The total N-division ratio, as a function of the 64/65 dual-modulus and the 64/65/72 triple-modulus prescaler can be expressed as:

- N_{total} = 64(NM1 + 2) + 65(NM2), where PR = 0X,
- N_{total} = 64(NM1 + 2) + 65(NM2) + 72(NM3 + 1), where PR = 1X.

For contiguous channels, the values of NM1, NM2, and NM3 are defined:

- For PR = 0X: $61 \leq NMI \leq 4095$ and $0 \leq NM2 \leq 63$, which yields minimum and maximum divide ratios of 4032 and 266303, respectively.
- For PR = 1X: $14 \leq NMI \leq 4095$ and $0 \leq NM2 \leq 15$ and $0 \leq NM3 \leq 15$, which yields minimum and maximum divide ratios of 1096 and 264335, respectively.

The alternate programming scheme (ALT=1) is provided for ease of use. The 32/33 dual modulus prescaler is the reference of the alternate programming scheme. Referring to the A-word of Figure 4 shown previously, the main divider consists of 18-bit NM-field counters. The NM-field counter section is composed of two separate counters: a 5-bit A-counter and a 13-bit B-counter, as shown in Figure 9. The prescaler divides by 33 until the A-counter reaches terminal count and then divides by 32 until the B-counter reaches terminal count where upon both counters reset and the cycle repeats.

The total NM division is defined as:

$NM_{Total} = 32(B - A) + 33(A)$, where $0 \leq A \leq 31$ and $31 \leq B \leq 8191$.

This results in a continuous integral divide range of 992 to 262143. If B < 31, the synthesizer no longer provides contiguous channels. It is important to note that the value assigned to A is never greater than the value assigned to B.

PRINCIPLES OF OPERATION

main variable divider – general (continued)

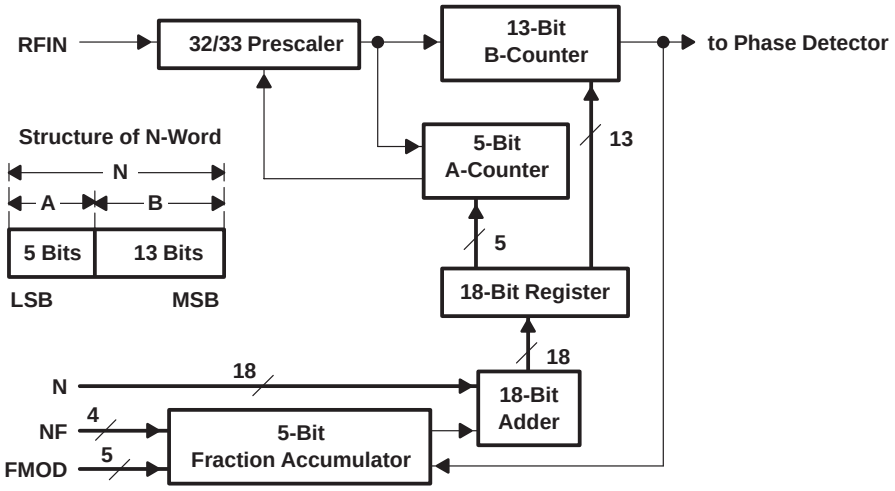


Figure 9. Main Divider Organization

main variable divider – synchronization

The A-word is loaded into working registers only when a main divider synchronization signal is active in order to avoid phase jumps when reprogramming the main divider. The synchronization signal is generated by the main divider and is active when the main divider reaches its terminal count; also at this time, a main divider output pulse is sent to the main phase detector. The new A-word is correctly loaded provided that the STROBE signal is at an active high.

main variable divider – fractional accumulator

The TRF3040 main synthesizer loop can operate as a traditional integer-N feedback phase-locked loop or as a fractional-N feedback phase-locked loop. The integer-N feedback loop divides the VCO frequency by integer values of N that result in phase detector reference comparisons at the desired channel spacing. A fractional-N feedback loop divides the VCO frequency by an integer term plus a fractional term that results in phase detector reference comparisons at integer multiples of the desired system channel spacing.

Integer-N division: VCO frequency $\div$ N = Phase detector reference frequency
= channel spacing

Fractional-N division: VCO frequency $\div$ (N + NF/FMOD) = Phase detector reference frequency
= FMOD $\times$ channel spacing

where $0 \le NF < FMOD$ and $1 \le FMOD \le 16$.

Because the programmable main counter and prescaler can not divide by a fraction of an integer, fractional-N division is accomplished by averaging main divider cycles of division by N and N+1. A fractional accumulator that is programmed with values of NF and FMOD is responsible for causing the main counter and prescaler sections to divide by N or N+1.

The fractional accumulator operates modulo-FMOD and is incremented by NF at the completion of each main divider cycle. When the fractional accumulator overflows, division by N+1 occurs. Otherwise, the main counters and prescaler divide by N; division by N+1 is transparent to the user. Table 7 shows the contents of the fractional accumulator and the resulting N or N+1 division for two fractional division ratios.

PRINCIPLES OF OPERATION

Table 7. Fractional Accumulator Operation

NF = 3, FMOD = 8	
ACCUMULATOR NUMERATOR	STATE
3	÷ N
6	÷ N
1	÷ N + 1, overflow
4	÷ N
7	÷ N
2	÷ N + 1, overflow
5	÷ N
0	÷ N + 1, overflow

NF = 6, FMOD = 8	
ACCUMULATOR NUMERATOR	STATE
6	÷ N
4	÷ N + 1, overflow
2	÷ N + 1, overflow
0	÷ N + 1, overflow
6	÷ N
4	÷ N + 1, overflow
2	÷ N + 1, overflow
0	÷ N + 1, overflow

For example, suppose that the main synthesizer input frequency is 1958.97 MHz, the main phase detector reference frequency is 240 kHz, and a channel spacing of 30 kHz is realized. The value of FMOD = 8 would be selected because 240 kHz/30 kHz = 8. Dividing the main synthesizer input frequency by the reference frequency results in 1958.97 ÷ 0.24 = 8162.375 = 8162 + 3/8. As a result, the fractional accumulator overflow cycle of this particular frequency is described with NF=3 and FMOD=8 (see Table 7). Figure 10 illustrates the division by N and N+1 for this 3/8 fractional channel example.

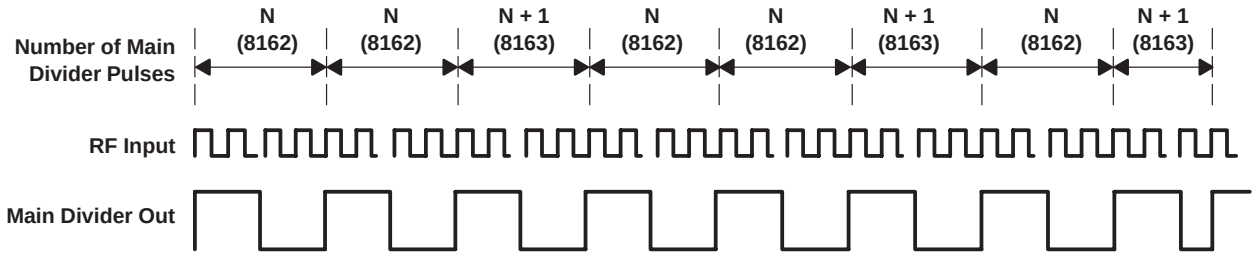


Figure 10. 3/8 Fractional Channel Main Divider Operation

The mean division over the complete fractional accumulator cycle as shown in Figure 9 is:

$$N_{MEAN} = \frac{8162 + 8162 + 8163 + 8162 + 8162 + 8163 + 8162 + 8163}{8} = 8162.375$$

$$= 8162 + 3/8.$$

Therefore, fractional channels are available every 30 kHz or 240 kHz $\frac{1}{FMOD} = \frac{240\ kHz}{8}$.

main divider – integer channels

In the case where NF = 0, only division by N occurs and the fractional accumulator essentially is steady state with a numerator of 0 and never increments or overflows. A channel that requires NF = 0 is a pure integer channel because the fractional term of $\frac{NF}{FMOD}$ is zero.

PRINCIPLES OF OPERATION

main divider – fractional-N sidebands and compensation

Programming a fractional-N channel means the main divider and prescaler divide by N or N + 1 as dictated by the operation of the fractional accumulator. Because the main divider operation is integer in nature and the desired VCO frequency is not, the output of the main phase detector is modulated with a resultant fractional-N phase ripple that, if left uncompensated, produces sideband energy. This phase ripple is proportional and synchronized to the contents of the fractional accumulator that is used to control fractional-N sideband compensation. Only channels that require a nonzero value of NF have the fractional-N sideband energy. The fractional-N sidebands appear at offset frequencies from the VCO fundamental tone, which are multiples of NF/FMOD. Figure 11 shows the fractional-N phase detector ripple for a 3/8 fractional channel.

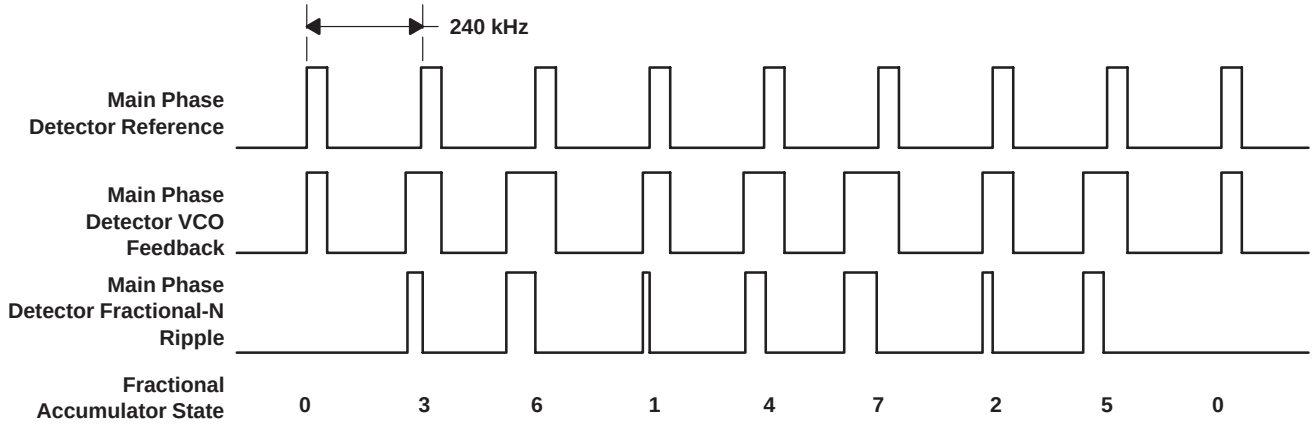


Figure 11. Fractional-N Phase Detector Ripple for 3/8 Fractional Channel

The TRF3040 has internal circuitry that provides a means to compensate for the phase detector fractional-N phase ripple thereby significantly reducing the magnitude of the fractional-N sidebands. Because the current waveform output of the main phase-locked loop (PLL) proportional charge pumps is modulated with the phase detector fractional-N phase ripple, a fractional-N compensation charge pump output is summed with the main PLL proportional charge pump.

Figure 12 shows the fractional-N ripple magnitude on the main PHP charge pump output. The magnitude is essentially constant and the pulse width is modulated with the contents of the fractional accumulator. The area under the Main PHP charge pump curve represents the amount of charge delivered to the system loop filter network. In order to minimize fractional-N sidebands in the VCO spectrum, the compensation current waveform is generated to have *equal* and *opposite* sign magnitude *areas* as the main PHP charge pump.

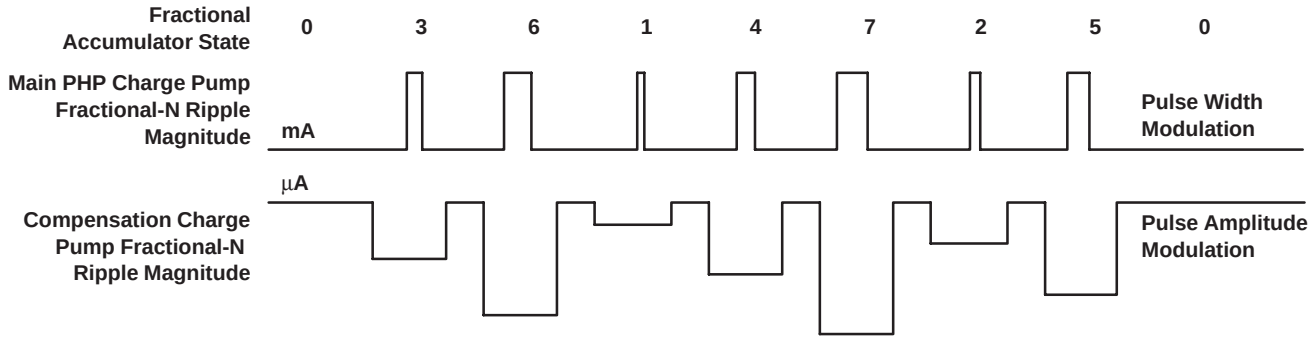


Figure 12. Main PHP and Compensation Charge Pump Fractional-N Waveforms for 3/8 Fractional Channel

PRINCIPLES OF OPERATION

main divider – fractional-N sidebands and compensation (continued)

The compensation waveform is pulse-amplitude modulated with the contents of the fractional accumulator. The main PHP pulse magnitude is much larger than the compensation pulse magnitude, but the compensation pulse has a much longer duration than that of the main PHP pulse. The compensation pulse is optimally centered about the main PHP charge pump pulse in order to avoid additional sideband energy due to phase-offset between the main and compensation pulses.

The following step illustrates a method for determining correct values for RN, RF, and CN for minimal fractional-N sidebands based on VCO frequency and reference frequency.

Assumptions:

The main VCO is locked on channel.
The 1970 ± 15-MHz main VCO operation, 1958.19 – 1983.15 MHz.
19.44-MHz reference frequency
240-kHz phase detector reference frequency
288-μA peak main PHP current

1. Determine the fundamental fractional-N pulse-width portion of the main PHP charge-pump output waveform for the lower, upper, and mean frequencies.

$$\text{Frac}_{\text{PW–LWR}} = \frac{1}{f_{PD}} - \frac{N}{f_{VCO}} = \frac{1}{240\ \text{kHz}} - \frac{8159}{1958.19\ \text{MHz}} = 63.83\ \text{ps},$$

$$\text{Frac}_{\text{PW–UPR}} = \frac{1}{f_{PD}} - \frac{N}{f_{VCO}} = \frac{1}{240\ \text{kHz}} - \frac{8263}{1983.15\ \text{MHz}} = 63.031\ \text{ps},$$

$$\text{Frac}_{\text{PW–MEAN}} = \frac{\text{Frac}_{\text{PW}-\text{LWR}} + \text{Frac}_{\text{PW–UPR}}}{2} = \frac{63.83\ \text{ps} + 63.031\ \text{ps}}{2} = 63.43\ \text{ps}.$$

Therefore, the mean unit pulse-width of the fractional-N portion of the main PHP charge-pump output waveform over the VCO frequencies of interest is 63.43 *ps*. This fundamental pulse width is modulated by the contents of the fractional accumulator. For the 3/8 fractional-N channel example, the pulse width varies as shown in Table 8.

Table 8 also shows the area of the fractional-N portion of the main PHP charge-pump waveform.

Table 8. Main PHP Fractional-N Pulse Widths and Areas for 3/8 Channel

NF = 3, FMOD = 8		
ACCUMULATOR STATE	**MAIN PHP FRACTIONAL PULSE WIDTH (E–12 SECONDS)**	**MAIN PHP FRACTIONAL AREA (E–12 SECOND X AMPS)**
3	3 × *PW–Mean* = 190.29	190.29 ps × 288 μA = 0.54804
6	6 × *PW–Mean* = 380.58	380.58 ps × 288 μA = 0.109607
1	1 × *PW–Mean* = 63.43	63.43 ps × 288 μA = 0.018268
4	4 × *PW–Mean* = 253.72	253.72 ps × 288 μA = 0.073071
7	7 × *PW–Mean* = 444.01	444.01 ps × 288 μA = 0.127875
2	2 × *PW–Mean* = 126.86	126.86 ps × 288 μA = 0.036536
5	5 × *PW–Mean* = 317.15	317.15 ps × 288 μA = 0.091339
0	0 × *PW–Mean* = 0	0 ps × 288 μA = 0

PRINCIPLES OF OPERATION

main divider – fractional-N sidebands and compensation (continued)

1. Determine the pulse width of the compensation charge-pump output waveform.

$$Comp_{PW} = \frac{1}{f_{Ref}} = \frac{1}{19.44\ MHz} = 51.440\ ns$$

2. Determine the fundamental compensation charge pump current magnitude using the fundamental main PHP fractional area.

$$Comp_{Mag} = \frac{Frac_{Area}}{Comp_{PW}} = \frac{0.018268\ psA}{51.440\ ns} = 0.3551\ \mu A$$

Table 9 shows the magnitude of the compensation pulse as a function of the fractional accumulator.

Table 9. Compensation Pulse Magnitudes for 3/8 Channel

NF = 3, FMOD = 8	
Accumulator Numerator	**Compensation Pulse Magnitude (μA)**
3	3 × 0.3551 = 1.0653
6	6 × 0.3551 = 2.136
1	1 × 0.3551 = 0.3551
4	4 × 0.3551 = 1.4204
7	7 × 0.3551 = 2.4857
2	2 × 0.3551 = 0.7102
5	5 × 0.3551 = 2.4857
0	0 × 0.3551 = 0

3. Using the result of Step 2, determine the value of RF to give the fundamental compensation pulse magnitude.

$$RF\ (k\Omega) = \frac{VBG}{40\ x\ Comp_{Mag}(\mu A)} = \frac{1.25}{40\ x\ 0.3551} = 88\ k\Omega.$$

4. Determine values of CN and RN to give a main PHP charge-pump peak current of 500 μA. Assume a mid-range value of CN equal 128.

$$RN(k\Omega) = \left(18.75 \times \frac{CN}{256} \times \frac{1}{I(mA)}\right) - 0.75 = \left(18.75 \times \frac{128}{256} \times \frac{1}{0.288\ mA}\right) - 0.75 = 32.55\ k\Omega.$$

5. The value of the fundamental compensation pulse magnitude calculated in step 3 is fixed, and the compensation pulse width calculated in step 2 is also fixed. However, because the VCO can tune over a significant range of frequencies, the pulse width of the fractional-N portion of the main PHP charge-pump waveform varies, thus the area of the same waveform varies. In order to maintain equal areas under the fractional-N portion of the main PHP charge-pump and compensation waveforms, CN is varied with the VCO frequency. As the VCO frequency increases, the fractional-N portion of the main PHP charge-pump waveform pulse width decreases proportionally, thereby decreasing the area under the same waveform. Therefore, CN must be adjusted to equalize the main PHP and compensation waveform areas. The lower and upper fractional–N pulse widths are calculated using the equations in step 1, as follows:

$Frac_{PW\text{-}LWR}$ = 64.168 ps for f_{VCO} = 1958.19 MHz
$Frac_{PW\text{-}UPR}$ = 63.064 ps for f_{VCO} = 1983.15 MHz

PRINCIPLES OF OPERATION

main divider – fractional-N sidebands and compensation (continued)

The fundamental area mean value of the fractional-N portion of the main PHP charge-pump waveform was calculated to be 0.018268 pSA. If the fundamental area of the fractional-N portion of the main PHP charge-pump waveform uses the actual pulse widths calculated in step 1 in place of the average pulse width, the fractional-N main PHP areas are as follows:

$Frac_{Area\text{-}LWR}$ = 63.83 ps x 0.288 mA = 0.018383 (E-12 second $\times$ Amps),
$Frac_{Area\text{-}UPR}$ = 63.031 ps x 0.288 mA = 0.018383 (E-12 second $\times$ Amps).

The actual areas under the fractional-N portion of the main PHP waveform require slight modification in the charge-pump current. The variation of CN required for area equalization can be determined using a simple ratio form:

$$CN_{LWR} = \frac{Frac_{Area–AVG}}{Frac_{Area–LWR}} \times CN_{AVG} = \frac{0.018268}{0.018383} \times 128 = 127,$$

$$CN_{UPR} = \frac{Frac_{Area–AVG}}{Frac_{Area–UPR}} \times CN_{AVG} = \frac{0.018268}{0.018153} \times 128 = 129.$$

Therefore, *CN* values would vary from 127–129 over the VCO frequency range of 1958.19–1983.15 MHz for optimum fractional-N sideband suppression. Due to component and circuit tolerances, additional deviations in *CN* may be appropriate.

phase detectors

The main and auxiliary synthesizer sections (see Figure 13) incorporate dual D-type flip-flop phase-frequency detectors (PFD). The PFD has gain with phase error over a range of +/–2π and exhibits infinite pull-in range. Dead-band compensation about zero phase error is provided by forcing the sourcing and sinking charge pumps to have a minimum on-time rate of $1/f_{Ref}$ when the loop is operating in a locked condition.

The phase detectors can be programmed for polarity sense. Normally, external system VCOs have a positive slope control voltage-frequency characteristic. Some VCOs have a negative slope characteristic. The TRF3040 main and auxiliary phase detectors can be programmed for use with positive or negative slope VCOs using the *MCP* and *ACP* fields, respectively, in the B word (EPM mode).

For positive slope VCOs: MCP = ACP = 0; for negative slope VCOs: MCP = ACP = 1.

PRINCIPLES OF OPERATION

phase detectors (continued)

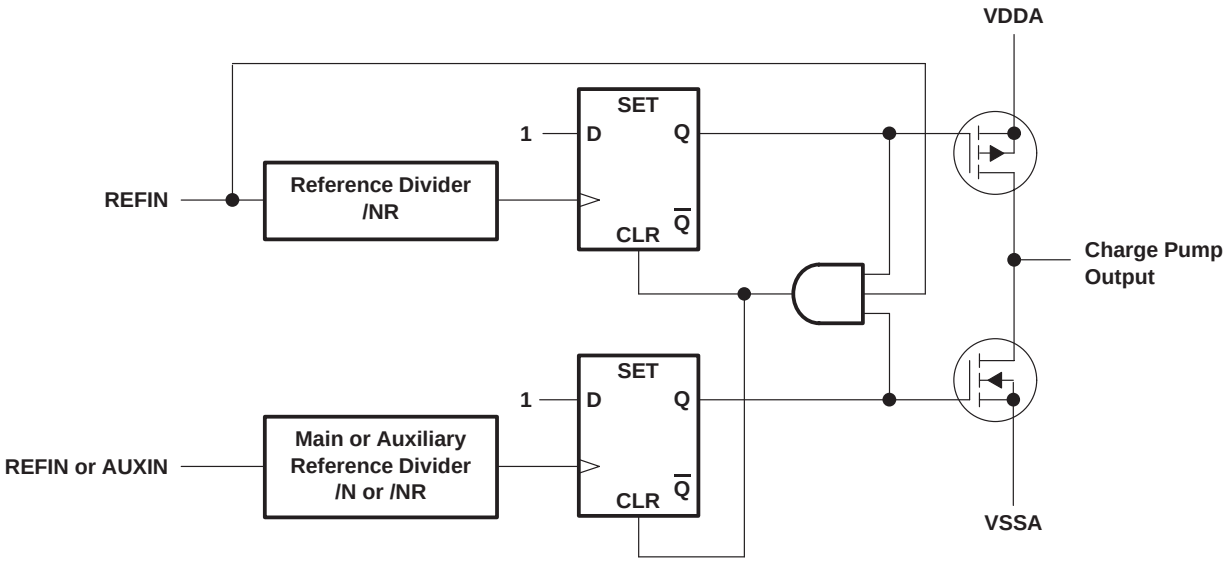


Figure 13. Main and Auxiliary Phase Detector Circuit

charge-pump current plans

The TRF3040 uses internal band-gap references and external resistors to develop biasing reference currents for the various charge pump sections. Three terminals are designated for the external resistors: RN, RF, and RA. Internal, programmable coefficients CN, CL, and CK are also used. Table 10 shows how the external resistors are used to achieve desired charge-pump peak currents.

Table 10. Charge Pump Current Plans

PARAMETER	MODE	CONDITION	UNIT
Main $PHP_{NORMAL} = \frac{V_{BG} \times CN}{17(RN + 300)}$	Normal	RN in kΩ	mA
Main $PHP_{SPEED\ UP} = \frac{2^{CL+1} \times CN \times V_{BG}}{17(RN + 300)}$	Speed-up	RN in kΩ	mA
Main $PHI_{PSPEED\ UP} = \frac{2^{CL+1} \times V_{BG} \times CN \times CK}{17\ (RN + 300)}$	Speed-up	RN in kΩ	mA
†Fractional $PHP_{NORMAL} = \frac{V_{BG}}{40 \times RF}$	Normal	RF in kΩ	μA
Fractional $PHP_{SPEED\ UP}$ = TBD	Speed-up		
Fractional $PHI_{SPEED\ UP}$ = TBD	Speed-up		
Peak auxiliary current $PHA_{PK} = \left(\frac{1.25}{RA} \times 20\right)$	Normal	RA in kΩ	mA

† The compensation charge-pump current is a pulse-amplitude modulated with the contents of the fractional accumulator. See the section on Main Divider – Fractional-N Sidebands and Compensation.

PRINCIPLES OF OPERATION

charge-pump current plans (continued)

The average charge-pump current for the PHP, PHI, and PHA terminals is defined by:

$$I_{AVG} = \frac{\theta_{error}}{2\pi} \times I_{PK}.$$

loop enable/disable

The main and auxiliary loops can be enabled and disabled by the contents of enable bits EM and EA, respectively, as described in Table 11. When disabled, all currents in the RF input stages are switched off; the bias currents for the respective charge-pump circuits are switched off as well. When both loops are disabled (EM = EA = 0), the reference input stage currents are switched off. The reference chain can be turned off because the serial interface operates independent of the reference input for the loading of serial words.

Table 11. Loop Enable/Disable

EM	EA	ENABLED	DISABLED
0	0		Main, auxiliary, reference
0	1	Auxiliary, reference	Main
1	0	Main, reference	Auxiliary
1	1	Main, auxiliary, reference	

speed-up mode

When the main synthesizer frequency is changed, it may be desirable to increase the loop bandwidth for a short time in order to achieve a faster lock time. The proportional charge-pump current is increased and the integral charge-pump current is switched on for the duration of speed-up mode. The *charge-pump current plans* section, illustrates how the charge-pump currents are a function of the external resistor RN and the programmable coefficients CN, CL, and CK.

The duration of speed-up mode is controlled by two different means that are dependent on the operational programming scheme of the TRF3040 device: either the alternate (ALT) or standard (STD) programming scheme. In the alternate programming scheme, the speed-up mode duration is controlled as a function of the G-field in the B-word and the reference frequency divider period.

$$\text{Duration}_{ALT} = G \times \frac{NR}{f_{REFIN}}, \text{ ALT speed-up mode duration}$$

The content of the G-field is the value of the most significant 4 bits of a total 8-bit programming operation. The least significant 4 bits are static 1 bits. Therefore the minimum of Duration_{ALT} is:

$$\text{Duration}_{ALTmin} = 15 \times \frac{NR}{f_{REFIN}},$$

and the maximum of Duration_{ALT} is:

$$\text{Duration}_{ALTmax} = 255 \times \frac{NR}{f_{REFIN}},$$

When the TRF3040 is operated in standard programming scheme, the speed-up mode duration is a function of the STROBE signal associated with the A-word. When the STROBE signal following an A-word write operation goes active, speed-up mode currents begin and persist until the STROBE signal is returned to an inactive state.

PRINCIPLES OF OPERATION

lock detect

The LOCK terminal can be polled to determine the synthesizer lock condition of either or all three loops. The lock detect function is described by the Boolean expression:

$$\text{LOCK} = \left(\text{LD}_{\text{Main}} + \overline{\text{EM}}\right) \times \left(\text{LD}_{\text{Aux}} + \overline{\text{EA}}\right) \times \left(\text{TXIF\_LD} + \overline{\text{SE}}\right)$$

test modes

The LOCK terminal may be used for test operation. When test modes are enabled, the LOCK terminal is connected to internal nodes of the TRF3040. Test modes are enabled by writing to the E-word. Test modes are disabled by writing zeros to the E-word. These bits are also reset to zero when the D-word is written. Table 12 lists all available test modes and associated programming bits.

Table 12. Test Modes

TEST MODE	T19 – T16	T15 – T12	T11 – T8	T7 – T4	T3 – T0
Lock detect	0000	0000	0000	0000	0000
Fractional overflow	0000	0000	0000	0000	0100
Auxiliary_VCO divider	0000	0000	0000	0000	0101
Main_VCO divider	0000	0000	0000	0000	0110
Main reference divider	0000	0000	0000	0000	0111
Force lock pin HIGH	1100	0000	0000	0000	0000
Force lock pin LOW	0100	0000	0000	0000	0000
Auxiliary and main pumps UP	0000	0000	0000	1010	1000
Auxiliary and main pumps DOWN	0000	0000	0000	0101	1000
Fractional pump test	0000	0000	0010	0000	0000
Main prescaler bypass	0000	0000	0001	0000	0110
Auxiliary prescaler bypass	0000	1000	0000	0000	0101
Enable reference chain test	0001	0000	0000	0000	0111

transmit modulator

The transmit modulator section of the TRF3040 is composed of a transmit intermediate frequency synthesizer reset circuit that controls the operation of the transmit modulator, a transmit intermediate frequency phase-locked loop that generates the intermediate transmit frequency (TXIF), a single-sideband suppressed carrier (SSBSC) converter, an I/Q modulator, and an output VGA.

transmit intermediate frequency synthesizer reset circuit

Figure 14 and Figure 15 reveal that the falling edge of the STROBE toggles the Q output of flip flop (1) to a 1 state, which enables the TXIF phase detector, the TXIF_VCO, the divide-by-N, the TXIF buffer, and the SSB converter. Once the synthesizer is locked, the TXEN signal (enable = 1) turns on the modulator and the VGA. The rising edge of TXEN has no affect on $\text{SYN}_{\overline{\text{EN}}}$ as shown in Figure 15. However, the falling edge of TXEN toggles the $\overline{\text{Q}}$ output of flip flop (2) to a 0 state which resets flip flop (1) and causes $\text{SYN}_{\overline{\text{EN}}}$ to go to a 0 state, thus disabling the transmit intermediate synthesizer, the I/Q modulator, and the VGA.

PRINCIPLES OF OPERATION

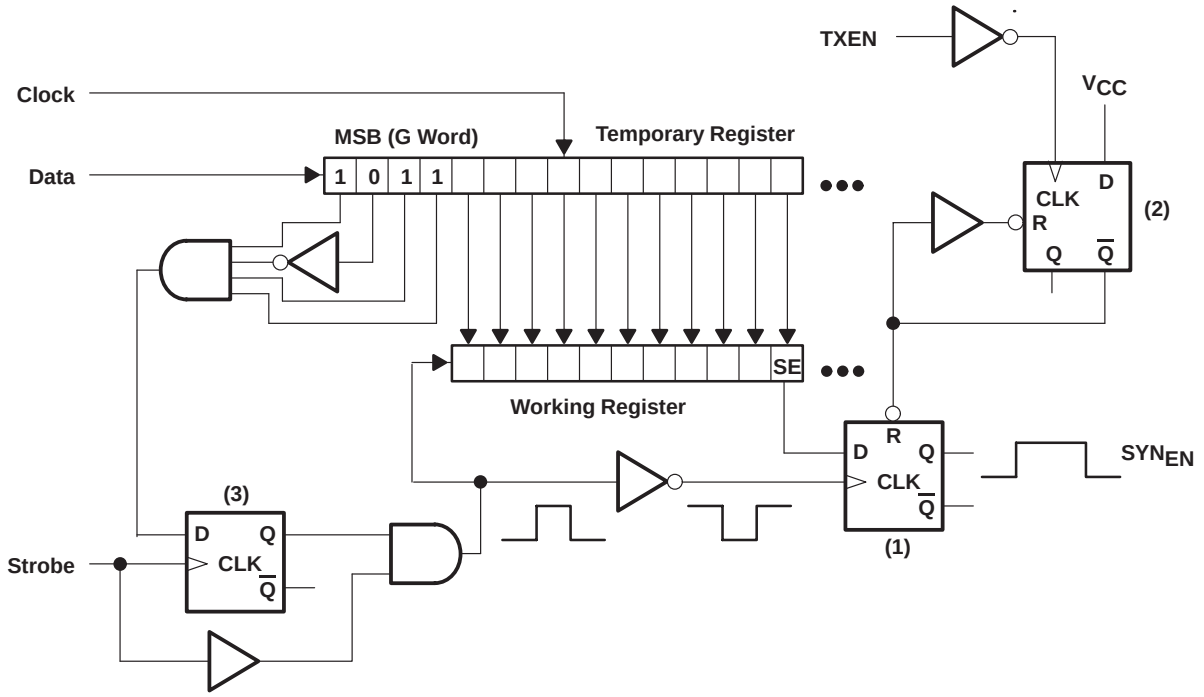


Figure 14. Transmit Intermediate Frequency Synthesizer Reset Circuit

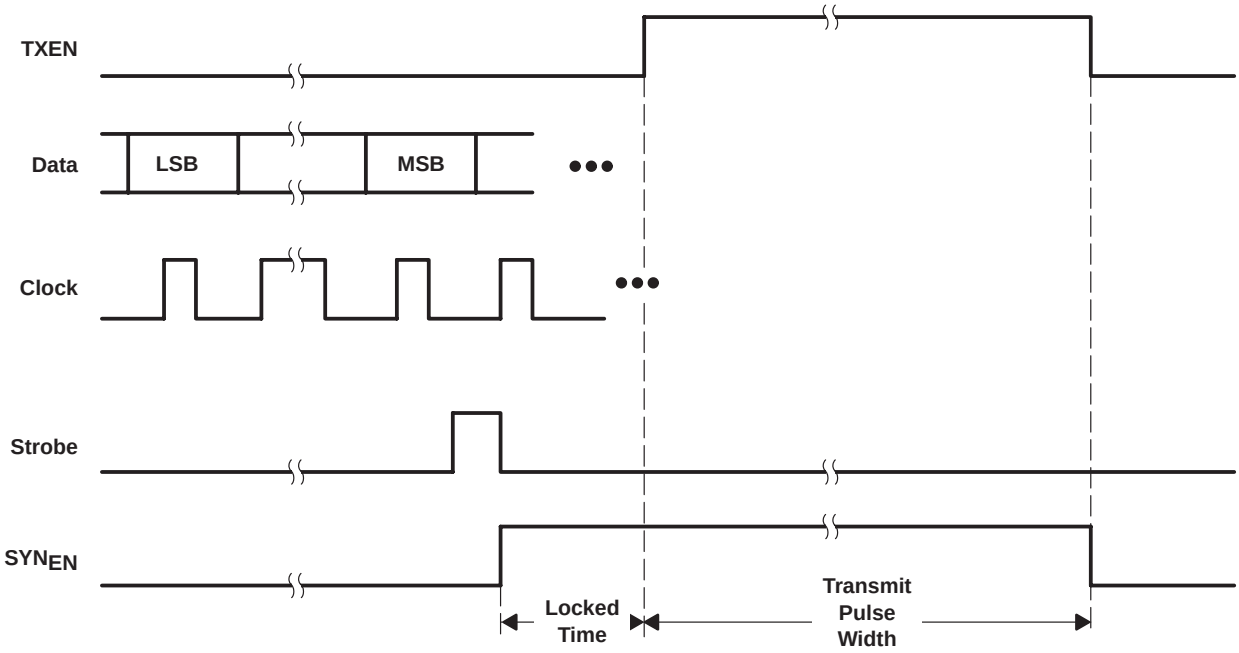


Figure 15. Transmit Intermediate Frequency Synthesizer Reset Circuit Timing Diagram

PRINCIPLES OF OPERATION

transmit intermediate frequency (TXIF) synthesizer

The transmit intermediate frequency (TXIF) PLL portion of the TRF3040 design consists of the following functional blocks: a reference oscillator, a TXIF phase detector, a divide-by-N (÷N), a TXIF_VCO, and an external passive loop filter.

reference oscillator

The reference crystal oscillator (XTAL OSC) generates the internal reference signal INR. This signal is directly fed to the phase detector of the PLL in the transmit modulator section and to three other different buffers. The first buffer feeds the reference divider of the main phase detector and the auxiliary phase detector. The second buffer, MCLK, is used to provide a clock for external digital circuitry, which is always on. The third buffer, RCLK, is used as a clock for the external circuitry that is used in standby and transmit modes.

TXIF phase detector and charge pump

The phase comparator compares the output of the divider with the reference oscillator. It provides an output proportional to the phase difference between the divided down TXIF_VCO and the reference. This output is then filtered and used as the control voltage input to the TXIF_VCO. The phase detector is a Gilbert multiplier cell type, with a linear output from 0 to π ($\pi/2 \pm \pi/2$), followed by a charge pump. The charge-pump peak output current could be programmable to 6.4 mA using an external resistor.

TXIF lock detect

A lock detect signal is provided and ANDed together with lock detect signals from both the main channel synthesizer and auxiliary synthesizer. While in standby mode, the lock detect signal is forced to a valid lock state so that the lock detect signal will indicate when the main and auxiliary phase detectors achieve phase lock.

divide-by-N

The ÷N is a 2-bit programmable divider that can be configured for any integer division from 6 to 9. The field bits setting for this ÷N is described in Note 6. The divider converts the VCO output down to the reference frequency before feeding it into the phase comparator.

TXIF_VCO

The voltage controlled oscillator, TXIF_VCO, generates the transmit IF frequency, TXIF, between 90 MHz and 200 MHz. This TXIF_VCO is configured using an external parallel inductor and a dual common-cathode tuning-varactor diode. DC blocking capacitors are used to isolate the varactor control voltage from the VCO tank dc bias voltages.

SSBSC converter and TXIF buffer

The TXIF buffer provides isolation between the SSBSC converter and the TXIF_VCO output. The converter is an active Gilbert cell multiplier (matched pair) combined with two quadrature phase shift networks and a band-pass filter. The SSBSC converter rejects the unwanted upper sideband that would normally occur during the conversion process.

PRINCIPLES OF OPERATION

I/Q modulator

The quadrature modulator is an active Gilbert cell multiplier (matched pair) with cross-coupled outputs. These outputs are provided to the variable gain amplifier, DUALTX VGA.

variable gain amplifier (VGA) and power amplifier (PA) driver

The DUALTX VGA power control circuit has a control range of 50 dB (–41 dBm to 9 dBm) with a monotonically decreasing slope, 0.5 dB per step (typical), as shown in Figure 16. A 4:1 balun is used on the applications circuit to transform the 200-Ω differential output impedance of the PA driver to a 50-Ω single-ended impedance for testing purposes.

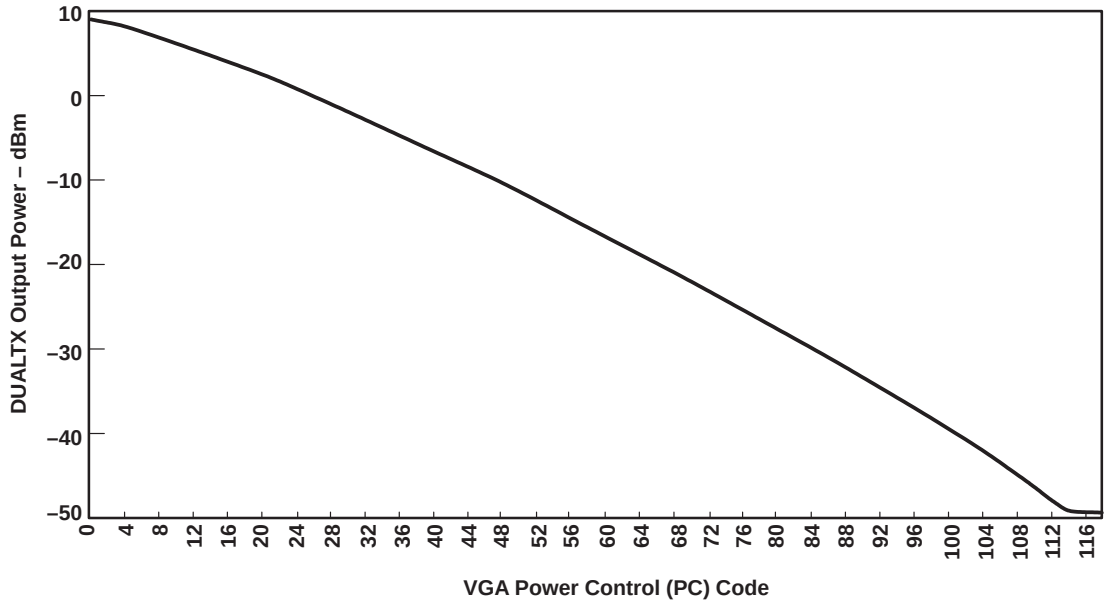
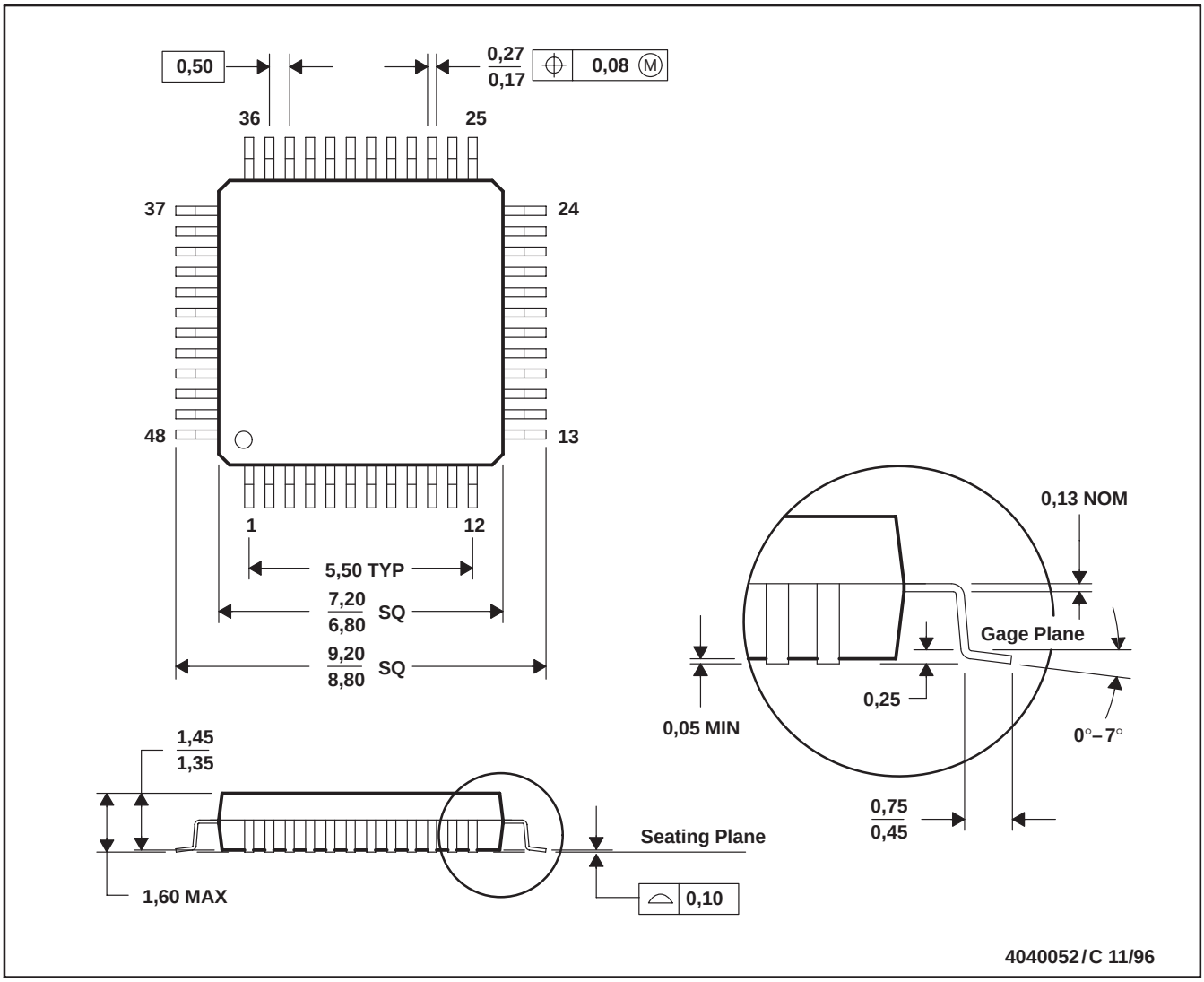


Figure 16. Power Control

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads connected to the die pads.

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