

Features

- Fast 8192 x 8 bit static CMOS RAM
- 35 ns Access Time
- Bidirectional data inputs and data outputs
- Three-state outputs
- Data retention mode at $V_{CC} > 2V$
- Data retention current at 2 V:
 - < 3 μA (K-Type)
 - < 50 μA (A-Type)
- Standby current
 - < 5 μA (K-Type)
 - < 100 μA (A-Type)
- TTL/CMOS-compatible
- Automatic reduction of power dissipation in long Read or Write cycles
- Power supply voltage 5 V
- Operating temperature ranges
 - 40 to 85 °C
 - 40 to 125 °C
- QS 9000 Quality Standard
- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity > 200 mA
- Package: SOP28 (300 mil)

Description

The U62H64 is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read
- Standby
- Write
- Data Retention

The memory array is based on a 6-transistor cell.

The circuit is activated by the rising edge of $\overline{E2}$ (at $\overline{E1} = L$), or the falling edge of $\overline{E1}$ (at $\overline{E2} = H$). The address and control inputs open simultaneously.

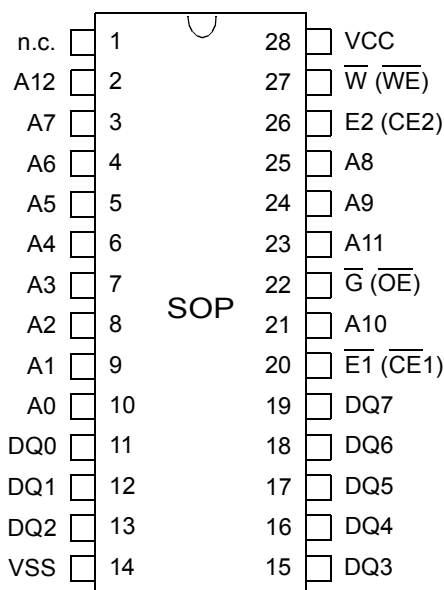
According to the information of \overline{W} and \overline{G} , the data inputs, or outputs, are active. In a Read cycle, the data outputs are activated by the falling edge of \overline{G} , afterwards the data word read will be available at the outputs DQ0 - DQ7. After the address change, the data outputs go High-Z until the new read information is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no

change of the address, data input and control signals \overline{W} or \overline{G} , the operating current (at $I_O = 0$ mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of $\overline{E2}$ or \overline{W} , or by the rising edge of $\overline{E1}$, respectively.

Data retention is guaranteed down to 2 V.

With the exception of $\overline{E1}$ and $\overline{E2}$, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required. This gate circuit allows to achieve low power standby requirements by activation with TTL-levels too.

Pin Configuration



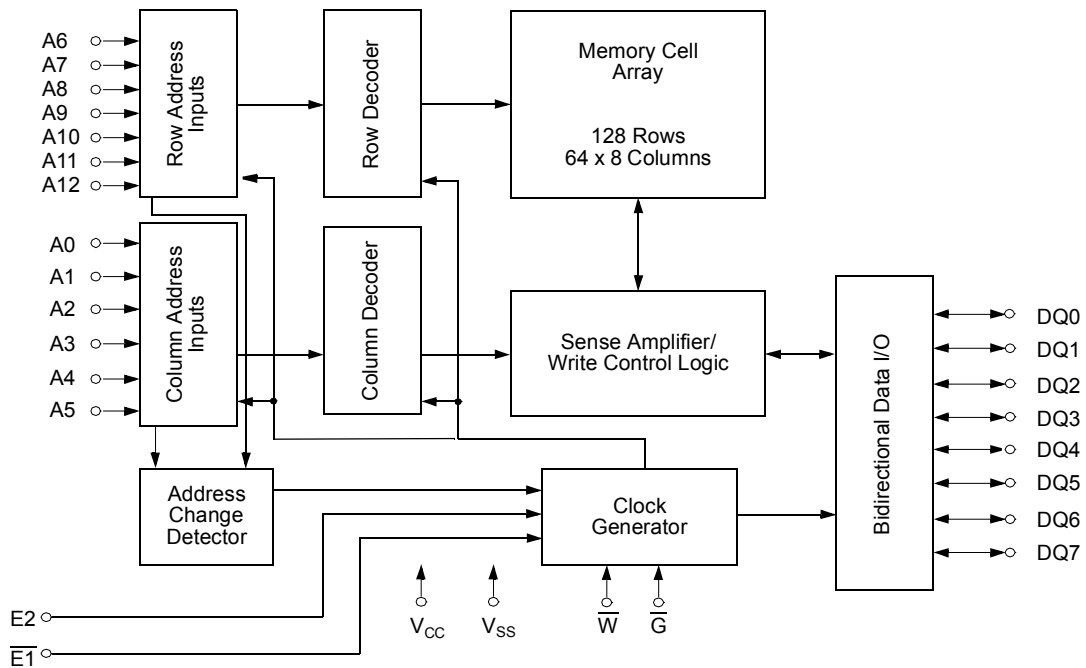
Top View

Pin Description

| Signal Name | Signal Description |
|-----------------|----------------------|
| A0 - A12 | Address Inputs |
| DQ0 - DQ7 | Data In/Out |
| $\overline{E1}$ | Chip Enable 1 |
| E2 | Chip Enable 2 |
| \overline{G} | Output Enable |
| \overline{W} | Write Enable |
| VCC | Power Supply Voltage |
| VSS | Ground |
| n.c. | not connected |

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Block Diagram



Truth Table

| Operating Mode | $\overline{E1}$ | E2 | \overline{W} | \overline{G} | DQ0 - DQ7 |
|----------------------|-----------------|----|----------------|----------------|--------------------|
| Standby/not selected | * | L | * | * | High-Z |
| | H | * | * | * | High-Z |
| Internal Read | L | H | H | H | High-Z |
| Read | L | H | H | L | Data Outputs Low-Z |
| Write | L | H | L | * | Data Inputs High-Z |

* H or L

Characteristics

All voltages are referenced to $V_{SS} = 0$ V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I , as well as input levels of $V_{IL} = 0$ V and $V_{IH} = 3$ V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis} -times and t_{en} -times, in which cases transition is measured ± 200 mV from steady-state voltage.

| Absolute Maximum Ratings ^a | Symbol | Min. | Max. | Unit | |
|---|------------|--------|-----------------------------|------|----|
| Power Supply Voltage | V_{CC} | -0.3 | 7 | V | |
| Input Voltage | V_I | -0.3 | $V_{CC} + 0.5$ ^b | V | |
| Output Voltage | V_O | -0.3 | $V_{CC} + 0.5$ ^b | V | |
| Operating Temperature | T_a | K-Type | -40 | 85 | °C |
| | | A-Type | -40 | 125 | °C |
| Storage Temperature | T_{stg} | -65 | 150 | °C | |
| Output Short-Circuit Current at $V_{CC} = 5$ V and $V_O = 0$ V ^c | $ I_{OS} $ | | 200 | mA | |

^a Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

^b Maximum voltage is 7 V

^c Not more than 1 output should be shorted at the same time. Duration of the short circuit should not exceed 30 s.

| Recommended Operating Conditions | Symbol | Conditions | Min. | Max. | Unit |
|----------------------------------|--------------|------------|------|----------------|------|
| Power Supply Voltage | V_{CC} | | 4.5 | 5.5 | V |
| Data Retention Voltage | $V_{CC(DR)}$ | | 2.0 | - | V |
| Input Low Voltage ^d | V_{IL} | | -0.3 | 0.8 | V |
| Input High Voltage | V_{IH} | | 2.2 | $V_{CC} + 0.3$ | V |

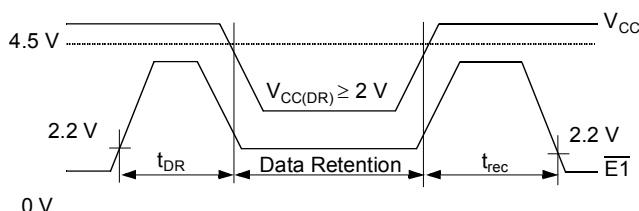
^d -2 V at Pulse Width 10 ns or -1 V at Pulse Width 50 ns

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| Electrical Characteristics | Symbol | Conditions | Min. | Max. | Unit |
|--|---------------|--|------|---------------|--------------------------------|
| Supply Current - Operating Mode | $I_{CC(OP)}$ | $V_{CC} = 5.5\text{ V}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.2\text{ V}$ $t_{cW} = 35\text{ ns}$ | | 50 | mA |
| Supply Current - Standby Mode (CMOS level) | $I_{CC(SB)}$ | $V_{CC} = 5.5\text{ V}$ $V_{E1} = V_{E2} = V_{CC} - 0.2\text{ V}$ K-Type A-Type | | 5 100 | μA μA |
| Supply Current - Standby Mode (TTL level) | $I_{CC(SB)1}$ | $V_{CC} = 5.5\text{ V}$ $V_{E1} = V_{E2} = 2.2\text{ V}$ | | 5 (typ. 2) | mA |
| Supply Current - Data Retention Mode | $I_{CC(DR)}$ | $V_{CC(DR)} = 2.0\text{ V}$ $V_{E1} = V_{E2} = V_{CC(DR)} - 0.2\text{ V}$ K-Type A-Type | | 3 50 | μA μA |
| Output High Voltage | V_{OH} | $V_{CC} = 4.5\text{ V}$ $I_{OH} = -4.0\text{ mA}$ | 2.4 | - | V |
| Output Low Voltage | V_{OL} | $V_{CC} = 4.5\text{ V}$ $I_{OL} = 8.0\text{ mA}$ | - | 0.4 | V |
| Output High Current | I_{OH} | $V_{CC} = 4.5\text{ V}$ $V_{OH} = 2.4\text{ V}$ | - | -4.0 | mA |
| Output Low Current | I_{OL} | $V_{CC} = 4.5\text{ V}$ $V_{OL} = 0.4\text{ V}$ | 8.0 | - | mA |
| Input High Leakage Current | I_{IH} | $V_{CC} = 5.5\text{ V}$ $V_{IH} = 5.5\text{ V}$ | - | 2 | μA |
| Input Low Leakage Current | I_{IL} | $V_{CC} = 5.5\text{ V}$ $V_{IL} = 0\text{ V}$ | -2 | - | μA |
| Output Leakage Current High at Three-State Outputs | I_{OHZ} | $V_{CC} = 5.5\text{ V}$ $V_{OH} = 5.5\text{ V}$ | - | 2 | μA |
| Low at Three-State Outputs | I_{OLZ} | $V_{CC} = 5.5\text{ V}$ $V_{OL} = 0\text{ V}$ | -2 | - | μA |

| Switching Characteristics | Symbol | | Min. | Max. | Unit |
|---|--|--|---------------------|----------------|----------------------|
| | Alt. | IEC | | | |
| Time to Output in Low-Z from $\overline{E1}$ LOW or E2 HIGH \overline{G} LOW \overline{W} HIGH | t_{LZCE} t_{LZOE} t_{LZWE} | $t_{en(E)}$ $t_{en(G)}$ $t_{en(W)}$ | 5 0 0 | | ns ns ns |
| Cycle Time Write Cycle Time Read Cycle Time | t_{WC} t_{RC} | t_{cW} t_{cR} | 35 35 | | ns ns |
| Access Time $\overline{E1}$ LOW or E2 HIGH to Data Valid \overline{G} LOW to Data Valid Address to Data Valid | t_{ACE} t_{OE} t_{AA} | $t_{a(E)}$ $t_{a(G)}$ $t_{a(A)}$ | | 35 15 35 | ns ns ns |
| Pulse Widths Write Pulse Width Chip Enable to End of Write | t_{WP} t_{CW} | $t_{w(W)}$ $t_{w(E)}$ | 20 25 | | ns ns |
| Setup Times Address Setup Time Chip Enable to End of Write Write Pulse Width Data Setup Time | t_{AS} t_{CW} t_{WP} t_{DS} | $t_{su(A)}$ $t_{su(E)}$ $t_{su(W)}$ $t_{su(D)}$ | 0 25 20 15 | | ns ns ns ns |
| Data Hold Time Address Hold from End of Write | t_{DH} t_{AH} | $t_{h(D)}$ $t_{h(A)}$ | 0 0 | | ns ns |
| Output Hold Time from Address Change | t_{OH} | $t_{v(A)}$ | 5 | | ns |
| $\overline{E1}$ HIGH or E2 LOW to Output in High-Z \overline{W} LOW to Output in High-Z \overline{G} HIGH to Output in High-Z | t_{HZCE} t_{HZWE} t_{HZOE} | $t_{dis(E)}$ $t_{dis(W)}$ $t_{dis(G)}$ | | 15 15 12 | ns ns ns |
| $\overline{E1}$ LOW or E2 HIGH to Power-Up | t_{PU} | | 0 | | ns |
| $\overline{E1}$ HIGH or E2 LOW to Power-Down | t_{PD} | | | 35 | ns |

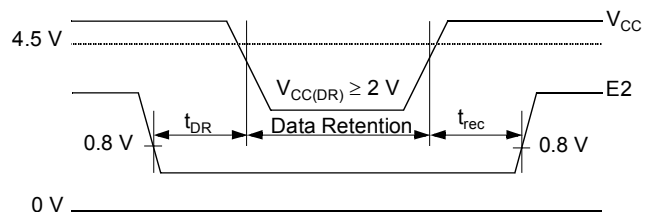
Data Retention Mode $\overline{E1}$ -Controlled



$$V_{E2(DR)} \geq V_{CC(DR)} - 0.2 \text{ V or } V_{E2(DR)} \leq 0.2 \text{ V}$$

$$V_{CC(DR)} - 0.2 \text{ V} \leq V_{E1(DR)} \leq V_{CC(DR)} + 0.3 \text{ V}$$

Data Retention Mode E2-Controlled



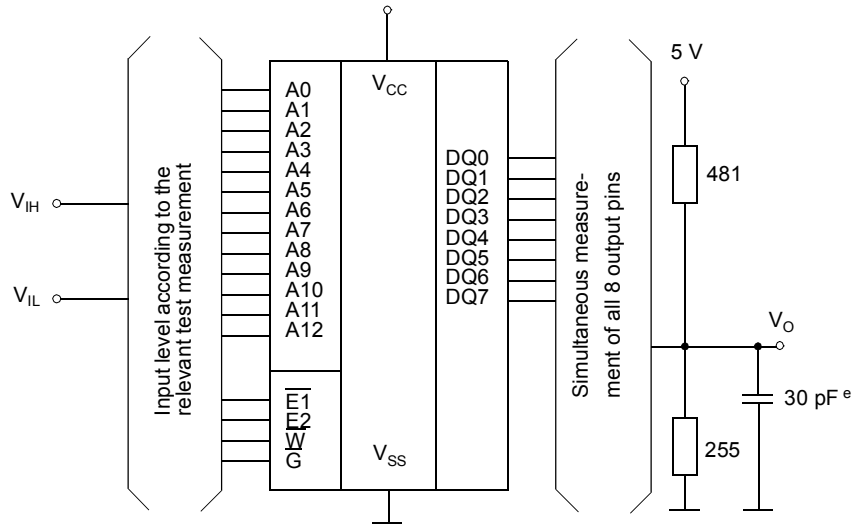
$$V_{E1(DR)} \geq V_{CC(DR)} - 0.2 \text{ V or } V_{E1(DR)} \leq 0.2 \text{ V}$$

$$V_{E2(DR)} \leq 0.2 \text{ V}$$

Chip Deselect to Data Retention Time t_{DR} : min 0 ns
 Operating Recovery Time at $V_{CC(DR)}$ t_{rec} : min t_{cR}

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Test Configuration for Functional Check

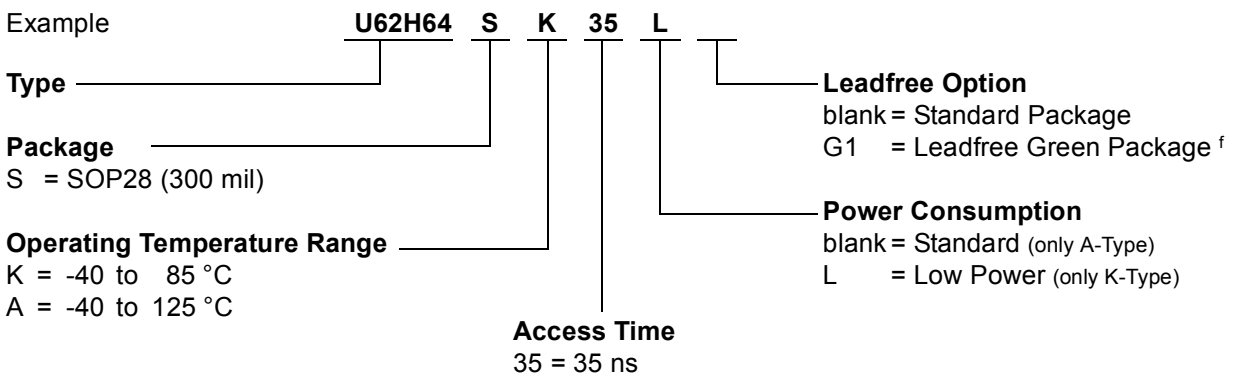


^e In measurement of $t_{dis(E)}$, $t_{dis(W)}$, $t_{dis(G)}$, $t_{en(E)}$, $t_{en(W)}$, $t_{en(G)}$ the capacitance is 5 pF.

| Capacitance | Conditions | Symbol | Min. | Max. | Unit |
|--------------------|--|--------|------|------|------|
| Input Capacitance | $V_{CC} = 5.0\text{ V}$ $V_I = V_{SS}$ | C_I | | 8 | pF |
| Output Capacitance | $f = 1\text{ MHz}$ $T_a = 25\text{ }^\circ\text{C}$ | C_O | | 10 | pF |

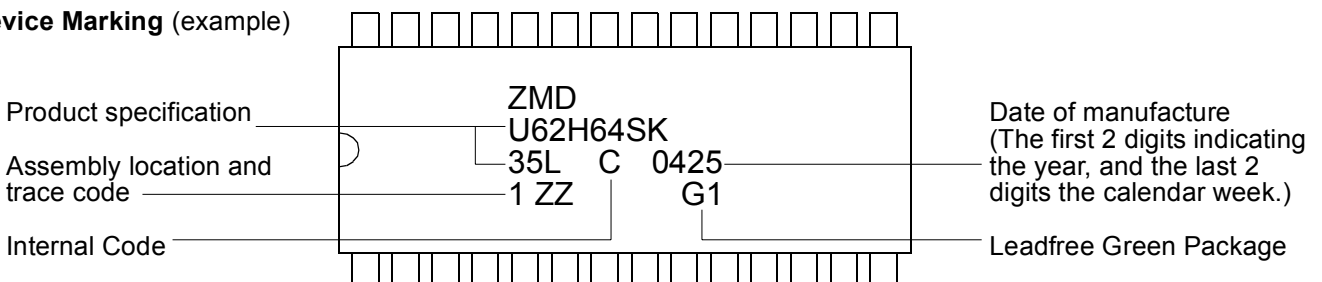
All pins not under test must be connected with ground by capacitors.

Ordering Code

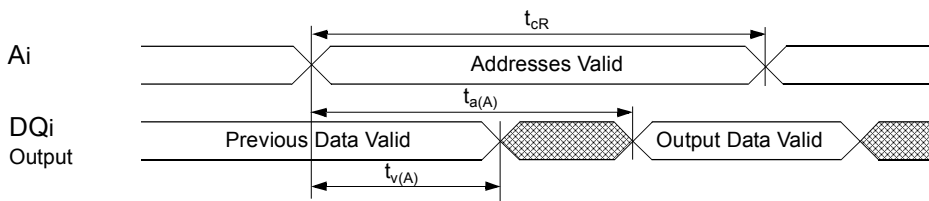


^f on special request

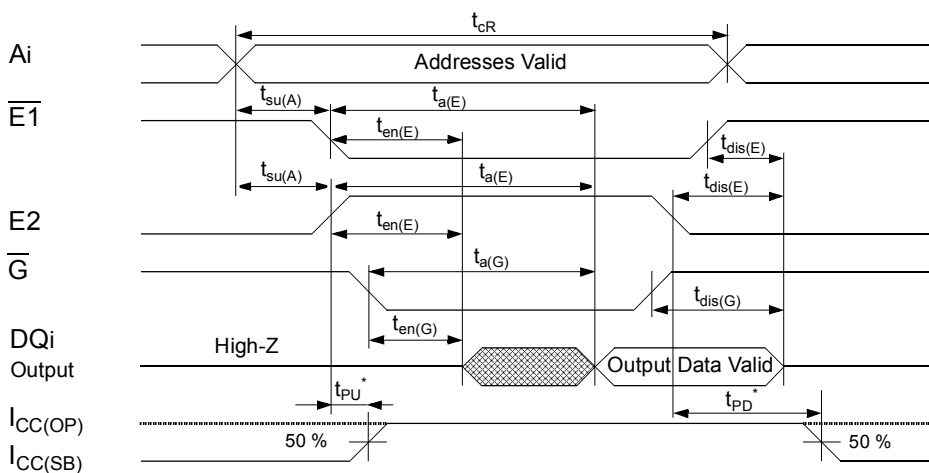
Device Marking (example)



Read Cycle 1 (during Read cycle: $\overline{E1} = \overline{G} = V_{IL}$, $E2 = \overline{W} = V_{IH}$, A_i -controlled)

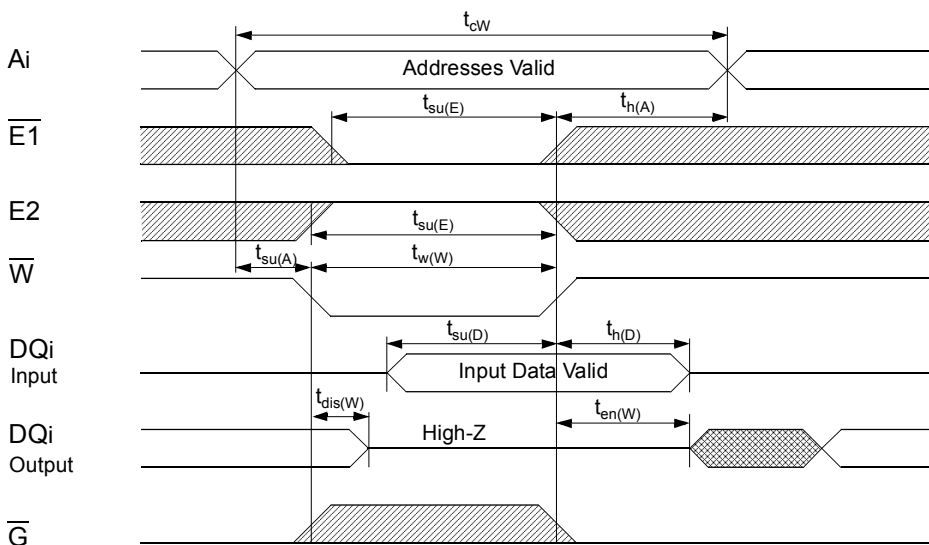


Read Cycle 2 (during Read cycle: $\overline{W} = V_{IH}$, \overline{G} -, $\overline{E1}$ - or $E2$ -controlled)



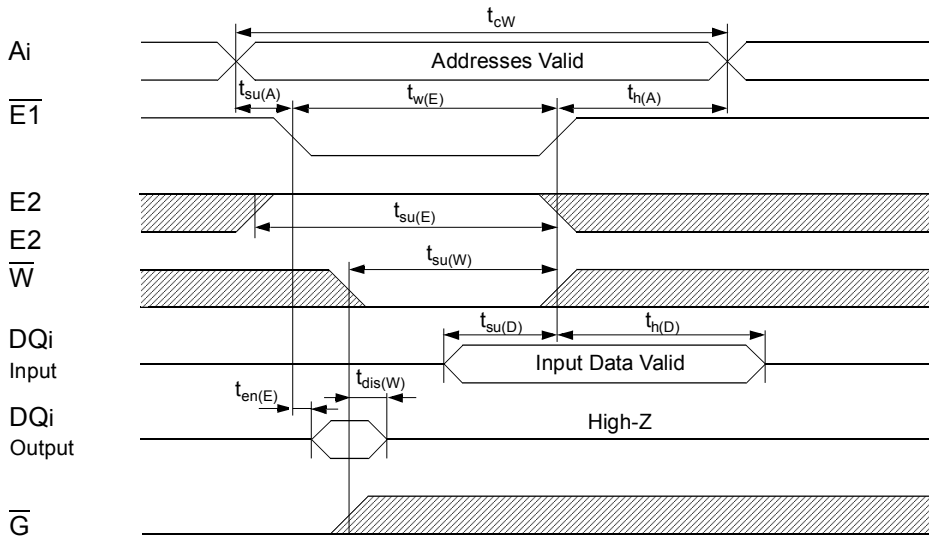
* The same applies to $\overline{E1}$

Write Cycle 1 (\overline{W} -controlled)

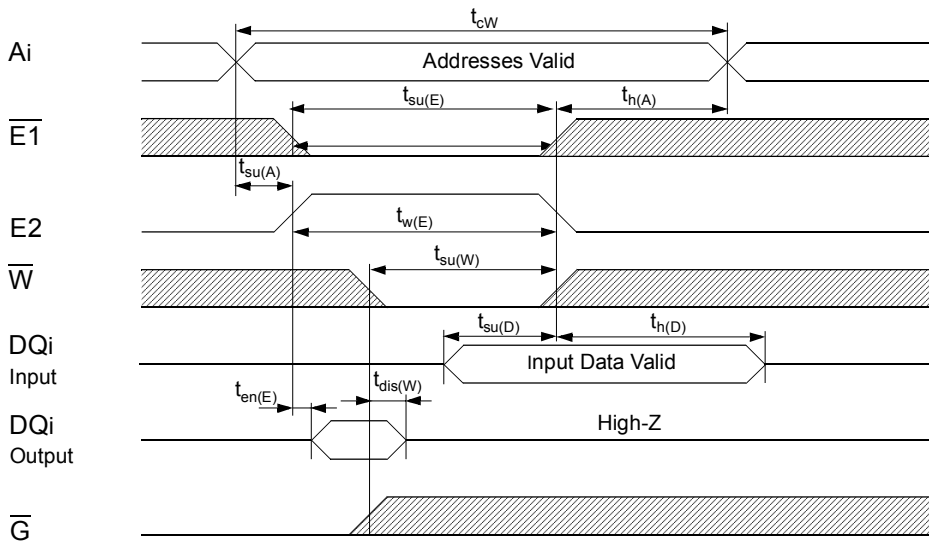


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Write Cycle 2 ($\overline{E1}$ -controlled)



Write Cycle 3 (E2-controlled)



undefined



L- or H-level



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