μPD42270
NTSC Field Buffer

June 1990

Description

The μPD42270 is a field buffer designed for NTSC TV applications and for other applications where serial data is needed. Equipped with four planes of 263-line by 910-bit storage, the μPD42270 can execute serial write and read cycles on any of the 263 lines. Within a line, four planes of 910 bits each may be written or read at the NTSC sampling rate of $4f_{SC}$.

Each of the four planes in the μPD42270 is equipped with two ports, one each for the write and read data registers. Each of the registers is split into two 455-bit segments but functions as if it were organized as one scan line of 910 bits. Independent control of write and read operation makes it possible for the device to operate synchronously or asynchronously at a clock frequency of 14.3 MHz or higher.

The synchronous option simplifies interframe luminance (Y) and chrominance (C) separation and interfield noise reduction and makes it easy to obtain a one-field delay line for digital TV and VCR applications requiring NTSC $4f_{SC}$ sampling. To obtain a very long delay, field length can be configured from 260 to 263 lines and line length of the last line from 896 to 910 bits.

The asynchronous option is useful in applications such as frame synchronization and time base correction, where line jump, line hold, line reset and pointer clear functions are required to support special effects in TV field processing.

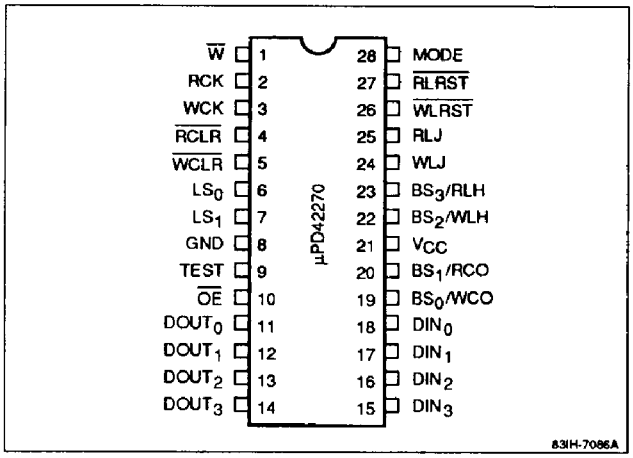
Regular refreshing of the device's dynamic storage cells is performed automatically by an internal circuit. All inputs and outputs, including clocks, are TTL-compatible. The μPD42270 is packaged in a 400-mil, 28-pin plastic DIP and is guaranteed for operation at −20 to +70°C.

Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42270C-60	40 ns	60 ns	28-pin plastic DIP

Pin Configuration

28-Pin Plastic DIP



Features

- Three functional blocks
  - — Four 263-line x 910-bit storage planes
  - — Four 910-bit write registers, one for each plane
  - — Four 910-bit read registers, one for each plane
- Two data ports: serial write and serial read
- Asynchronous operation
  - — Dual-port accessibility
  - — Carry-out feature to indicate position of scan line
  - — Line jump, line hold, line reset, and pointer clear functions
- Synchronous operation
  - — Variable field length: from 260 to 263 lines
  - — Variable last line length: from 896 to 910 bits
- Automatic refreshing
- CMOS technology
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs
- Single + 5-volt power supply
- On-chip substrate bias generator
- Standard 400-mil, 28-pin plastic DIP packaging

Pin Identification

Symbol	Function
D_{IN0} - D_{IN3}	Write data inputs
D_{OUT0} - D_{OUT3}	Read data outputs
$\overline{W}$	Write enable
$\overline{OE}$	Output enable
WCK	Write clock input
RCK	Read clock input
$\overline{WCLR}$	Write pointer clear
$\overline{RCLR}$	Read pointer clear
$\overline{WLRST}$	Write line reset
$\overline{RLRST}$	Read line reset
WLJ	Write line jump
RLJ	Read line jump
WLH	Write line hold
RLH	Read line hold
WCO	Write data register carry output
RCO	Read data register carry output
LS_0 - LS_1	Line select inputs
BS_0 - BS_3	Bit select inputs
MODE	Synchronous/asynchronous control
GND	Ground
V_{CC}	+5-volt power supply
TEST	Test pin (connect to GND in system)

Pin Functions

D_{IN0} - D_{IN3}. These pins function as write data inputs, e.g., for $4f_{SC}$ composite color or brightness signals.

D_{OUT0} - D_{OUT3}. These pins are three-state read data outputs.

$\overline{W}$. A low level on $\overline{W}$ enables write operation. $\overline{W}$ must be kept low throughout the entire scan line to ensure that data is stored serially; if $\overline{W}$ goes high any time during the WCK clock sequencing for a line, write operation will be disabled for the half of the line (455 bits) being written. The write address pointer increments in synchronization with WCK, regardless of $\overline{W}$.

$\overline{OE}$. This signal controls read data output. When $\overline{OE}$ is low, read data is output on D_{OUT0}-D_{OUT3}. When $\overline{OE}$ is high, D_{OUT0} - D_{OUT3} are in a state of high impedance. The read address pointer is incremented by RCK, regardless of the signal level of $\overline{OE}$.

WCK The rising edge of WCK latches write data from D_{IN0} - D_{IN3}. Each time this signal is activated, the write bit pointer increments sequentially and 4 bits of data are sampled and loaded into the write register. Although the register functions as one scan line of 910 bits, data is moved into and out of it in blocks of 455 x 4 bits. While 455 serial write cycles are being executed in one-half of the register, the 455 addresses previously written to the other half are simultaneously transferred to storage. Writing continues in this manner, alternating between the two halves of the register. Automatic refreshing and data transfer timing decisions are made by the internal arbitration circuit after each block of 455 addresses has been written.

RCK. The rising edge of RCK initiates read operation. Each time this signal is activated, the bit pointer increments by 1 and serial read cycles are executed in the read register. Although the register functions as one scan line of 910 bits, data is moved into and out of it in blocks of 455 x 4 bits. While 455 serial read cycles are being executed in one-half of the register, the 455 addresses previously read out of the other half are replaced by data from the storage array. Reading continues in this manner, alternating between the two halves of the register. Automatic refreshing and data transfer timing decisions are made by the arbitration circuit after each block of 455 addresses has been read. In synchronous operation, WCK controls read cycles and RCK is not used.

$\overline{WCLR}$. When $\overline{WLRST}$ is high, $\overline{WCLR}$ can be brought low to clear the write pointers to address 0 of the data register and scan line 0 of the storage array. At least one rising edge of WCK must occur while $\overline{WCLR}$ is held low for a minimum of 3 μs to ensure clearing of both pointers. The clear function ends when $\overline{WCLR}$ goes high. If $\overline{WLRST}$ is still high, the next rising edge of WCK writes the data on D_{IN0} - D_{IN3} into address 0 of the write register.

$\overline{RCLR}$. When $\overline{RLRST}$ is high, $\overline{RCLR}$ can be brought low to clear the read pointers to address 0 of the data register and scan line 0 of the storage array (asynchronous operation only). At least one rising edge of RCK must occur while $\overline{RCLR}$ is held low for a minimum of 3 μs to ensure clearing of both pointers. The clear function ends when $\overline{RCLR}$ goes high. If $\overline{RLRST}$ is still high, the data from address 0 is read out on D_{OUT0} - D_{OUT3} and the next rising edge of RCK initiates data access from address 1.

$\overline{WLRST}$. This pin is used in synchronous or asynchronous operation to reset the bit pointer to address 0 of the line following the one to which the signal is applied. In standard write operation, the scan line pointer increments by 1 whenever the bit pointer reaches the last address of a line. If $\overline{WCLR}$ is high, $\overline{WLRST}$ can be brought low for a minimum of 3 μs to force an end-of-

line condition, whereby write cycles begin executing from address 0 of the next sequential scan line. When used in conjunction with WLH, $\overline{\text{WLRST}}$ resets the current scan line; when combined with WLJ, $\overline{\text{WLRST}}$ begins writing from address 0 of the line to which the scan line pointer is jumped.

$\overline{\text{RLRST}}$. This pin is valid in asynchronous operation and can be used to reset the bit pointer to address 0 of the read line following the one to which the signal is applied. In standard read operation, the scan line pointer increments by 1 whenever the bit pointer reaches the last address of a line. If $\overline{\text{RCLR}}$ is high, $\overline{\text{RLRST}}$ can be brought low for a minimum of 3 μs to force an end-of-line condition, whereby read cycles begin executing from address 0 of the next sequential scan line. When used in conjunction with RLH, $\overline{\text{RLRST}}$ resets the current scan line; when combined with RLJ, $\overline{\text{RLRST}}$ begins reading from address 0 of the line to which the scan line pointer is jumped.

WLJ. Each positive pulse of this signal increments the write scan line pointer by one line (asynchronous operation only). WLJ is sampled at the rising edge of WCK. If WLJ is high, a single jump is executed. If WLJ remains high, no further jumps occur. To jump again, WLJ must go low for at least one rising edge of WCK before going high again. It takes a minimum of two WCK cycles to complete a line jump. The first cycle senses the high level of WLJ and increments the scan line pointer. An additional WCK cycle with WLJ low is required to complete the function. If more than one line jump is needed, then the sequence must be repeated. A line jump occurs either when the current line has been completely filled or after $\overline{\text{WLRST}}$ has reset the write address. The new scan line can be calculated by n+11+1x (where "n" is the current line and "x" equals the number of positive WLJ pulses). Changes in the level of WLJ must be made when the bit pointer is between locations 229 and 909 of the current line and when $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ are high and WLH is low.

RLJ. Each positive pulse of this signal increments the read scan line pointer by one line (asynchronous operation only). RLJ is sampled at the rising edge of RCK. If RLJ remains high, a single line jump is executed. To jump again, RLJ must go low for at least one rising edge of RCK before going high again. It takes a minimum of two RCK cycles to complete a line jump. The first cycle senses the high level of RLJ and increments the scan line pointer. An additional RCK cycle with RLJ low is required to complete the function.If more than one line jump is needed, then this sequence must be repeated.

A line jump occurs either when the current line has been completely read or after $\overline{\text{RLRST}}$ has reset the read address. The new scan line can be calculated by n+ 1+x (where "n" is the current line and "x" equals the number of positive RLJ pulses).

Changes in the level of RLJ must be made when the bit pointer is between locations 682 and 909 of the previous line, or between 0 and 452 of the current line, and when $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$ are high and RLH is low.

WLH. Once this input is applied, the write scan line pointer will hold its position even if successive write clocks are applied. The level of WLH is sampled at the rising edge of WCK and must be applied between locations 229 and 909 of the line to be held. The held line is released after 910 addresses have been rewritten or after $\overline{\text{WLRST}}$ resets the write line address. WLH is multiplexed with BS_2 and is valid in asynchronous operation only. WLH (high) must be input only when $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ are high and WLJ is low.

RLH. Once this input is applied, the read scan line pointer will hold its position even if successive read clocks are applied. The level of RLH is sampled at the rising edge of RCK and must be clocked between locations 682 and 909 of the line preceding the line to hold, or between locations 0 and 452 of the line to hold. The held line is released after 910 addresses have been read or after $\overline{\text{RLRST}}$ resets the read line address. RLH (high) must be input only when $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$ are high and RLJ is low. RLH is multiplexed with BS_3 and is valid in asynchronous operation only.

WCO. When the bit pointer reaches address 909 of the write data register, this signal goes high for one WCK cycle. WCO is multiplexed with BS_0 and is valid in asynchronous operation only.

RCO. When the bit pointer reaches address 909 of the read data register, this signal goes high for one RCK cycle. RCO is multiplexed with BS_1 and is valid in asynchronous operation only.

BS_0 - BS_3. These pins control the number of bits in the last line of the field. The combined signals of BS_0-BS_3 set the line length from 896 to 910 bits in one-bit steps (table 1). The length of the last line can change for each field, but all four pins should not be set low. BS_0, BS_1, BS_2 and BS_3 are multiplexed with WCO, RCO, WLH and RLH, respectively, and are valid in synchronous operation only. In asynchronous operation, the line length is fixed at 910 bits.

LS_0 - LS_1. These pins control the number of lines for one field in either synchronous or asynchronous operation. The combined signals of LS_0 and LS_1 set the number of lines to 260, 261, 262, or 263 (table 2). The number of lines can be changed for each field.

MODE. This pin selects the operating mode. A low signal selects synchronous operation and a high signal selects asynchronous operation. If MODE is changed after power has been applied to the μPD42270, it is necessary to clear the address pointers by bringing $\overline{WCLR}$ and $\overline{RCLR}$ low. MODE can be changed at any time; however, data input in one mode may be unreliable in the other (see table 3 for valid pin functions).

Table 1. Line Length Adjustment

BS_3	BS_2	BS_1	BS_0	Number of Bits in the Last Line
L	L	L	L	Prohibited
L	L	L	H	896
L	L	H	L	897
L	L	H	H	898
L	H	L	L	899
L	H	L	H	900
L	H	H	L	901
L	H	H	H	902
H	L	L	L	903
H	L	L	H	904
H	L	H	L	905
H	L	H	H	906
H	H	L	L	907
H	H	L	H	908
H	H	H	L	909
H	H	H	H	910

Notes:

(1) LS_0 - LS_1 and BS_0 - BS_3 must be held at a stable high or low level to maintain the number of bits per scan line and the number of scan lines per field while the line pointer indicates the position between lines 258 and 262.

Table 2. Line Number Adjustment

LS_1	LS_0	Number of Lines
L	L	260
L	H	261
H	L	262
H	H	263

Notes:

(1) LS_0 - LS_1 and BS_0 - BS_3 must be held at a stable high or low level to maintain the number of bits per scan line and the number of scan lines per field while the line pointer indicates a position between lines 258 and 262.

Table 3. Valid Pin Functions According to Mode

Pin Name	Synchronous Mode (Note 1)	Asynchronous Mode (Note 2)
MODE	0	1
BS_0/WCO	BS_0	WCO
BS_1/RCO	BS_1	RCO
BS_2/WLH	BS_2	WLH
BS_3/RLH	BS_3	RLH
$\overline{RCLR}$	Invalid	Valid
RCK	Invalid	Valid
$\overline{RLRST}$	Invalid	Valid
$\overline{WCLR}$	Valid	Valid
WCK	Valid	Valid
$\overline{WLRST}$	Valid	Valid
WLJ	Invalid	Valid
RLJ	Invalid	Valid

Notes:

(1) Write and read cycles are controlled by $\overline{WCLR}$, WCK, and $\overline{WLRST}$ in synchronous operation.

(2) In asynchronous operation, write and read cycles are controlled independently.

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; GND = 0 V; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	D_{IN0} - D_{IN3}, $\overline{W}$, $\overline{OE}$, WCK, RCK, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$, WLJ, RLJ, LS_0 - LS_1, BS_2/WLH, BS_3/RLH, MODE
I/O capacitance	$C_{I/O}$			8	pF	BS_0/WCO, BS_1/RCO
Output capacitance	C_O			7	pF	D_{OUT} - D_{OUT}

DEVICE OPERATION

The μPD42270 supports two operating modes to accommodate various NTSC TV applications. Depending on the logic level of the MODE pin, the device will execute either synchronous or asynchronous write and read cycles on the addresses specified by the internal address pointers. When selecting the mode after power-on, it is necessary to reset these pointers to starting address 0 using $\overline{WCLR}$ and $\overline{RCLR}$. The level of MODE may be changed at any time.

Synchronous Mode

In synchronous mode, write and read cycles are executed simultaneously by $\overline{WCLR}$, $\overline{WLRST}$, WCK, $\overline{W}$ and $\overline{OE}$ to create a delay line, which means that write and read addresses always coincide. After all lines within a field have been written, they then are read out as the device begins overwriting new data to the same addresses again. Field length may be configured from 260 to 263 lines and last line length from 896 to 910 bits by means of the LS and BS pins, respectively. Synchronous operation is useful in applications where a very long delay line is required and may be selected by setting MODE low.

Asynchronous Mode

In asynchronous mode, $\overline{WCLR}$, $\overline{WLRST}$, WCK and $\overline{W}$ control write cycles, while read cycles are controlled independently by $\overline{RCLR}$, $\overline{RLRST}$, RCK and $\overline{OE}$. Field length may be configured from 260 to 263 lines using LS_0 - LS_1. Line length remains fixed at 910 bits and BS_0-BS_3 are disabled to provide for the register carry out, line hold, and line jump functions. Asynchronous operation is useful for frame synchronization or time base correction and may be selected by setting MODE high.

Address Clear. Setting $\overline{WCLR}$ and $\overline{RCLR}$ low for a minimum of 3 μs during successive WCK and RCK cycles initializes the internal pointers to starting address 0 of the first scan line ($\overline{RCLR}$ is disabled in synchronous mode). Although address clear signals must meet the specifications for setup and hold times as measured from the rising edges of WCK and RCK, they are not dependent on the status of $\overline{W}$ or $\overline{OE}$. An address clear cycle cannot occur in conjunction with $\overline{WLRST}$ or $\overline{RLRST}$ line reset cycles.

Write Operation. Write cycles are executed in synchronization with WCK as $\overline{W}$ is held low. Bits are input sequentially into one of the two halves of the data register before being transferred to the storage array. Since data is transferred into the array in blocks of 455 x 4 bits, no data transfer occurs if $\overline{W}$ goes high to disable write operation before all 455 bits are written. Despite write operation being disabled, the internal bit pointer continues to increment with each successive write clock.

Read Operation. Read cycles are executed in synchronization with RCK (asynchronous operation only) or WCK (synchronous operation only) as $\overline{OE}$ is held low. If $\overline{OE}$ goes high any time during a cycle, the outputs are in a state of high impedance until OE returns low. Since the internal bit pointer increments by 1 in spite of read operation being disabled, it is always important to reset the write and read pointers using $\overline{WCLR}$ and $\overline{RCLR}$ prior to beginning or resuming operation at the first address location in the array.

Special Functions

Line Reset. A line reset is similar to an address clear cycle, except that it only affects the bit pointers within a line. While $\overline{WCLR}$ and $\overline{RCLR}$ are held high, $\overline{WLRST}$ or $\overline{RLRST}$ can be brought low for a minimum of 3 μs during successive WCK or RCK cycles to reset the bit pointer to address 0 of the scan line. At the completion of the reset cycle, the next sequential scan line will be selected unless line hold (WLH or RLH) or line jump (WLJ or RLJ) are also used. See $\overline{WLRST}$ and $\overline{RLRST}$ for more detail.

A combination of line reset and an address clear cycle must be separated by at least one serial clock cycle. The timing relationship of WCLR, $\overline{WLRST}$ and WCK (or RCLR, $\overline{RLRST}$ and RCK) is shown in figure 1.

In asynchronous operation, $\overline{WLRST}$ and $\overline{RLRST}$ independently reset the write and read bit pointers. During synchronous operation, $\overline{WLRST}$ resets both pointers.

Line Jump. With the line jump function, it is possible to advance the current write or read line position according to the number of positive WLJ or RLJ pulses applied (see descriptions for the WLJ and RLJ pins). In this cycle, which is valid in asynchronous mode only, the scan line pointer resets to address 0 if the number of positive pulses causes the resulting line number (n+11+1x, where "n" is the current line number and "x" is the number of positive WLJ or RLJ pulses) to exceed the maximum line number (number of lines minus 1) specified by the LS_0 and LS_1 pins (table 2).

Line Hold. The line hold feature is available in asynchronous mode only and can be used to prevent the internal scan line pointers from incrementing to the next sequential address. The read and write line pointers may be held independently; however, restrictions pertaining to when this function can be initiated, detailed in the descriptions for the WLH and RLH pins, should be carefully followed.

Block Diagram

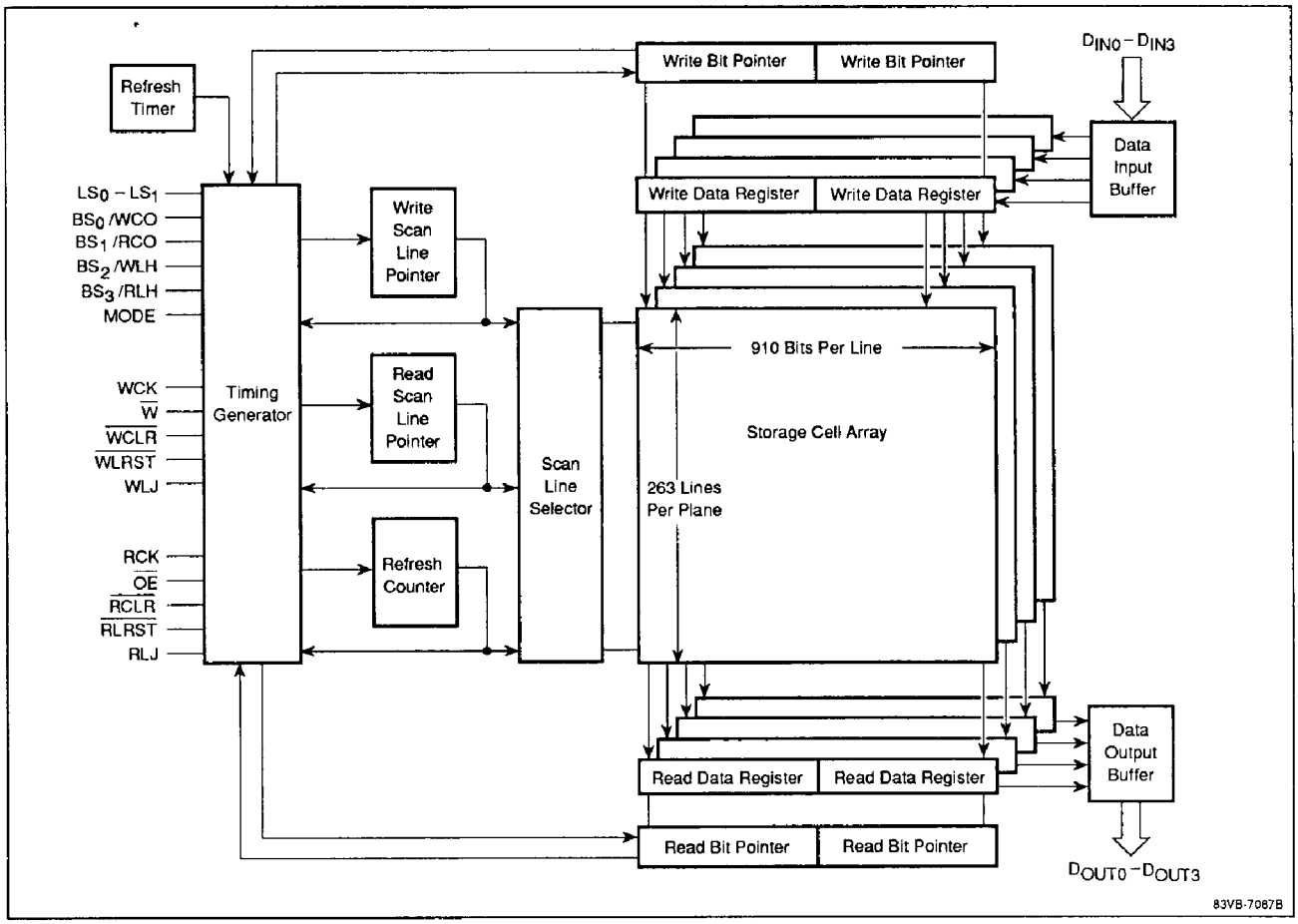
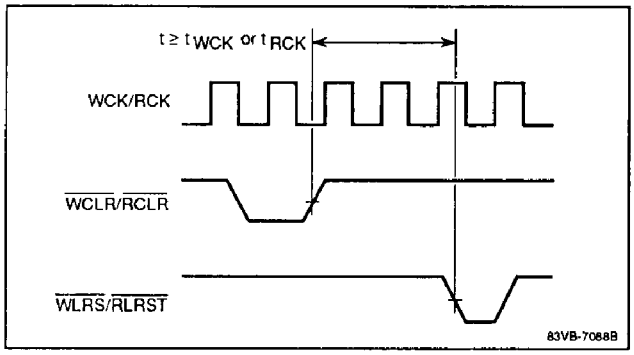


Figure 1. Separation of Clear and Reset Signals



Absolute Maximum Ratings

Supply voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.5 to +7.0 V
Supply voltage on V_{CC} relative to GND, V_{R2}	−1.5 to +7.0 V
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Ambient temperature	T_A	−20		70	°C

DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA
Standby current	I_{CC1}		6	20	mA	WCK, RCK = V_{IL}
Operating current	I_{CC2}		40	80	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Access time from RCK	t_{AC}		40	ns	
Write clock cycle time	t_{WCK}	60		ns	(Note 5)
Write clock active pulse width	t_{WCW}	20		ns	
Write clock precharge time	t_{WCP}	20		ns	
Read clock cycle time	t_{RCK}	60		ns	(Note 5)
Read clock active pulse width	t_{RCW}	20		ns	
Read clock precharge time	t_{RCP}	20		ns	
Output hold time	t_{OH}	5		ns	
Output low impedance delay	t_{LZ}	5	40	ns	(Note 6)
Data output buffer high impedance delay	t_{HZ}	5	40	ns	(Note 7)
Input data setup time	t_{DS}	15		ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input data hold time	t_{DH}	3		ns	
$\overline{WCLR}$ ($\overline{RCLR}$) setup time before the rising edge of WCK (RCK)	t_{CS}	20		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) hold time after the rising edge of WCK (RCK)	t_{CH}	3		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) invalid hold time after the rising edge of WCK (RCK)	t_{CN1}	5		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) invalid setup time before the rising edge of WCK (RCK)	t_{CN2}	20		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) low level valid time	t_{CLR}	3		μs	
$\overline{WLRST}$ ($\overline{RLRST}$) setup time before the rising edge of WCK (RCK)	t_{LRS}	20		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) hold time after the rising edge of WCK (RCK)	t_{LRH}	3		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) invalid hold time after the rising edge of WCK (RCK)	t_{LRN}	5		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) invalid setup time before the rising edge of WCK (RCK)	t_{LRN}	20		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) low level valid time	t_{LRST}	3		μs	
$\overline{W}$ setup time before the rising edge of WCK	t_{WS}	20		ns	(Note 9)
$\overline{W}$ hold time after the rising edge of WCK	t_{WH}	3		ns	(Note 9)
$\overline{W}$ valid hold time after subline (1/2) switch	t_{WN1}	5		ns	(Note 9)
$\overline{W}$ valid setup time before subline (1/2) switch	t_{WN2}	20		ns	(Note 9)
WLH (RLH) setup time before the rising edge of WCK (RCK)	t_{LHS}	20		ns	
WLH (RLH) hold time after the rising edge of WCK (RCK)	t_{LHH}	3		ns	
WLH invalid hold time measured from the end of write cycle 227	t_{WHN1}	5		ns	
WLH invalid setup time measured before write cycle 0	t_{WHN2}	20		ns	
RLH invalid hold time measured from the end of read cycle 681	t_{RHN1}	5		ns	
RLH invalid setup time measured before read cycle 453	t_{RHN2}	20		ns	
WLJ (RLJ) setup time before the rising edge of WCK (RCK)	t_{LJS}	20		ns	
WLJ (RLJ) hold time after the rising edge of WCK (RCK)	t_{LJH}	3		ns	
WLJ hold time measured from the end of write cycle 227	t_{WJN1}	5		ns	
WLJ setup time measured before write cycle 0	t_{WJN2}	20		ns	
RLJ hold time measured from the end of read cycle 681	t_{RJN1}	5		ns	
RLJ setup time measured before read cycle 453	t_{RJN2}	20		ns	
$\overline{OE}$ setup time before the rising edge of RCK (WCK)	t_{OES}	20		ns	(Note 9)
$\overline{OE}$ hold time after the rising edge of RCK (WCK)	t_{OEH}	3		ns	(Note 9)
$\overline{OE}$ valid hold time after the rising edge of RCK (WCK)	t_{OEN1}	5		ns	(Note 9)
$\overline{OE}$ valid setup time before the rising edge of RCK (WCK)	t_{OEN2}	20		ns	(Note 9)
LS, BS setup time before WCK (RCK), line 258	t_{FSS}	0		ns	
LS, BS hold time after WCK (RCK), line 0	t_{FSH}	3		μs	
Write carry output high level delay	t_{WCLH}		40	ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Write carry output low level delay	t_{WCHL}		40	ns	
Read carry output high level delay	t_{RCLH}		40	ns	
Read carry output low level delay	t_{RCHL}		40	ns	
Transition time	t_T	3	35	ns	(Note 4)

Notes:

(1) All voltages are referenced to GND

(2) Ac measurements assume t_T = 5 ns.

(3) Input timing reference levels = 1.5 V; input levels are measured between GND and 3.0 V; output levels are measured between 0.8 and 2.0 V. See figures 2 and 3.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = −20 to 70°C) is assured.

(6) This delay is measured at −200 mV from the steady-state voltage with the load specified in figure 5.

(7) This delay is measured at the maximum steady-state output high voltage −200 mV or the minimum steady-state output low voltage +200 mV with the load specified in figure 5.

(8) For proper execution of the pointer clear and line reset functions, specifications for t_{CS}, t_{CH}, t_{CN1}, t_{CN2}, t_{LRS}, t_{LRH}, t_{LRN1} and t_{LRN2} must be met; otherwise, these functions may not affect the desired cycles or may affect adjacent cycles erroneously.

(9) If a $\overline{W}$ (or $\overline{OE}$) pulse does not satisfy the specifications for t_{WS}, t_{WH}, t_{WN1} and t_{WN2} (or t_{OES}, t_{OEH}, t_{OEN1} and t_{OEN2}), the write disable function (output high impedance) being executed may not affect the desired cycles or may affect adjacent cycles erroneously.

(10) For the μPD42270 to read new data, read operation must be delayed from write operation by at least 920 cycles. In those cases where the delay is less than 920 cycles, read data will vary as shown below:

Source of Read Data	Delay Between Write and Read Operation
Old data	0 to 450 cycles
Indeterminate (either old or new data)	451 to 919 cycles
New data	920 or more cycles

Figure 2. Input Timing

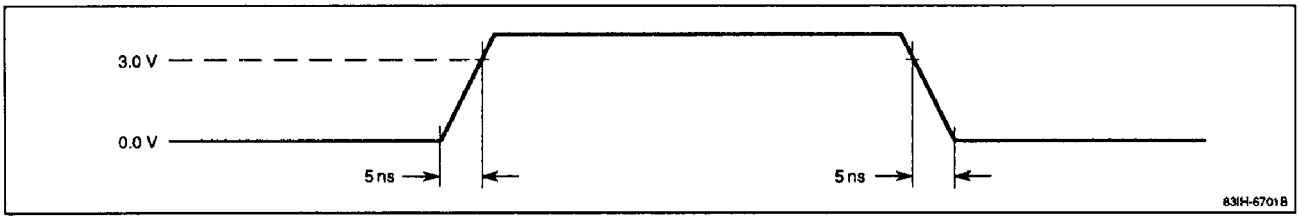


Figure 3. Output Timing

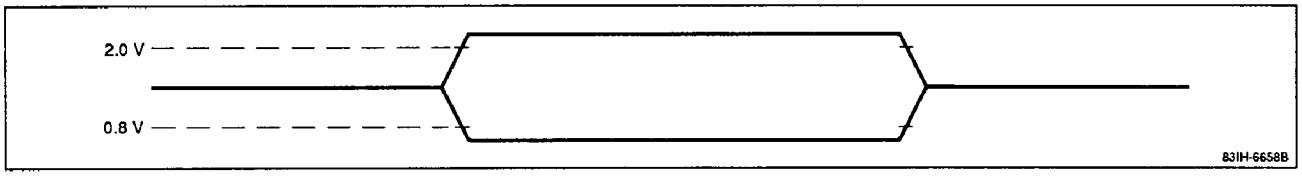


Figure 4. Output Loading for t_{AC}, t_{OH}, t_{WCLH}, t_{WCHL}, t_{RCLH}, t_{RCHL}

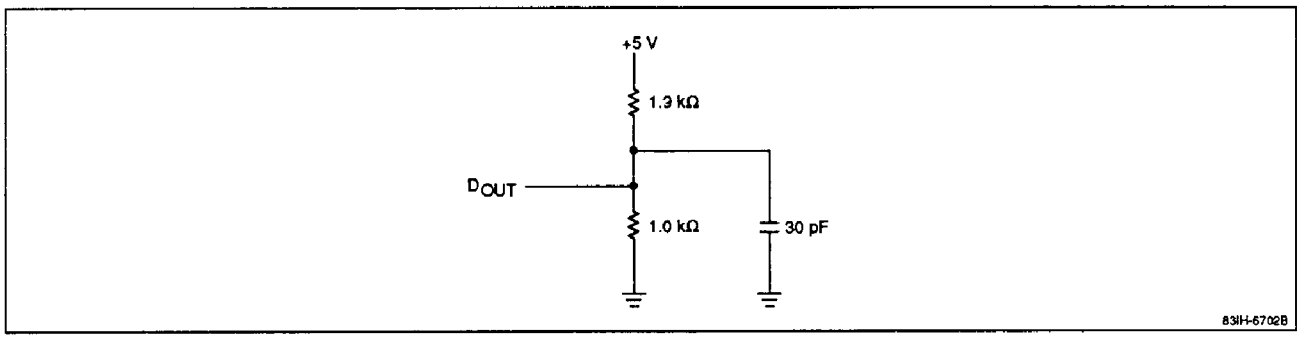
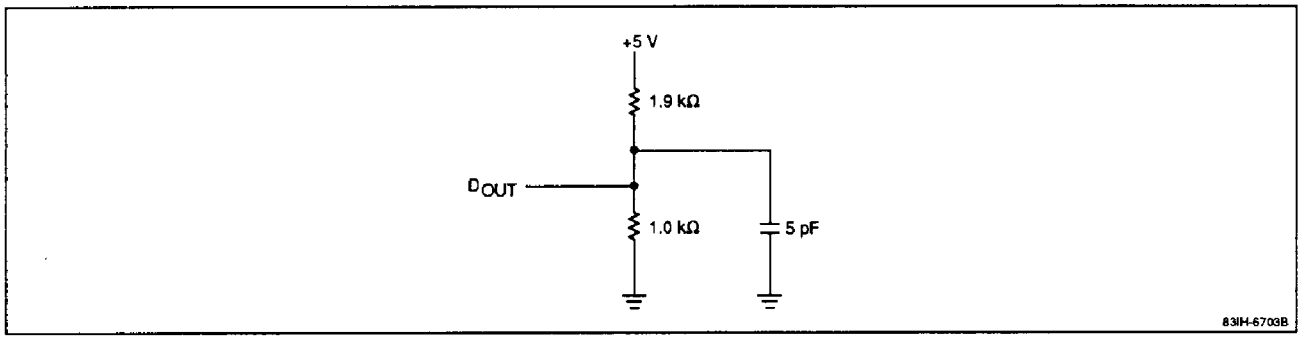
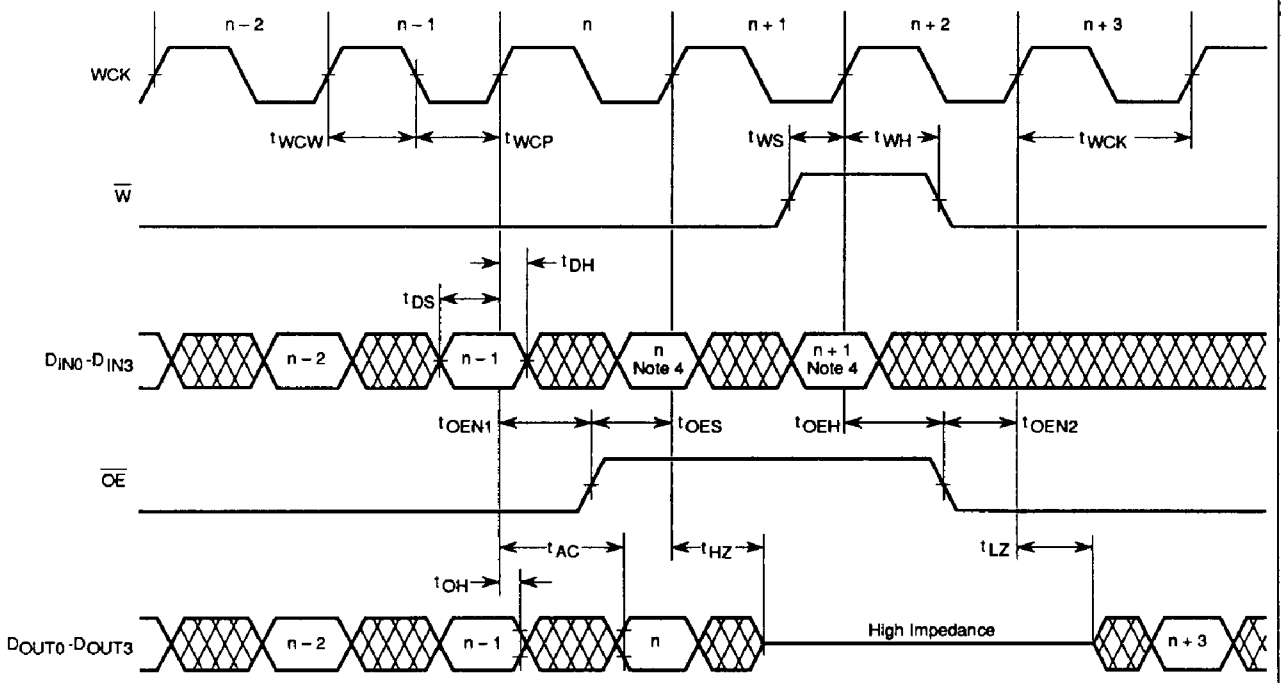


Figure 5. Output Loading for t_{LZ} and t_{HZ}



Timing Waveforms

Synchronous Write/Read Cycle



Notes:

[1] In synchronous mode, output data is delayed by one field from the input data.

[2] $\overline{WLRST} = \overline{WCLR} = V_{IH}$. MODE = V_{IL}. LS_0 and $LS_1 = V_{IH}$ or V_{IL}. $\overline{RLRST}$, $\overline{RCLR}$, and RCK are "don't care" inputs.

[3] $BS_0 - BS_3 = V_{IH}$ or V_{IL}.

[4] Data is transferred into and out of the data registers in blocks of 455 x 4 bits. When $\overline{W}$ goes high before all 455 words are input, write operation is disabled and none of the words are transferred to the storage array.

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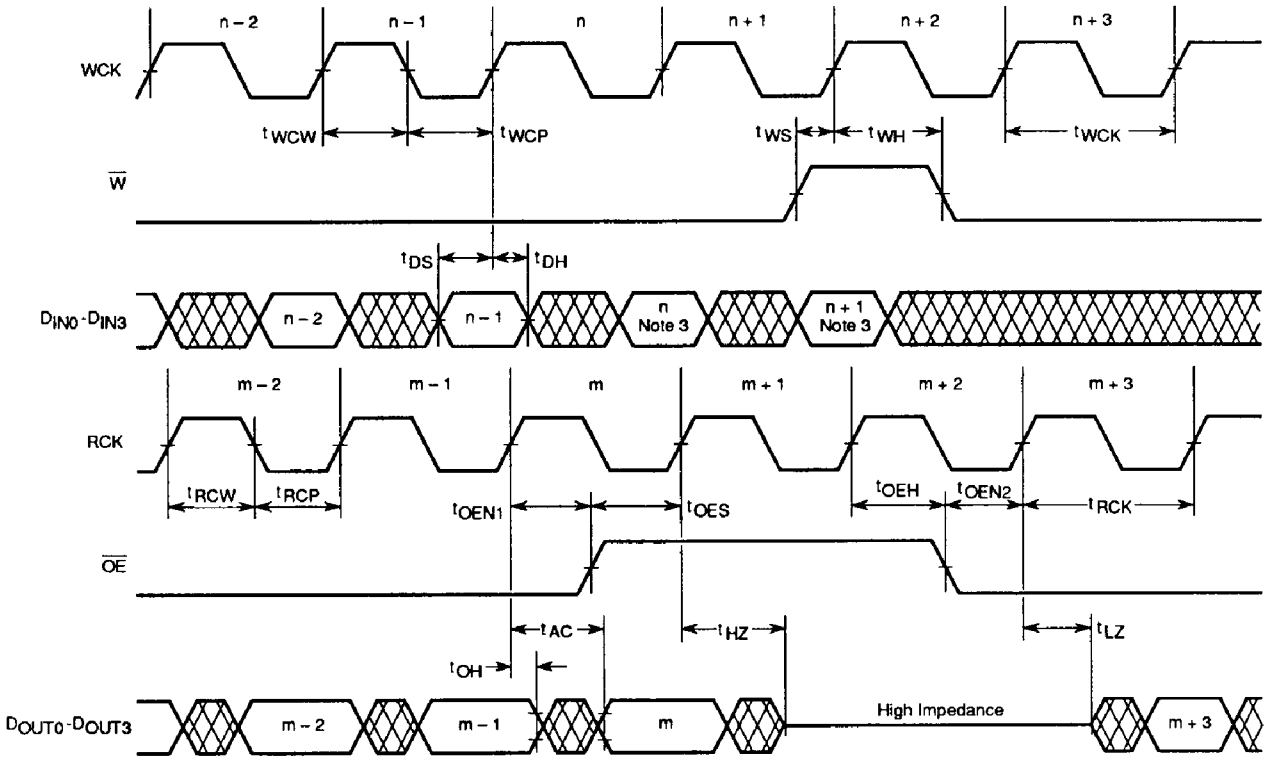
Timing Waveforms (cont)

Asynchronous Write and Read Cycles



Notes:

[1] $\overline{WCLR} = \overline{RCLR} = V_{IH}$. $\overline{WLRST} = \overline{RLRST} = V_{IH}$. MODE = V_{IH}.

[2] RLJ, WLJ, WLH, and RLH = V_{IH} or V_{IL}. LS_0 and LS_1 = V_{IH} or V_{IL}.

[3] Data is transferred into and out of the data registers in blocks of 455 x 4 bits. When $\overline{W}$ goes high before all 455 words are input, write operation is disabled and none of the words are transferred to the storage array.

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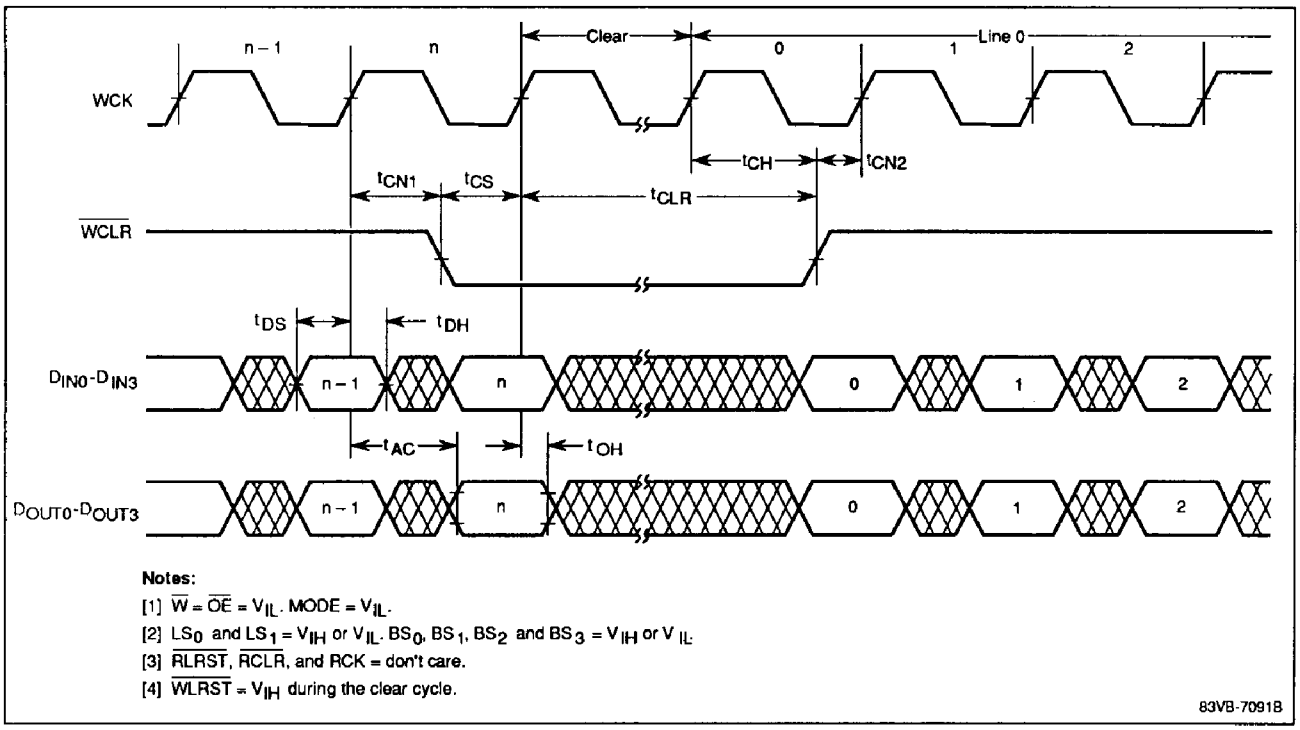
Timing Waveforms (cont)

Synchronous Pointer Clear Cycle



Notes:

[1] $\overline{W} = \overline{OE} = V_{IL}$. MODE = V_{IL}.

[2] LS_0 and $LS_1 = V_{IH}$ or V_{IL}. BS_0, BS_1, BS_2 and $BS_3 = V_{IH}$ or V_{IL}.

[3] $\overline{RLRST}$, $\overline{RCLR}$, and RCK = don't care.

[4] $\overline{WLRST} = V_{IH}$ during the clear cycle.

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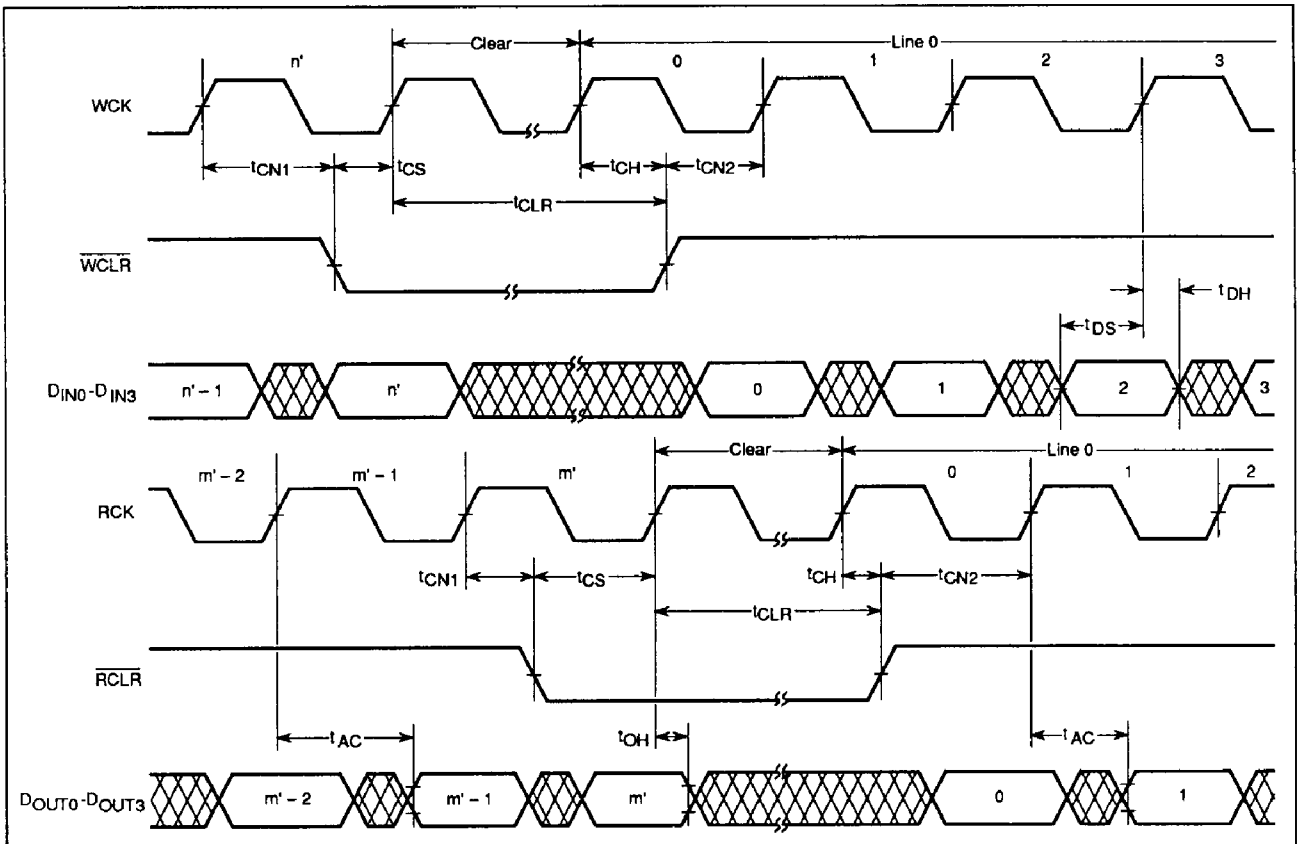
Timing Waveforms (cont)

Asynchronous Pointer Clear Cycle



Notes:

[1] $\overline{W} = \overline{OE} = V_{IL}$. MODE = V_{IH}, $\overline{WLRST}$ and $\overline{RLRST}$ = V_{IH} during clear pulse.

[2] LS_0 and LS_1 = V_{IH} or V_{IL}.

[3] WLH, RLH, WLJ and RLJ = V_{IL} during clear pulse.

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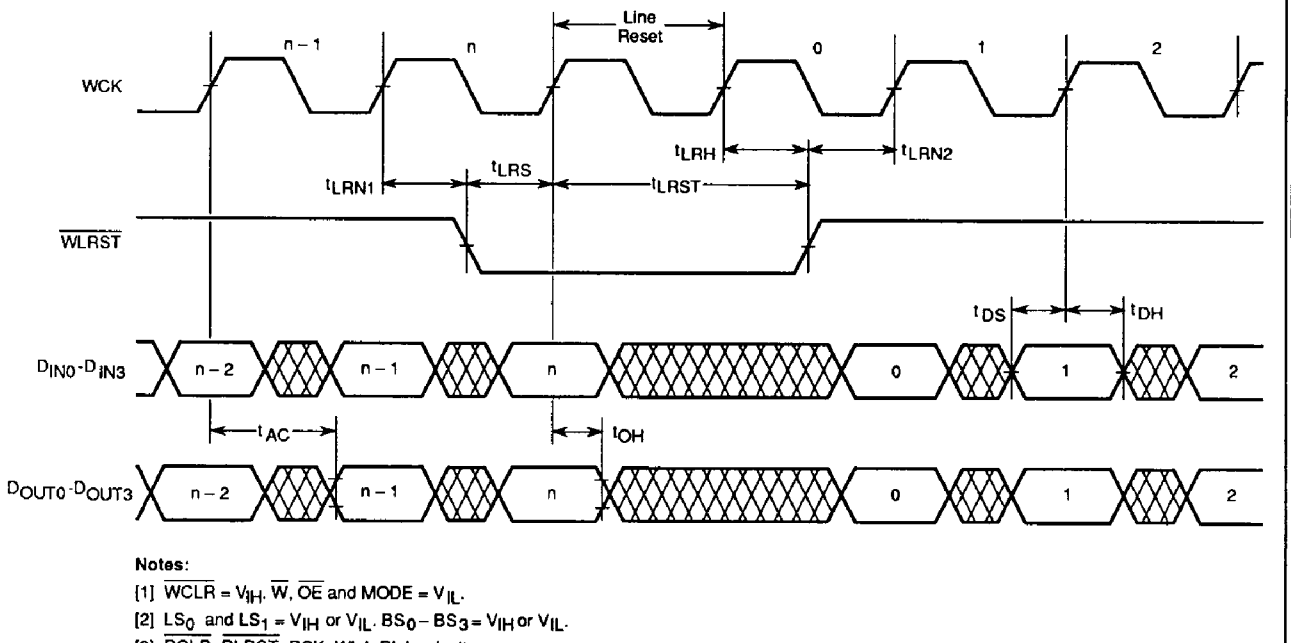
Timing Waveforms (cont)

Synchronous Line Reset Cycle



Notes:

[1] $\overline{WCLR}$ = V_{IH}. $\overline{W}$, $\overline{OE}$ and MODE = V_{IL}.

[2] LS_0 and $\overline{LS_1}$ = V_{IH} or V_{IL}. BS_0 – BS_3 = V_{IH} or V_{IL}.

[3] $\overline{RCLR}$, $\overline{RLRST}$, RCK, WLJ, RLJ = don't care.

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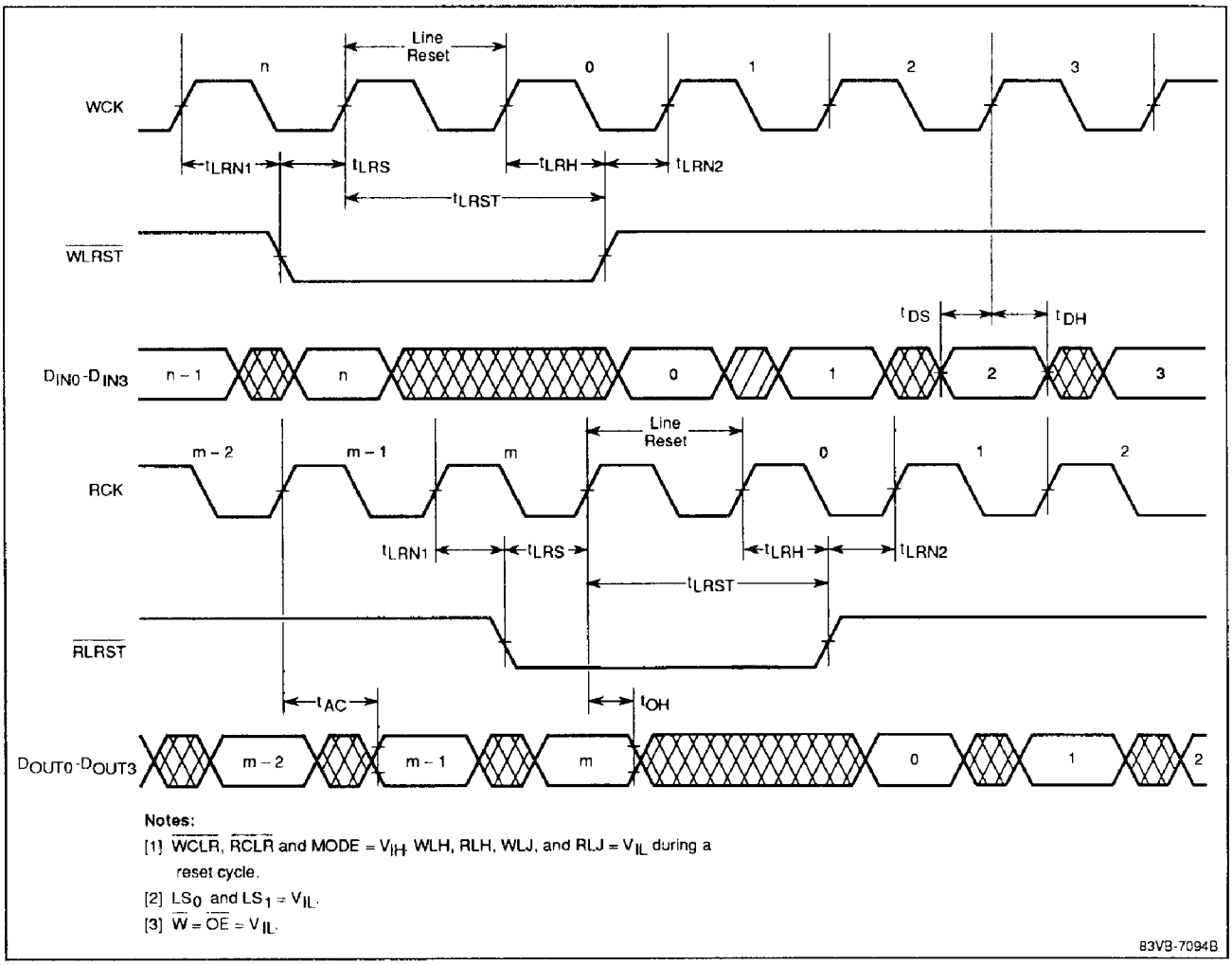
Timing Waveforms (cont)

Asynchronous Line Reset Cycle



Notes:

[1] $\overline{WCLR}$, $\overline{RCLR}$ and MODE = V_{IH}, WLH, RLH, WLJ, and RLJ = V_{IL} during a reset cycle.

[2] LS_0 and LS_1 = V_{IL}.

[3] $\overline{W}$ = $\overline{OE}$ = V_{IL}.

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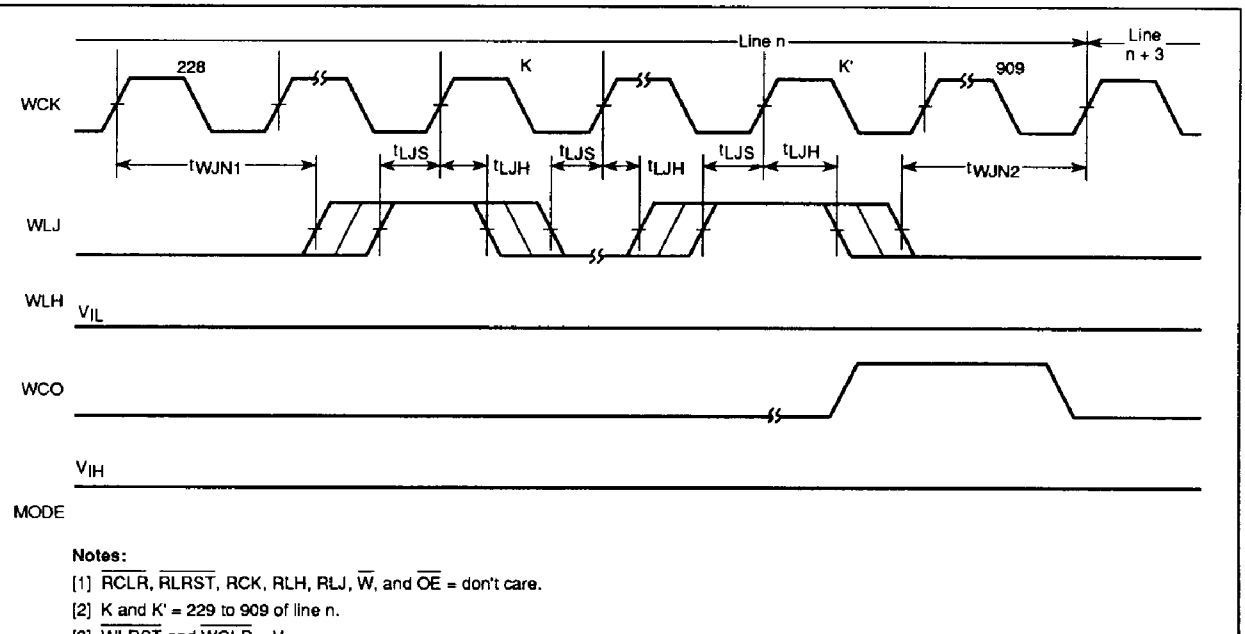
Timing Waveforms (cont)

Write Line Jump Cycle



Notes:

[1] $\overline{RCLR}$, $\overline{RLRST}$, RCK, RLH, RLJ, $\overline{W}$, and $\overline{OE}$ = don't care.

[2] K and K' = 229 to 909 of line n.

[3] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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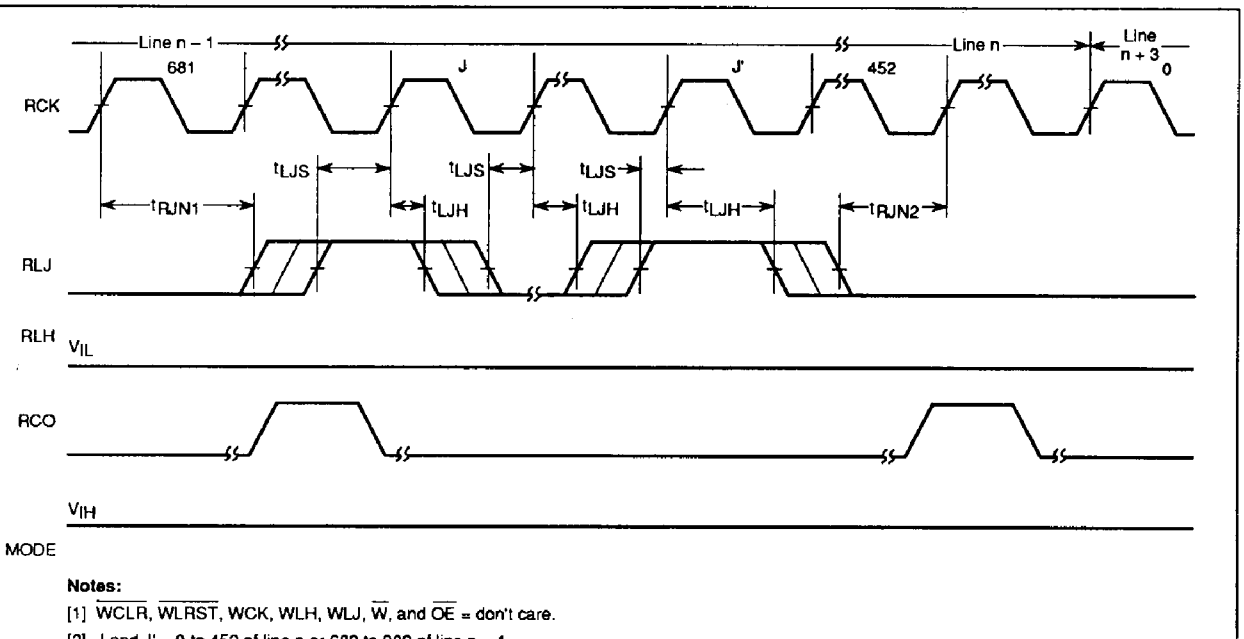
Read Line Jump Cycle



Notes:

[1] $\overline{WCLR}$, $\overline{WLRST}$, WCK, WLH, WLJ, $\overline{W}$, and $\overline{OE}$ = don't care.

[2] J and J' = 0 to 452 of line n or 682 to 909 of line n – 1.

[3] $\overline{RLRST}$ and $\overline{RCLR}$ = V_{IH}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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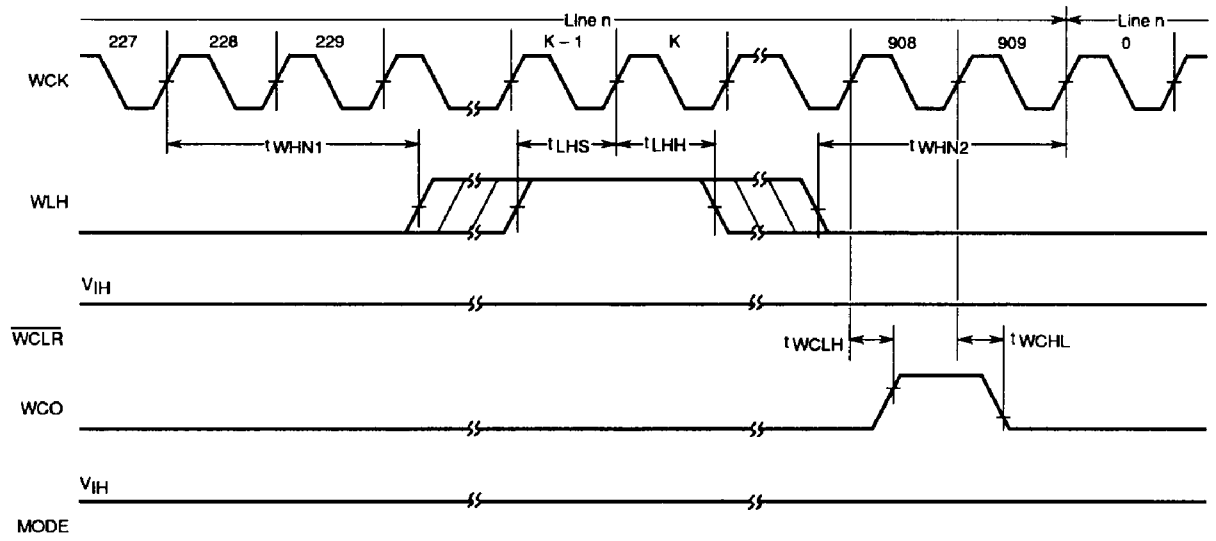
Timing Waveforms (cont)

Write Line Hold Cycle



Notes:

[1] $\overline{RLRST}$, RLJ, $\overline{W}$, RLH, $\overline{OE}$, $\overline{RCLR}$, and RCK = don't care.

[2] K = 229 to 909.

[3] $\overline{WLRST}$ = V_{IH}, WLJ = V_{IL}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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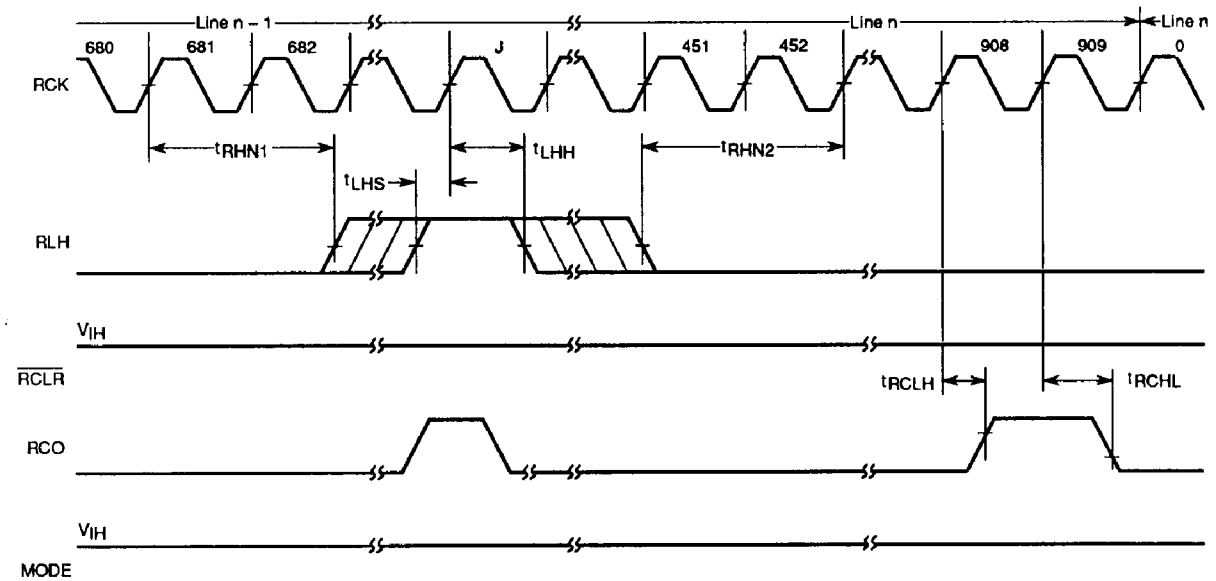
Read Line Hold Cycle



Notes:

[1] $\overline{WLRST}$, WLJ, $\overline{W}$, WLH, $\overline{OE}$, $\overline{WCLR}$, and WCK = don't care.

[2] J = 682 to 909 in $(n-1)^{th}$ or 0 to 452 in n^{th} line.

[3] $\overline{RLRST}$ = V_{IH}, RLJ = V_{IL}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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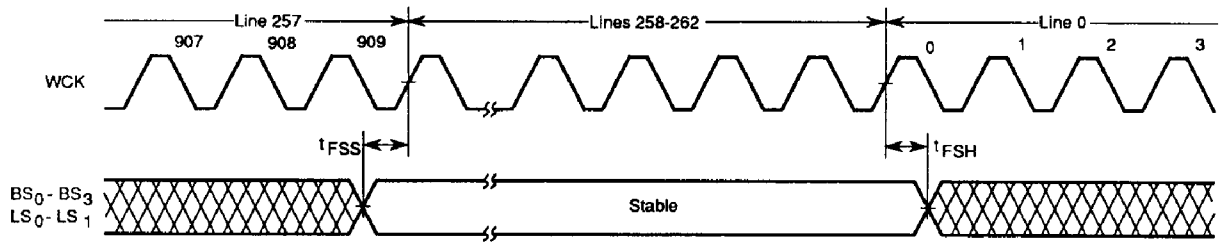
Timing Waveforms (cont)

Synchronous Field Buffer Size Adjustment



Notes:
[1] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.
[2] MODE = V_{IL}.
[3] $\overline{RLRST}$, $\overline{W}$, RCK, $\overline{RCLR}$, and $\overline{OE}$ = don't care.

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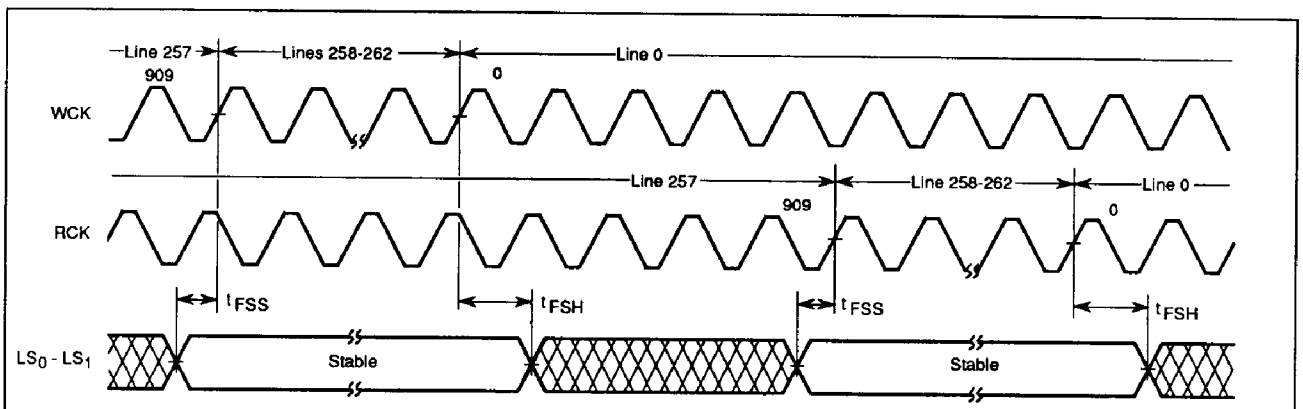
Asynchronous Field Buffer Size Adjustment



Notes:
[1] $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.
[2] MODE = V_{IH}. WLJ and RLJ = V_{IL}.
[3] $\overline{W}$, $\overline{OE}$, WLH, and RLH = don't care.

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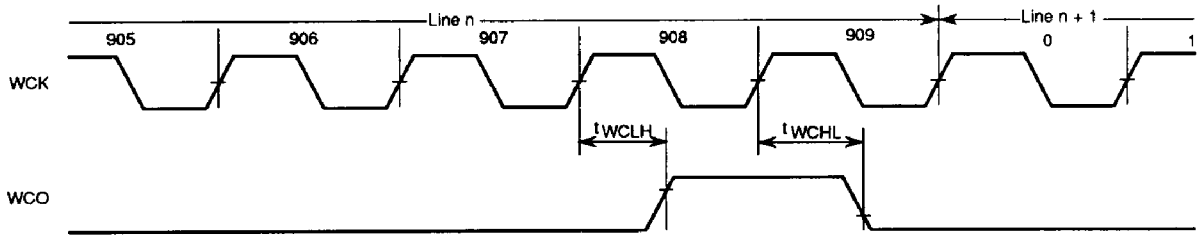
Timing Waveforms (cont)

Write Register Carry Out



Notes:

[1] MODE, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$ = V_{IH}

[2] LS_0 and LS_1 = V_{IH} or V_{IL}

[3] $\overline{OE}$, $\overline{W}$, WLH, RLH, WLJ, RLJ = don't care.

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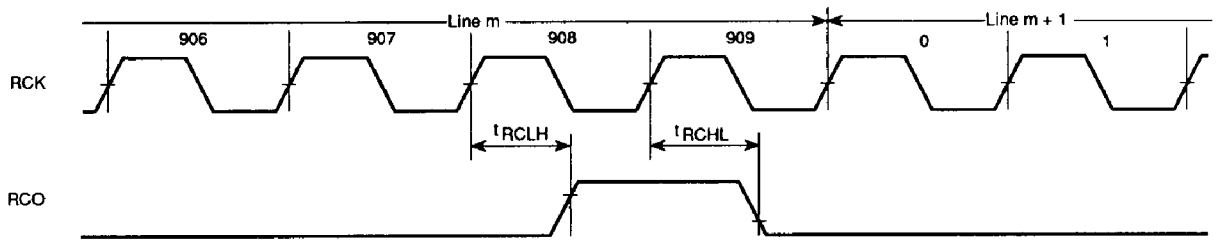
Read Register Carry Out



Notes:

[1] MODE, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$ = V_{IH}.

[2] LS_0 and LS_1 = V_{IH} or V_{IL}

[3] $\overline{OE}$, $\overline{W}$, WLH, RLH, WLJ, RLJ = don't care.

83VB-7102B

APPLICATION EXAMPLES

Delay Line

The synchronous mode may be used to create a full-field delay line with a fixed length (figures 6 and 7). Useful video applications include field interpolation, interframe noise reduction, and separation of luminance (Y) and chrominance (C) signals. In these applications, field buffer size is determined by the logic levels applied to pins LS_0 - LS_1 and BS_0 - BS_3. The former allows variation of the number of lines from 260 to 263, while the latter controls the actual line length at 896 to 910 bits for the last line. The actual delay between data being written into D_{IN} and read on D_{OUT} is controlled by the WCK clock period and the con figured size of the buffer.

Frame Synchronization or Time Base Correction

The μPD42270 has the capability of executing asyn chronous write and read cycles by independently clocking WCK and RCK, respectively. The feature is useful in applications requiring frame synchronization, time base correction or buffering, where WCK, RCK, $\overline{WCLR}$ and $\overline{RCLR}$ may all have variable time periods. In addition, the write carry out (WCO) and read carry out (RCO) options give a positive indication when the bit pointer reaches the end of the line.

Vertical or Horizontal Image Compression and Expansion

Vertical compression and expansion of the video image may be accomplished by means of the line jump or line hold functions. Compression occurs when WLJ or RLJ are used to jump over lines that are not to be displayed. Expansion occurs when the WLH or RLH line hold signals are used to display a line multiple times.

Horizontal compression and expansion can be achieved by modifying the cycle time of the WCK and RCK clocks, and by using the $\overline{WLRST}$ and $\overline{RLRST}$ line reset signals.

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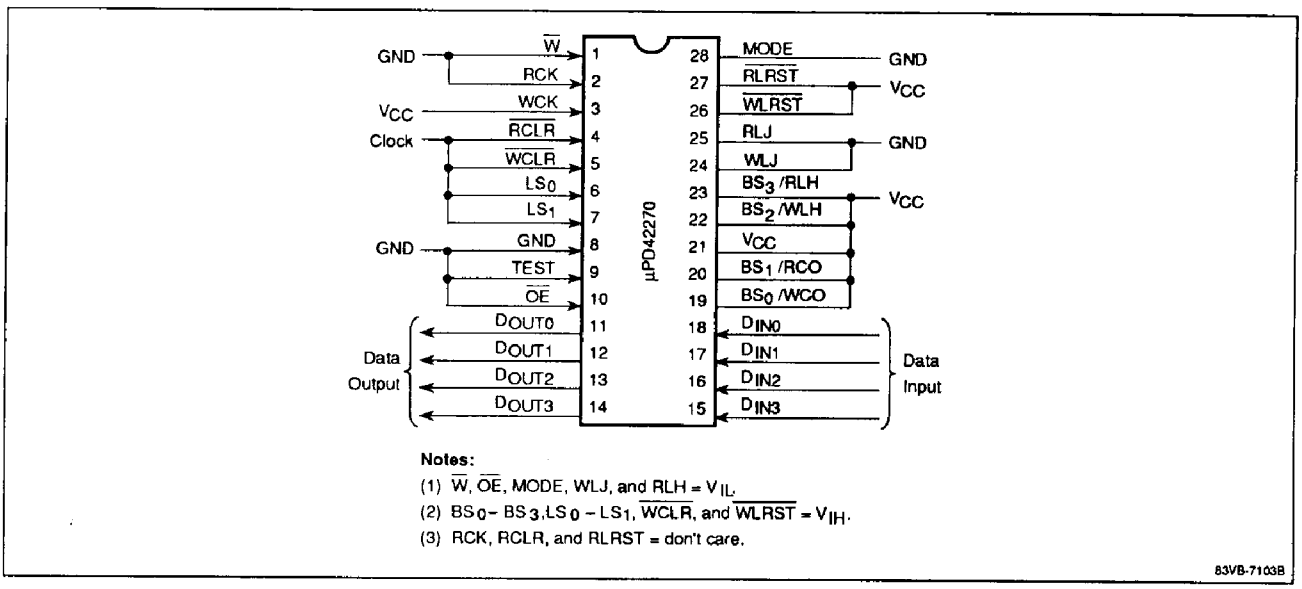
Figure 6. Example of Delay Line



Notes:

(1) $\overline{W}$, $\overline{OE}$, MODE, WLJ, and RLH = V_{IL}.

(2) BS_0 - BS_3, LS_0 - LS_1, $\overline{WCLR}$, and $\overline{WLRST}$ = V_{IH}.

(3) RCK, RCLR, and RLRST = don't care.

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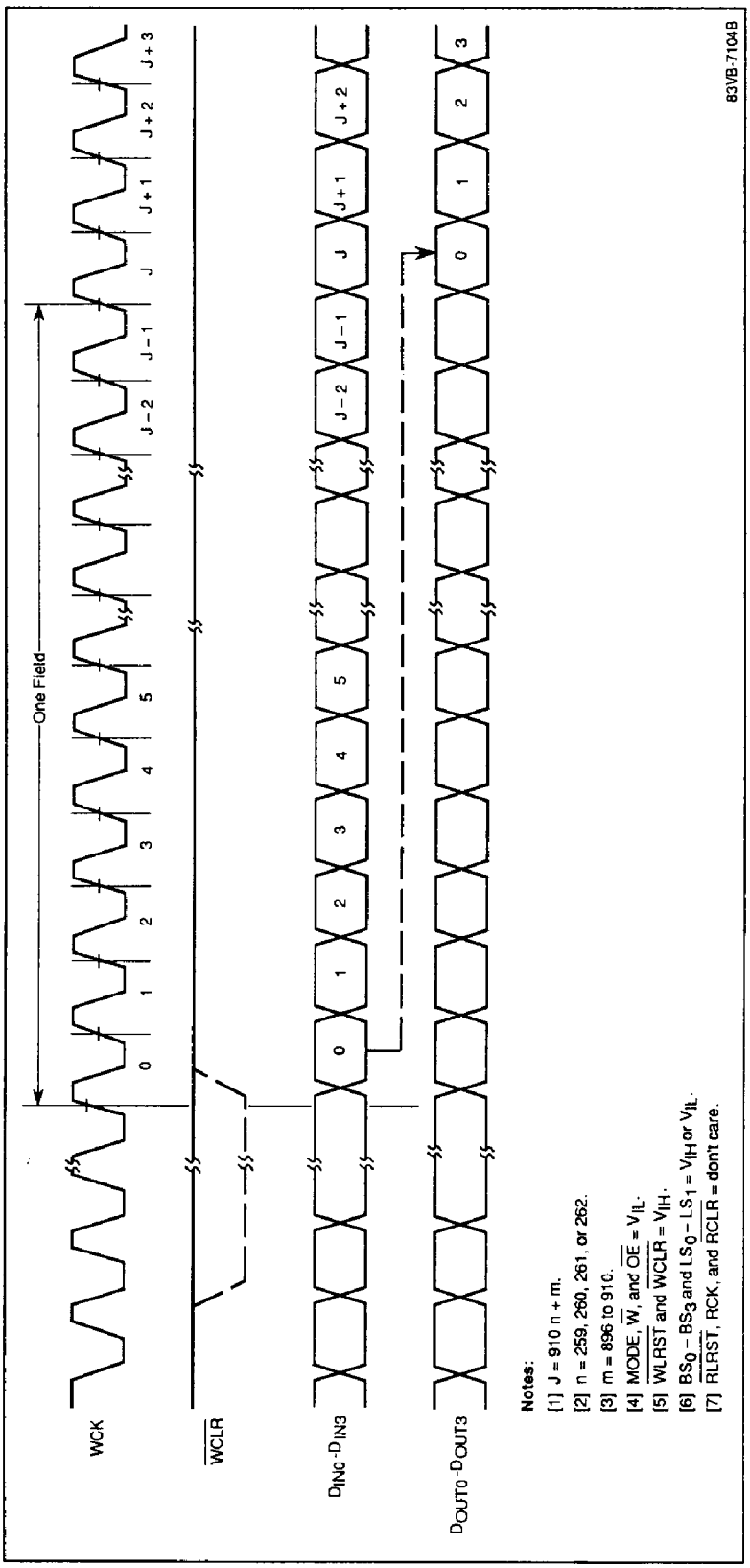


Figure 7. Delay Line Timing

Notes:

[1] J = 910 n + m.

[2] n = 259, 260, 261, or 262.

[3] m = 896 to 910.

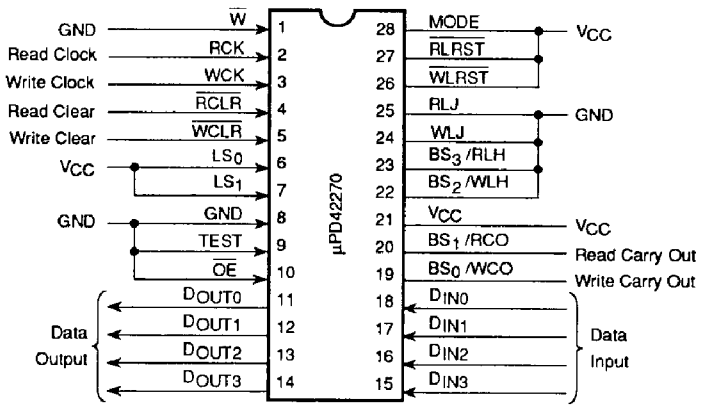
[4] MODE, $\overline{W}$, and $\overline{OE}$ = V_{IL}.

[5] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.

[6] $BS_0 - BS_3$ and $LS_0 - LS_1$ = V_{IH} or V_{IL}.

[7] $\overline{RLRST}$, RCK, and $\overline{RCLR}$ = don't care.

Figure 8. Example of Frame Synchronization/Time Base Correction



Notes:
(1) $\overline{W}$, $\overline{OE}$, WLJ, RLJ, WLH, and RLH = V_{IL}.
(2) LS_0 – LS_1, MODE, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.

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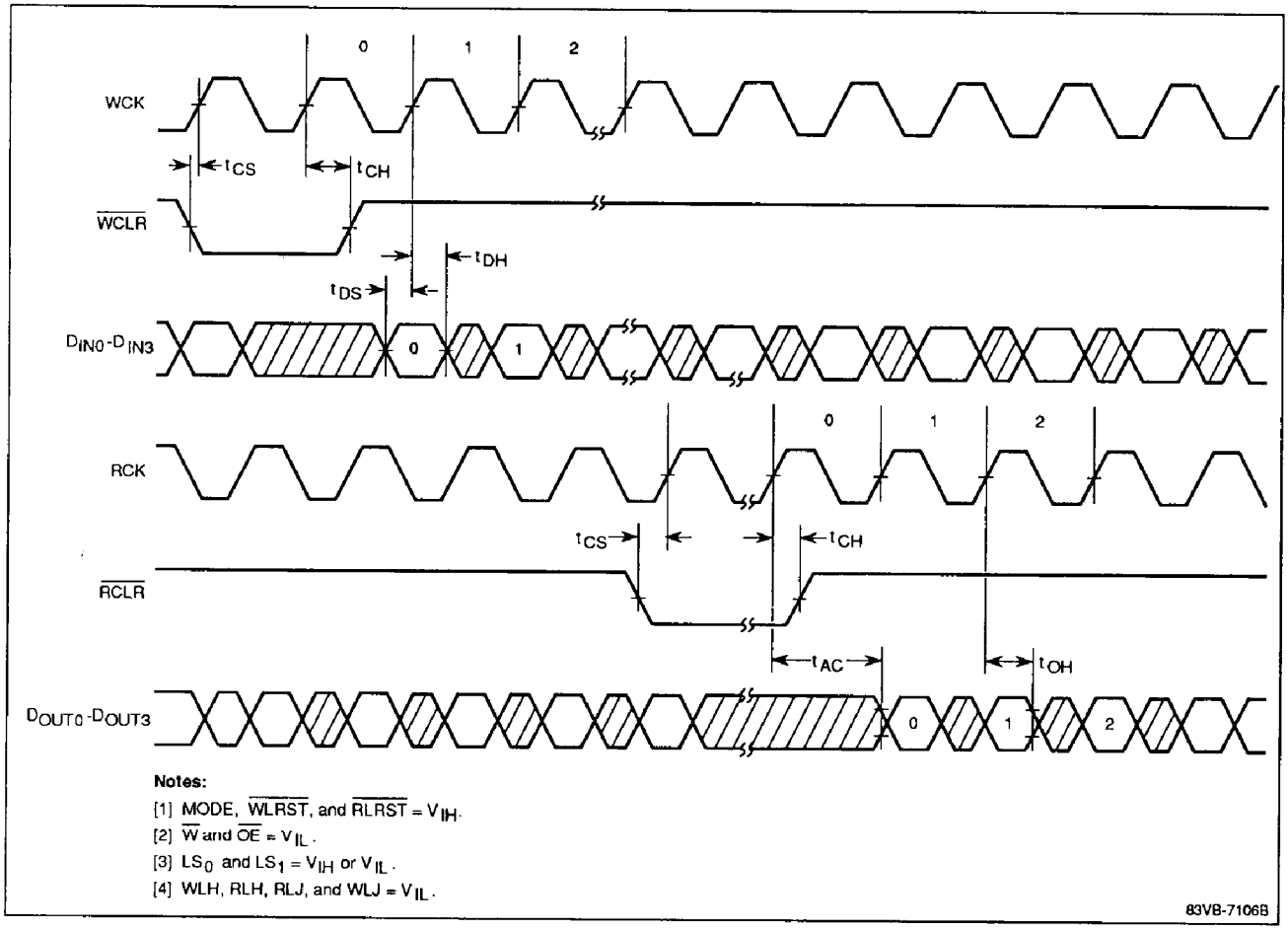
Figure 9. Asynchronous Read/Write Timing for Frame Synchronization or Time Base Correction



Notes:
[1] MODE, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.
[2] $\overline{W}$ and $\overline{OE}$ = V_{IL}.
[3] LS_0 and LS_1 = V_{IH} or V_{IL}.
[4] WLH, RLH, RLJ, and WLJ = V_{IL}.

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