



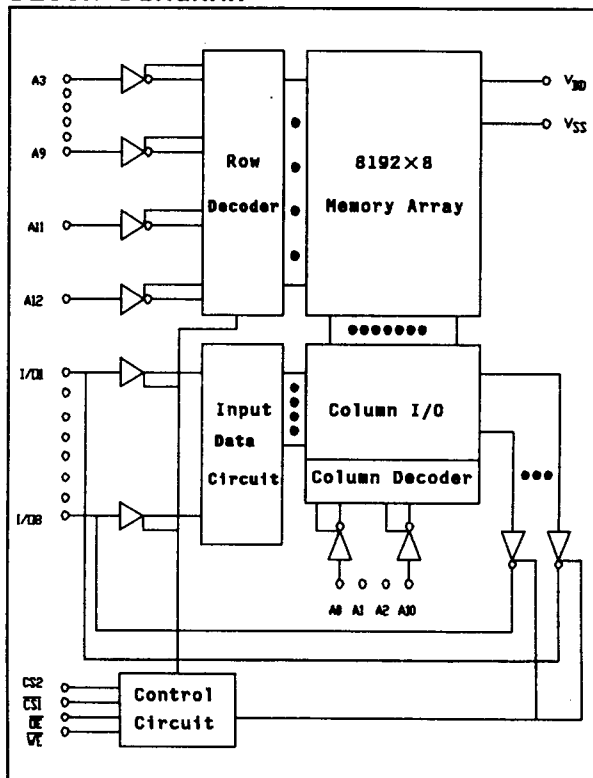
W2464A

8K X 8 HIGH SPEED CMOS STATIC RAM

FEATURES

- Low Power Consumption :
Active : 400mW (Typ.)
Standby : 25 μ W(Typ.)-- L-Version
- Fast Access Time : 20/25 ns (Max.)
- Single +5V Supply
- Fully Static Operation
- Direct TTL Compatible : All Inputs and Outputs
- Three State Outputs
- Capability of Battery Back Up Operation (L-Version)
- Data Retention Voltage : 2V (Min.) (L-Version)
- Available in 28 Pin SOJ, or Skinny DIP Packages

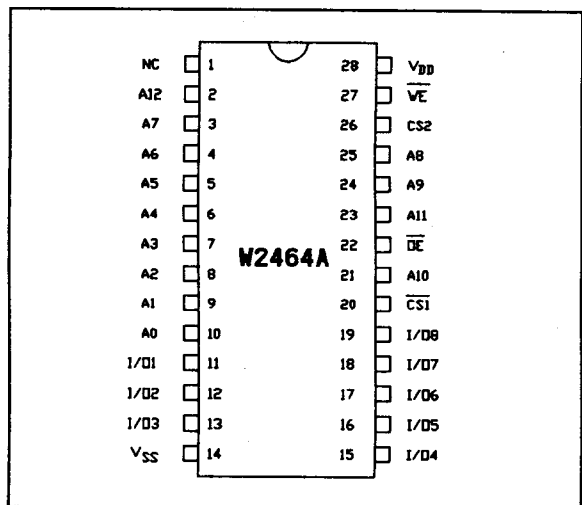
BLOCK DIAGRAM



DESCRIPTION

The W2464A is a Very High Speed, Low Power CMOS Static RAM Organized as 8192 x 8 Bits and Operates on a Single 5-Volt Supply. It is Manufactured Using WINBOND's High Performance CMOS Technology.

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
I/O1-I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select 1,2 Inputs
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection



DC CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Inputs/Outputs to V_{SS} Potential	-0.5 to $V_{DD}+0.5$	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-55 to +150	°C
Operating Temperature	0 to +70	°C

TRUTH TABLE

$\overline{CS1}$	CS2	\overline{OE}	\overline{WE}	Mode	I/O1 - I/O8	V_{DD} Current
H	X	X	X	Not Selected	High Z	I_{SB} , I_{SB1}
X	L	X	X	Not Selected	High Z	I_{SB} , I_{SB1}
L	H	H	H	Output Disable	High Z	I_{DD}
L	H	L	H	Read	Data Out	I_{DD}
L	H	X	L	Write	Data In	I_{DD}

OPERATING CHARACTERISTICS

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $70^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-	- 0.5	-	+ 0.8	V
Input High Voltage	V_{IH}	-	+ 2.2	-	$V_{DD} + 0.5$	V
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{DD}	-10	-	10	μA
Output Leakage Current	I_{LO}	$V_{I/O} = V_{SS}$ to V_{DD} $\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-10	-	10	μA
Output Low Voltage	V_{OL}	$I_{OL} = +8.0mA$	-	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS1}=V_{IL}$, $CS2=V_{IH}$, $I/O=0mA$ CYCLE=MIN, DUTY=100%	-	-	150	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$	-	-	30	mA
	I_{SB1}	$\overline{CS1} \geq V_{DD}-0.2V$ or $CS2 \leq 0.2V$	L	-	5	100
S			-	-	5000	μA

Note : Typical characteristics are at $V_{DD}=5V, T_a=25^\circ C$.

CAPACITANCE

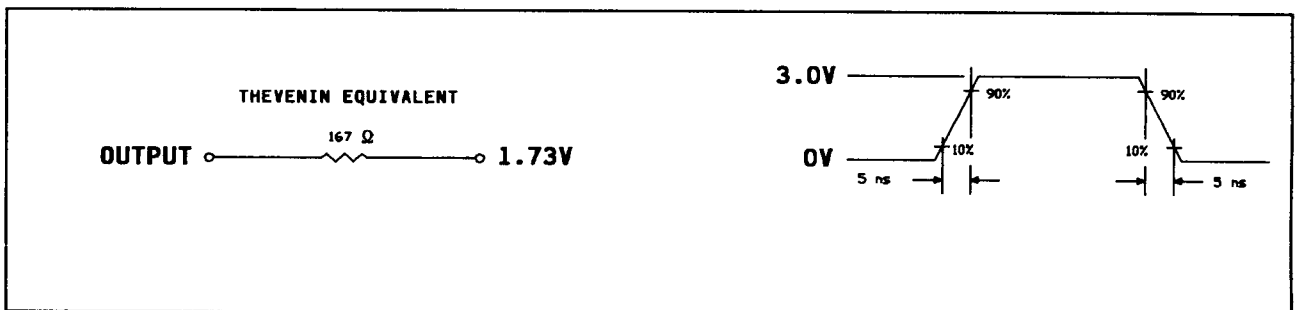
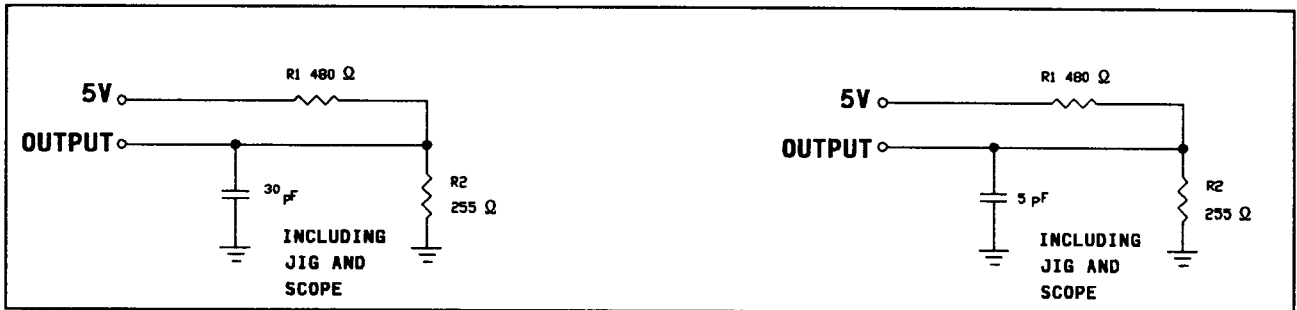
($V_{DD}=5V$, $T_a=25^\circ C$, $f=1MHz$)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	$V_{IN}=0V$	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT}=0V$	7	pF

Note : This parameter is sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	$C_L=30pF$, $I_{OH}/I_{OL}=-4mA/8mA$

AC TEST LOADS AND WAVEFORMS




AC CHARACTERISTICS

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $70^\circ C$)

(1) READ CYCLE

PARAMETER	SYMBOL	W2464A-20		W2464A-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	20	-	25	-	ns
Address Access Time	T_{AA}	-	20	-	25	ns
Chip Select Access Time	$\overline{CS1}$ T_{ACS1}	-	20	-	25	ns
	$CS2$ T_{ACS2}	-	20	-	25	ns
Output Enable to Output Valid	T_{AOE}	-	8	-	10	ns
Chip Selection to Output in Low Z	$\overline{CS1}$ T_{CLZ1}^*	3	-	3	-	ns
	$CS2$ T_{CLZ2}^*	3	-	3	-	ns
Output Enable to Output in Low Z	T_{OLZ}^*	0	-	0	-	ns
Chip Deselection to Output in High Z	$\overline{CS1}$ T_{CHZ1}^*	-	10	-	12	ns
	$CS2$ T_{CHZ2}^*	-	10	-	12	ns
Output Disable to Output in High Z	T_{OHZ}^*	-	10	-	12	ns
Output Hold from Address Change	T_{OH}	3	-	3	-	ns

Note: * This parameter is sampled but not 100% tested.

(2) WRITE CYCLE

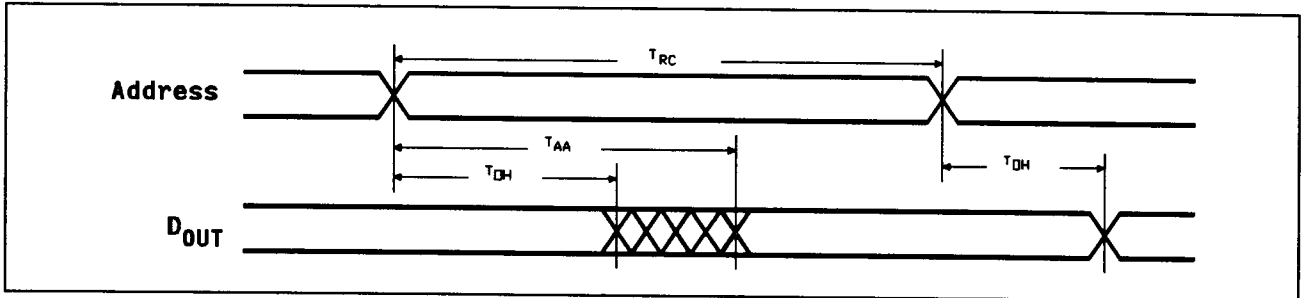
PARAMETER	SYMBOL	W2464A-20		W2464A-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	T_{WC}	20	-	25	-	ns
Chip Selection to End of Write	T_{CW}	17	-	22	-	ns
Address Valid to End of Write	T_{AW}	15	-	20	-	ns
Address Setup Time	T_{AS}	0	-	0	-	ns
Write Pulse Width	T_{WP}	12	-	15	-	ns
Write Recovery Time	$\overline{CS1}, \overline{WE}$ T_{WR1}	0	-	0	-	ns
	$CS2$ T_{WR2}	0	-	0	-	ns
Data Valid to End of Write	T_{DW}	10	-	12	-	ns
Data Hold from End of Write	T_{DH}	0	-	0	-	ns
Write to Output in High Z	T_{WHZ}^*	-	0	-	12	ns
Output Disable to Output in High Z	T_{OHZ}^*	-	0	-	12	ns
Output Active from End of Write	T_{OW}	0	-	0	-	ns

Note: * This parameter is sampled but not 100% tested.

TIMING WAVEFORMS

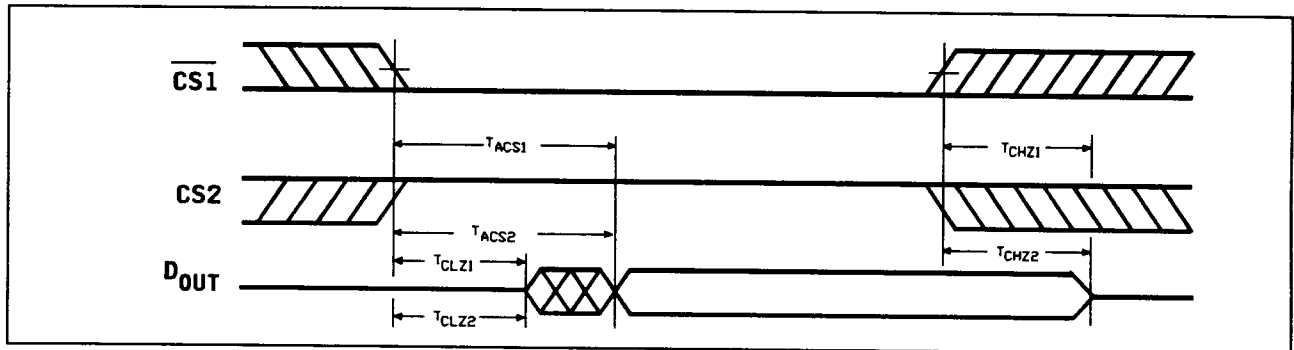
READ CYCLE 1

(Address Controlled)



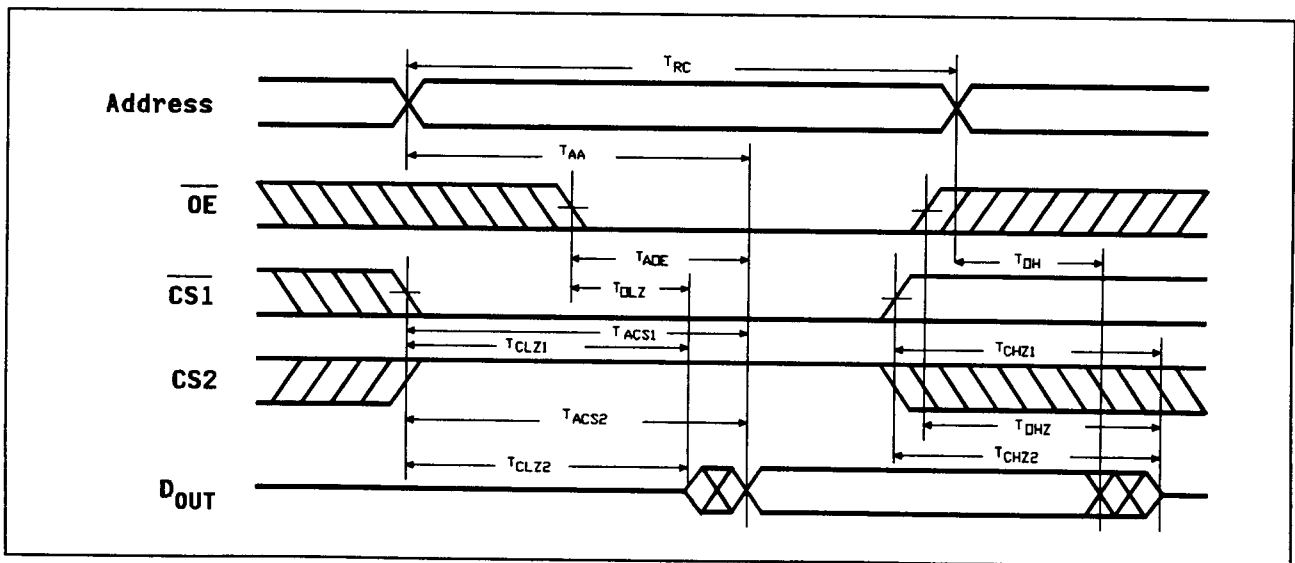
READ CYCLE 2

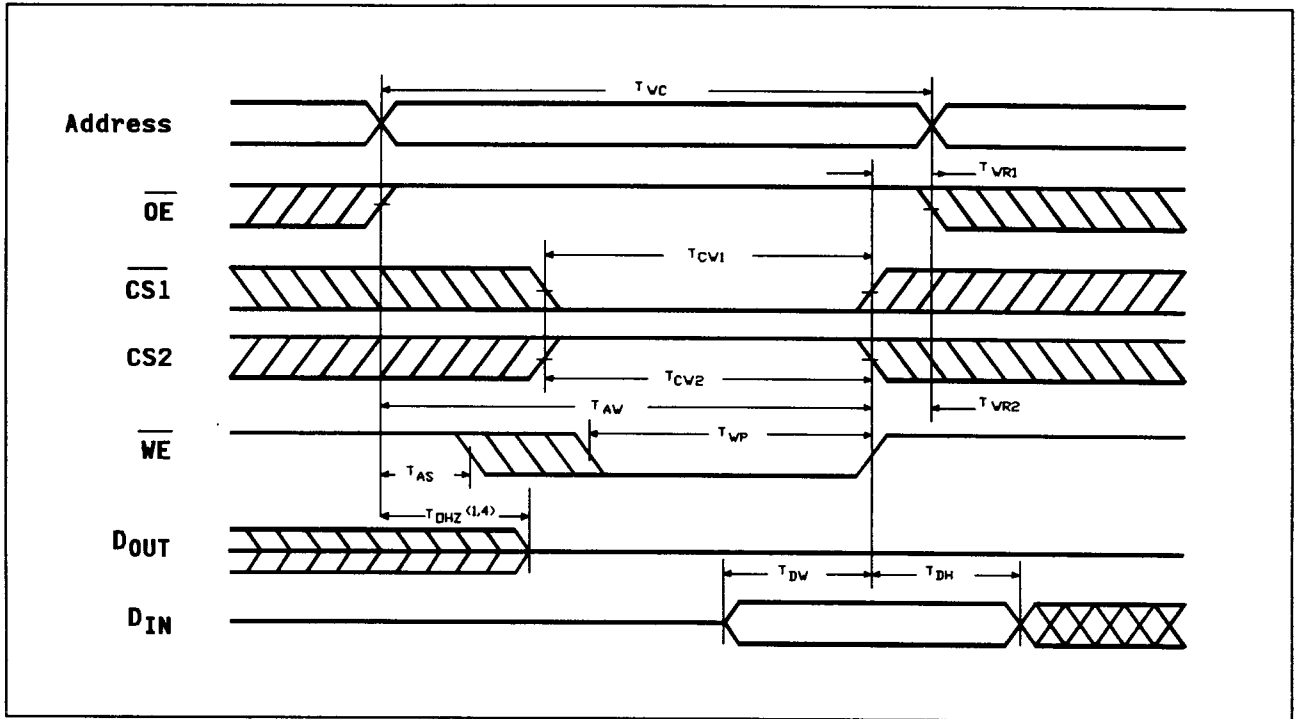
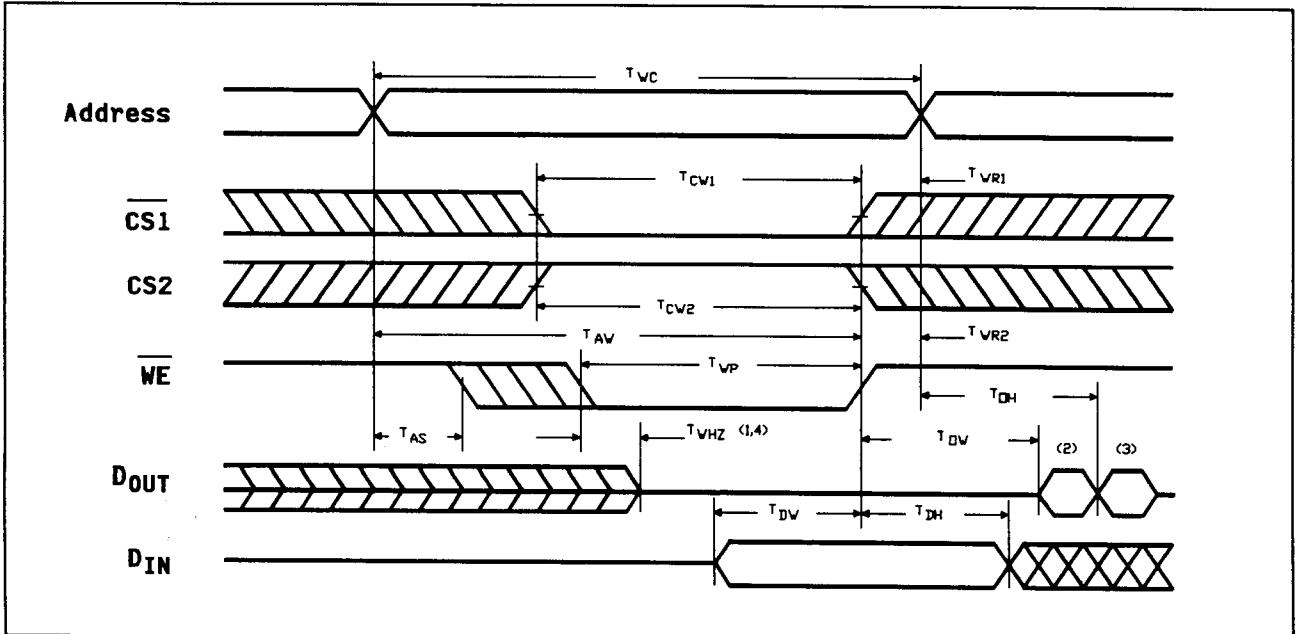
(Chip Select Controlled)



READ CYCLE 3

(Output Enable Controlled)



WRITE CYCLE 1
 (\overline{OE} Clock)

WRITE CYCLE 2
 ($\overline{OE} = V_{IL}$ Fixed)


Notes:

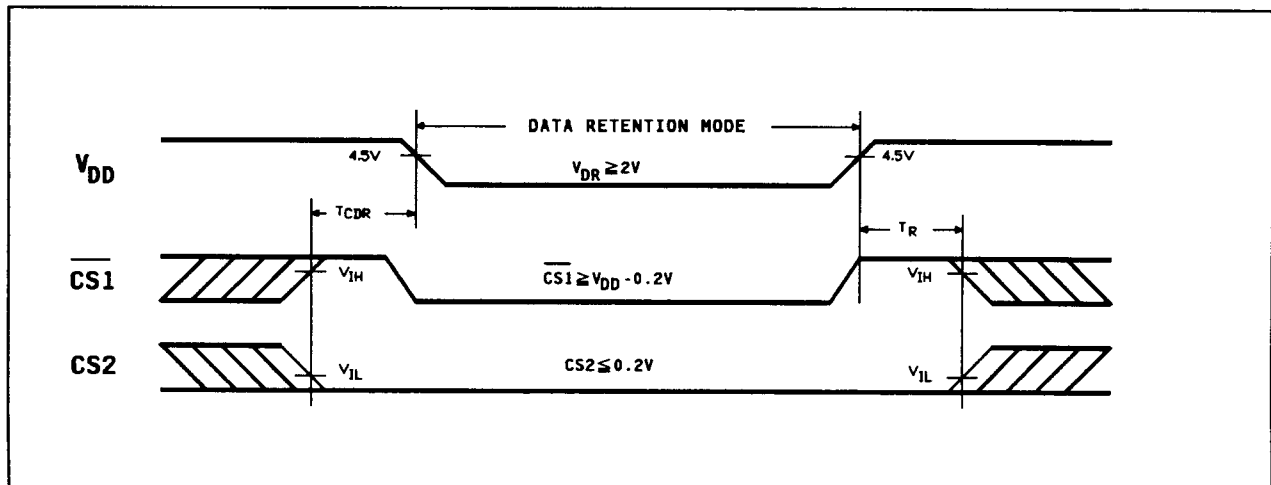
1. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
2. D_{OUT} is the same phase of write data of this write cycle.
3. D_{OUT} is the read data of next address.
4. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L=5\text{pF}$. This parameter is guaranteed but not 100% tested.

DATA RETENTION CHARACTERISTICS

(Ta=0 to 70°C, Guaranteed Only for L-Version)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{DD} - 0.2\text{V}$, or $CS2 \leq 0.2\text{V}$	2.0	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS1} \geq V_{DD} - 0.2\text{V}$, or $CS2 \leq 0.2\text{V}$ $V_{DD}=3\text{V}$	-	2	100	μA
Chip Deselect to Data Retention Time	T_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	T_R		T_{RC}^*	-	-	ns

 Note: * T_{RC} = Read Cycle Time

DATA RETENTION WAVEFORM




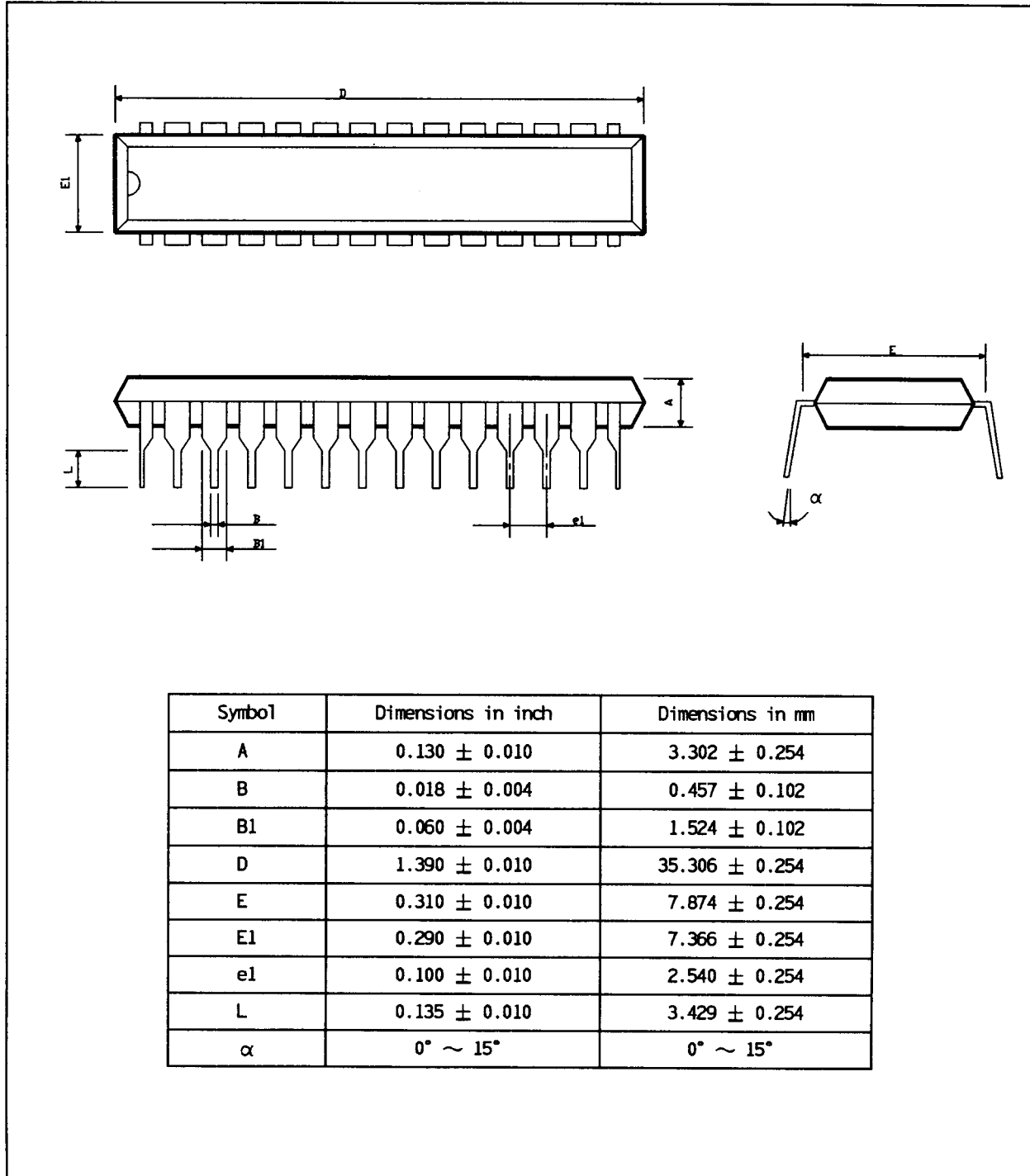
W2464A

ORDERING INFORMATION

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package	Remark
W2464AK-20	20	150	5	300mil Skinny	
W2464AK-20L	20	150	0.1	300mil Skinny	Low Power
W2464AK-25	25	150	4	300mil Skinny	
W2464AK-25L	25	150	0.1	300mil Skinny	Low Power
W2464AJ-20	20	150	5	300mil SOJ	
W2464AJ-20L	20	150	0.1	300mil SOJ	Low Power
W2464AJ-25	25	150	4	300mil SOJ	
W2464AJ-25L	25	150	0.1	300mil SOJ	Low Power

Notes:

1. Winbond Electronics Corp. reserves the right to make changes to its products without prior notice, in order to improve design and performance.
2. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such application.

28 LEAD P-DIP SKINNY




CORPORATE HEADQUARTERS:

No. 2, R&D Rd. VI,
Science-Based Industrial Park,
Hsin chu, Taiwan, R.O.C.
TEL: (035)770066
FAX: 886-35-774527

SALES OFFICE:

11 Fl. No. 673, Min Sheng E. Rd.,
Taipei, Taiwan, R.O.C.
TEL: (02)7190505
TLX: 16485 WINTPE
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.

Room 305, 3/F, 17 Wang Hai Road
Shun Fat Industrial Bldg. Kowloon Bay
Kowloon, Hong Kong
TEL: 7516023-7
FAX: 7552064

**Winbond Electronics (North
America) Corp.**

3350, Scott Blvd., Bldg. #20
Santa Clara, CA 95054 U.S.A.
TEL: (408) 982-0381
FAX: (408) 982-9231

Winbond Europe

Leuvensesteenweg 613
B-1930 Zaventem, Belgium
TEL: (32) (2) 7592910
FAX: (32) (2) 7592964
TLX: 20370 BC.Zav.B.

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