

N-Channel JFET Monolithic Dual



U443 / U444

FEATURES

- High Gain $g_{fs} > 6 \text{ mS typical}$
- Low Leakage $I_g < 1 \text{ pA typical}$
- Low Noise

APPLICATIONS

- Differential Wideband Amplifiers
- VHF/UHF Amplifiers
- Test and Measurement
- Multi-Chip/Hybrids

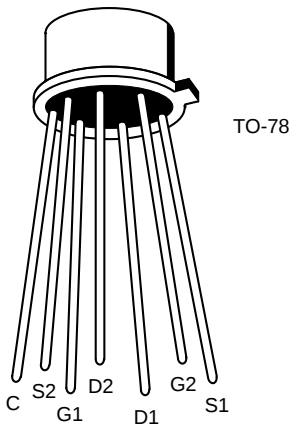
DESCRIPTION

The U443 Series is an N-Channel Monolithic Dual JFET designed for high speed amplifier circuits. Featuring high gain ($> 6 \text{ mS typical}$), low leakage ($< 1 \text{ pA typical}$) and low noise this device is an excellent choice for high performance test and measurement, wideband amplifiers and VHF/UHF circuits.

ORDERING INFORMATION

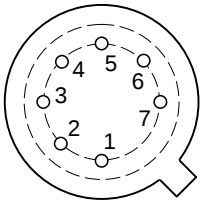
Part	Package	Temperature Range
U443-4	Hermetic M0-002AG (TO-78)	-55°C to $+150^{\circ}\text{C}$
XU443-4	Sorted Chips in Carriers	-55°C to $+150^{\circ}\text{C}$

PIN CONFIGURATION



CJ1

- 1 SOURCE 1
- 2 DRAIN 1
- 3 GATE 1
- 4 CASE/BODY
- 5 SOURCE 2
- 6 DRAIN 2
- 7 GATE 2



BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter/Test Condition	Symbol	Limit	Unit
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	V
Gate-Gate Voltage	V_{GG}	± 50	V
Forward Gate Current	I_G	50	mA
Power Dissipation (per side)	P_D	367	mW
(total)		500	mW
Power Derating (per side)		3	mW/ $^{\circ}\text{C}$
(total)		4	mW/ $^{\circ}\text{C}$
Operating Junction Temperature	T_J	-55 to 150	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-65 to 200	$^{\circ}\text{C}$
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

SYMBOL	CHARACTERISTCS	TYP ¹	U443		U444		UNIT	TEST CONDITIONS		
			MIN	MAX	MIN	MAX				
STATIC										
V _{(BR)GSS}	Gate-Source Breakdown Voltage	-35	-25		-25		V	I _G = -1μA, V _{DS} = 0V		
V _{GS(OFF)}	Gate-Source Cut off Voltage	-3.5	-1	-6	-1	-6		V _{DS} = 10V, I _D = 1nA		
I _{DSS}	Saturation Drain Current ²	15	6	30	6	30	mA	V _{DS} = 10V, V _{GS} = 0V		
I _{GSS}	Gate Reverse Current	-1		-500		-500	pA	V _{GS} = -15V, V _{DS} = 0V		
		-2					nA	T _A = 150°C		
I _G	Gate Operating Current	-1		-500		-500	pA	V _{DG} = 10V, I _D = 5mA		
		-0.3					nA	T _A = 125°C		
V _{GS(F)}	Gate-Source Forward Voltage	0.7					V	I _G = 1mA, V _{DS} = 0V		
DYNAMIC										
g _{fs}	Common-Source Forward Transconductance	6	4.5	9	4.5	9	mS	V _{DG} = 10V, I _D = 5mA f = 1kHz		
g _{os}	Common-Source Output Conductance	70		200		200	μS			
C _{iss}	Common-Source Input Capacitance	3					pF	V _{DG} = 10V, I _D = 5mA f = 1MHz		
C _{rss}	Common-Source Reverse Transfer Capacitance	1								
$\bar{e}_n$	Equivalent Input Noise Voltage	4					nV/√Hz	V _{DG} = 10V, I _D = 5mA f = 10kHz		
MATCHING										
V _{GS1} -V _{GS2}	Differential Gate-Source Voltage	6		10		20	mV	V _{DG} = 10V, I _D = 5mA		
$\Delta \mid \frac{V_{GS1}-V_{GS2}}{\Delta T}$	Gate-Source Voltage Differential Change with Temperature	20					μV/ °C	T = -55 to 25°C	V _{DG} =10V, I _D = 5mA	
		20						T = 25 to 125°C		
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.97						V _{DS} = 10V, V _{GS} = 0V		
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97						V _{DG} = 10V, I _D = 5mA f= 1 kHz		
CMRR	Common Mode Rejection Ratio	85					dB	V _{DD} = 5 to 10V, I _D = 5mA		

NOTES: 1. For design aid only, not subject to production testing.
2. Pulse test; $PW = 300\mu\text{s}$, duty cycle $\leq 3\%$.