



***Z08030/8530***

***Serial Communications  
Controller***

**Customer Procurement Specification**

PS011301-0601



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

**ZiLOG Worldwide Headquarters**

910 E. Hamilton Avenue  
Campbell, CA 95008  
Telephone: 408.558.8500  
Fax: 408.558.8300  
[www.ZiLOG.com](http://www.ZiLOG.com)

Windows is a registered trademark of Microsoft Corporation.

**Document Disclaimer**

©2001 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Devices sold by ZiLOG, Inc. are covered by warranty and limitation of liability provisions appearing in the ZiLOG, Inc. Terms and Conditions of Sale. ZiLOG, Inc. makes no warranty of merchantability or fitness for any purpose Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.

**Zilog**200030/2530 Customer  
Procurement Spec (CPS)

| DC Characteristic | Symbol   | Parameter               | Min               | Max              | Unit    | Condition                     |
|-------------------|----------|-------------------------|-------------------|------------------|---------|-------------------------------|
|                   | $V_{IH}$ | Input High Voltage      | 2.0 <sup>a</sup>  | $V_{CC} + 0.3^c$ | V       |                               |
|                   | $V_{IL}$ | Input Low Voltage       | -0.3 <sup>c</sup> | 0.8 <sup>a</sup> | V       |                               |
|                   | $V_{OH}$ | Output High Voltage     | 2.4 <sup>a</sup>  |                  | V       | $I_{OH} = -250 \mu A$         |
|                   | $V_{OL}$ | Output Low Voltage      |                   | 0.4 <sup>a</sup> | V       | $I_{OL} = +2.0 \text{ mA}$    |
|                   | $I_{IL}$ | Input Leakage           |                   | $\leq 10.0^a$    | $\mu A$ | $0.4 \leq V_{IH} \leq +2.4V$  |
|                   | $I_{OL}$ | Output Leakage          |                   | $\leq 10.0^a$    | $\mu A$ | $0.4 \leq V_{OUT} \leq +2.4V$ |
|                   | $I_{CC}$ | $V_{CC}$ Supply Current |                   | 250              | $\mu A$ |                               |

 $V_{CC} = 5V \pm 5\%$  unless otherwise specified, over specified temperature range.

- a Tested  
b Guaranteed by Design  
c Guaranteed by Characterization

**Absolute Maximum Ratings**

Voltages on all pins with respect to GND..... -0.3V to +7.0V  
Operating Ambient Temperature..... See Ordering Information  
Storage Temperature..... -65°C to +150°C

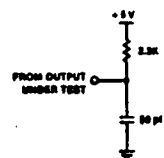
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Standard Test Conditions**

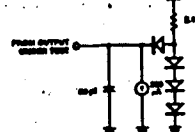
The DC characteristics and capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.

Standard conditions are as follows:

- $+4.75V \leq V_{CC} \leq +5.25V$
  - $GND = 0V$
  - $T_A$  as specified in Ordering Information
- All ac parameters assume a load capacitance of 50 pF max.



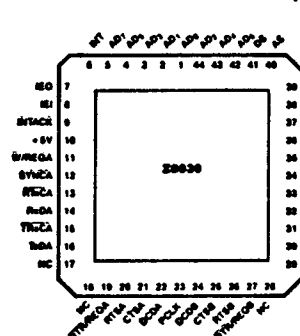
Open-Drain Test Load



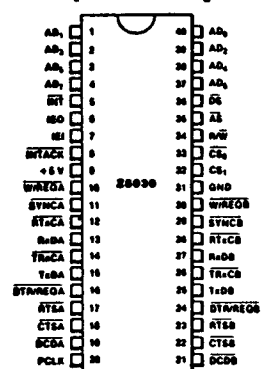
Standard Test Load

Z8000 is a registered trademark of Zilog, Inc. © 1989 by Zilog, Inc. All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without the prior written permission of Zilog. The information contained herein is subject to change without notice. Zilog assumes no responsibility for the use of any circuitry other than circuitry embodied in a Zilog product. No other circuit patent licenses are implied. All specifications (parameters) are subject to change without notice. The applicable Zilog test documentation will specify which parameters are tested. Zilog, Inc. 210 Hacienda Ave., Campbell, CA 95008-6600 Telephone (408) 376-8000 FAX 916-338-7621

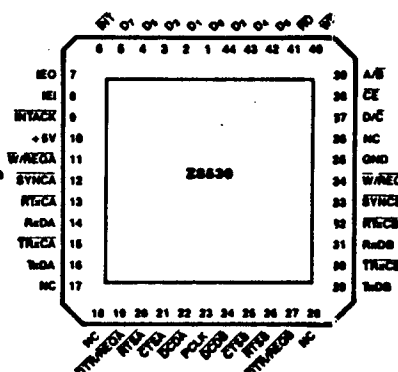
00-2837-02



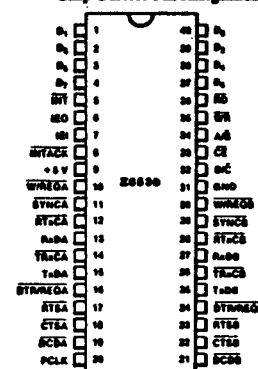
Chip Carrier Pin Assignments, Z8000



DIP Pin Assignments, Z8000



Chip Carrier Pin Assignments, Z8530



DIP Pin Assignments, Z8530

**General Description**

The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with conventional non-multiplexed buses and the Zilog Z-BUS.® The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, Digital Phase Locked Loops, and crystal oscillators that dramatically reduce the need for external logic.

The SCC handles asynchronous formats, Synchronous byte-oriented protocols such as IBM Bisync, and Synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

The device can generate and check CRC codes in any Synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The daisy-chain interrupt hierarchy is also supported—as is standard for Zilog peripheral components.

Maximum data rate:  
1/4 PCLOCK using external phase lock loop.

Minimum data rate:  
50 baud for any PCLOCK period.

# Z8030 AC CHARACTERISTICS

| Number | Symbol                | Parameter                          | 4 MHz                          |                  | 6 MHz                          |                  | 8 MHz                          |                  | Notes <sup>†</sup> |
|--------|-----------------------|------------------------------------|--------------------------------|------------------|--------------------------------|------------------|--------------------------------|------------------|--------------------|
|        |                       |                                    | Min                            | Max              | Min                            | Max              | Min                            | Max              |                    |
| 1      | T <sub>WAS</sub>      | AS Low Width                       | 70 <sup>a</sup>                |                  | 50 <sup>a</sup>                |                  | 35 <sup>a</sup>                |                  |                    |
| 2      | T <sub>DS(AS)</sub>   | DS ↑ to AS ↓ Delay                 | 50 <sup>c</sup>                |                  | 25 <sup>c</sup>                |                  | 15 <sup>c</sup>                |                  |                    |
| 3      | T <sub>CSO(AS)</sub>  | CS <sub>0</sub> to AS ↑ Setup Time | 0 <sup>a</sup>                 |                  | 0 <sup>a</sup>                 |                  | 0 <sup>a</sup>                 |                  | 1                  |
| 4      | T <sub>HCSO(AS)</sub> | CS <sub>0</sub> to AS ↑ Hold Time  | 60 <sup>a</sup>                |                  | 40 <sup>a</sup>                |                  | 30 <sup>a</sup>                |                  | 1                  |
| 5      | T <sub>CS1(DS)</sub>  | CS <sub>1</sub> to DS ↓ Setup Time | 100 <sup>a</sup>               |                  | 80 <sup>a</sup>                |                  | 65 <sup>a</sup>                |                  | 1                  |
| 6      | T <sub>HCS1(DS)</sub> | CS <sub>1</sub> to DS ↑ Hold Time  | 55 <sup>c</sup>                |                  | 40 <sup>c</sup>                |                  | 30 <sup>c</sup>                |                  | 1                  |
| 7      | T <sub>AI(AS)</sub>   | INTACK to AS ↑ Setup Time          | 10 <sup>c</sup>                |                  | 10 <sup>c</sup>                |                  | 10 <sup>c</sup>                |                  |                    |
| 8      | T <sub>HA(AS)</sub>   | INTACK to AS ↑ Hold Time           | 250 <sup>a</sup>               |                  | 200 <sup>a</sup>               |                  | 150 <sup>a</sup>               |                  |                    |
| 9      | T <sub>RWR(DS)</sub>  | R/W (Read) to DS ↓ Setup Time      | 100 <sup>a</sup>               |                  | 80 <sup>a</sup>                |                  | 65 <sup>a</sup>                |                  |                    |
| 10     | T <sub>HRW(DS)</sub>  | R/W to DS ↑ Hold Time              | 55 <sup>a</sup>                |                  | 40 <sup>a</sup>                |                  | 35 <sup>a</sup>                |                  |                    |
| 11     | T <sub>RWW(DS)</sub>  | R/W (Write) to DS ↓ Setup Time     | 0 <sup>c</sup>                 |                  | 0 <sup>c</sup>                 |                  | 0 <sup>c</sup>                 |                  |                    |
| 12     | T <sub>AS(DS)</sub>   | AS ↑ to DS ↓ Delay                 | 60 <sup>c</sup>                |                  | 40 <sup>c</sup>                |                  | 30 <sup>c</sup>                |                  |                    |
| 13     | T <sub>WDSI</sub>     | DS Low Width                       | 240 <sup>a</sup>               |                  | 200 <sup>a</sup>               |                  | 150 <sup>a</sup>               |                  |                    |
| 14     | T <sub>IC</sub>       | Valid Access Recovery Time         | 4T <sub>CPC</sub> <sup>a</sup> |                  | 4T <sub>CPC</sub> <sup>a</sup> |                  | 4T <sub>CPC</sub> <sup>a</sup> |                  | 2                  |
| 15     | T <sub>SA(AS)</sub>   | Address to AS ↑ Setup Time         | 30 <sup>a</sup>                |                  | 10 <sup>a</sup>                |                  | 10 <sup>a</sup>                |                  | 1                  |
| 16     | T <sub>HA(AS)</sub>   | Address to AS ↑ Hold Time          | 50 <sup>a</sup>                |                  | 30 <sup>a</sup>                |                  | 25 <sup>a</sup>                |                  | 1                  |
| 17     | T <sub>SDW(DS)</sub>  | Write Data to DS ↓ Setup Time      | 30 <sup>a</sup>                |                  | 20 <sup>a</sup>                |                  | 15 <sup>a</sup>                |                  |                    |
| 18     | T <sub>HDW(DS)</sub>  | Write Data to DS ↑ Hold Time       | 30 <sup>a</sup>                |                  | 20 <sup>a</sup>                |                  | 20 <sup>a</sup>                |                  |                    |
| 19     | T <sub>DS(DA)</sub>   | DS ↓ to Data Active Delay          | 0 <sup>c</sup>                 |                  | 0 <sup>c</sup>                 |                  | 0 <sup>c</sup>                 |                  |                    |
| 20     | T <sub>DSn(DR)</sub>  | DS ↑ to Read Data Not Valid Delay  | 0 <sup>a</sup>                 |                  | 0 <sup>a</sup>                 |                  | 0 <sup>a</sup>                 |                  |                    |
| 21     | T <sub>DSn(DR)</sub>  | DS ↓ to Read Data Valid Delay      |                                | 250 <sup>a</sup> |                                | 180 <sup>a</sup> |                                | 140 <sup>a</sup> |                    |
| 22     | T <sub>AS(DR)</sub>   | AS ↑ to Read Data Valid Delay      |                                | 520 <sup>a</sup> |                                | 300 <sup>a</sup> |                                | 250 <sup>a</sup> |                    |

## NOTES:

- Parameter does not apply to Interrupt Acknowledge transactions.
- Parameter applies only between transactions involving the SCC.
- Timings are preliminary and subject to change.
- Units in nanoseconds (ns).

<sup>a</sup> Tested

<sup>b</sup> Guaranteed by Design

<sup>c</sup> Guaranteed by Characterization

# Z8030 AC CHARACTERISTICS (Continued)

| Number | Symbol                | Parameter                                       | 4 MHz                                                |                   | 6 MHz                                                |                   | 8 MHz                                                |     | Notes <sup>†</sup> |
|--------|-----------------------|-------------------------------------------------|------------------------------------------------------|-------------------|------------------------------------------------------|-------------------|------------------------------------------------------|-----|--------------------|
|        |                       |                                                 | Min                                                  | Max               | Min                                                  | Max               | Min                                                  | Max |                    |
| 23     | T <sub>DS(DR)</sub>   | DS ↑ to Read Data Float Delay                   | 70 <sup>a</sup>                                      |                   | 40 <sup>a</sup>                                      |                   | 40 <sup>c</sup>                                      |     | 3                  |
| 24     | T <sub>ADR</sub>      | Address Required Valid to Read Data Valid Delay | 570 <sup>a</sup>                                     |                   | 510 <sup>a</sup>                                     |                   | 380 <sup>a</sup>                                     |     |                    |
| 25     | T <sub>DS(W)</sub>    | DS ↓ to Wait Valid Delay                        | 240 <sup>a</sup>                                     |                   | 200 <sup>a</sup>                                     |                   | 170 <sup>a</sup>                                     |     | 4                  |
| 26     | T <sub>DS(FREQ)</sub> | DS ↓ to WR/EO Not Valid Delay                   | 240 <sup>a</sup>                                     |                   | 200 <sup>a</sup>                                     |                   | 170 <sup>a</sup>                                     |     |                    |
| 27     | T <sub>DS(FREQ)</sub> | DS ↓ to DTR/EO Not Valid Delay                  | 5T <sub>CPC</sub> <sup>a</sup><br>+ 300 <sup>a</sup> |                   | 5T <sub>CPC</sub> <sup>a</sup><br>+ 250 <sup>a</sup> |                   | 5T <sub>CPC</sub> <sup>a</sup><br>+ 200 <sup>a</sup> |     |                    |
| 28     | T <sub>AS(NT)</sub>   | AS ↑ to INT Valid Delay                         | 600 <sup>a</sup>                                     |                   | 500 <sup>a</sup>                                     |                   | 500 <sup>a</sup>                                     |     | 4                  |
| 29     | T <sub>AS(DSA)</sub>  | AS ↑ to DS ↓ (Acknowledge) Delay                | 250 <sup>a</sup>                                     |                   | 250 <sup>a</sup>                                     |                   | 250 <sup>a</sup>                                     |     | 5                  |
| 30     | T <sub>WDA</sub>      | DS (Acknowledge) Low Width                      | 280 <sup>a</sup>                                     |                   | 200 <sup>a</sup>                                     |                   | 160 <sup>a</sup>                                     |     |                    |
| 31     | T <sub>DS(DR)</sub>   | DS ↓ (Acknowledge) to Read Data Valid Delay     | 260 <sup>a</sup>                                     |                   | 180 <sup>a</sup>                                     |                   | 140 <sup>a</sup>                                     |     |                    |
| 32     | T <sub>IE(DSA)</sub>  | IE ↑ to DS ↓ (Acknowledge) Setup Time           | 120 <sup>a</sup>                                     |                   | 100 <sup>a</sup>                                     |                   | 80 <sup>a</sup>                                      |     |                    |
| 33     | T <sub>IE(DSA)</sub>  | IE ↑ to DS ↓ (Acknowledge) Hold Time            | 0 <sup>c</sup>                                       |                   | 0 <sup>c</sup>                                       |                   | 0 <sup>c</sup>                                       |     |                    |
| 34     | T <sub>IE(EO)</sub>   | IE ↑ to EIO Delay                               | 120 <sup>a</sup>                                     |                   | 100 <sup>a</sup>                                     |                   | 80 <sup>a</sup>                                      |     |                    |
| 35     | T <sub>AS(EO)</sub>   | AS ↑ to EIO Delay                               | 280 <sup>a</sup>                                     |                   | 260 <sup>a</sup>                                     |                   | 200 <sup>a</sup>                                     |     | 6                  |
| 36     | T <sub>DS(NT)</sub>   | DS ↓ (Acknowledge) to INT Inactive Delay        | 600 <sup>a</sup>                                     |                   | 500 <sup>a</sup>                                     |                   | 460 <sup>a</sup>                                     |     | 4                  |
| 37     | T <sub>DS(ASQ)</sub>  | DS ↑ to AS ↓ Delay for No Reset                 | 30 <sup>a</sup>                                      |                   | 15 <sup>a</sup>                                      |                   | 15 <sup>a</sup>                                      |     |                    |
| 38     | T <sub>ASQ(DS)</sub>  | AS ↑ to DS ↓ Delay for No Reset                 | 30 <sup>a</sup>                                      |                   | 30 <sup>a</sup>                                      |                   | 30 <sup>a</sup>                                      |     |                    |
| 39     | T <sub>WES</sub>      | AS and DS Coincident Low for Reset              | 250 <sup>a</sup>                                     |                   | 200 <sup>a</sup>                                     |                   | 160 <sup>a</sup>                                     |     | 7                  |
| 40     | T <sub>PCI</sub>      | PCLK Low Width                                  | 105 <sup>a</sup>                                     | 2000 <sup>a</sup> | 70 <sup>a</sup>                                      | 1000 <sup>a</sup> | 50 <sup>a</sup>                                      |     |                    |
| 41     | T <sub>PCn</sub>      | PCLK High Width                                 | 105 <sup>a</sup>                                     | 2000 <sup>a</sup> | 70 <sup>a</sup>                                      | 1000 <sup>a</sup> | 50 <sup>a</sup>                                      |     |                    |
| 42     | T <sub>CPC</sub>      | PCLK Cycle Time                                 | 250 <sup>a</sup>                                     | 4000 <sup>a</sup> | 165 <sup>a</sup>                                     | 2000 <sup>a</sup> | 120 <sup>a</sup>                                     |     |                    |
| 43     | T <sub>PC</sub>       | PCLK Rise Time                                  | 20 <sup>a</sup>                                      |                   | 10 <sup>a</sup>                                      |                   | 10 <sup>a</sup>                                      |     |                    |
| 44     | T <sub>PC</sub>       | PCLK Fall Time                                  | 20 <sup>a</sup>                                      |                   | 10 <sup>a</sup>                                      |                   | 10 <sup>a</sup>                                      |     |                    |

## NOTES

- Float delay is defined as the time required for a  $\pm 0.5V$  change in the output with a maximum dc load and a minimum ac load.
- Open-drain output, measured with open-drain test load.
- Parameter is system dependent. For any Z80C in the data chain, T<sub>AS(DSA)</sub> must be greater than the sum of T<sub>AS(EO)</sub> for the highest priority device in the data chain, T<sub>IE(DSA)</sub> for the Z80C, and T<sub>IE(EO)</sub> for each device separating them in the data chain.
- Parameter applies only to a Z80C pulling INT Low at the beginning of the Interrupt Acknowledge transaction.
- Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the Z80C.
- Timings are preliminary and subject to change. All timing references assume 2.0V for a logic "1" and 0.5V for a logic "0".
- Units in nanoseconds (ns).

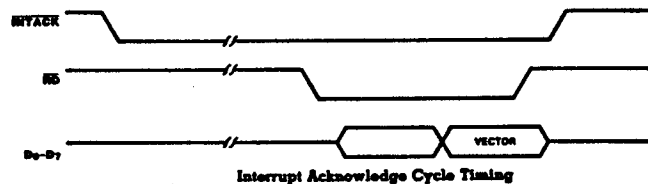
# Z8030/Z8530 SYSTEM TIMING AC CHARACTERISTICS

| Number | Symbol            | Parameter                                | 4 MHz |     | 6 MHz |     | 8 MHz |     | Notes*† |
|--------|-------------------|------------------------------------------|-------|-----|-------|-----|-------|-----|---------|
|        |                   |                                          | Min   | Max | Min   | Max | Min   | Max |         |
| 1      | TdRXC(REQ)        | RxC ↑ to W/REQ Valid Delay               | 8     | 12  | 8     | 12  | 8     | 12  | 2       |
| 2      | TdRXC(W)          | RxC ↑ to Wait Inactive Delay             | 8     | 14  | 8     | 14  | 8     | 14  | 1,2     |
| 3      | TdRXC(SY)         | RxC ↑ to SYNC Valid Delay                | 4     | 7   | 4     | 7   | 4     | 7   | 2       |
| 4a.    | TdRXC(INT), Z8530 | RxC ↑ to INT Valid Delay                 | 10    | 16  | 10    | 16  | 10    | 16  | 1,2     |
| 4b.    | TdRXC(INT), Z8030 |                                          | 8     | 12  | 8     | 12  | 8     | 12  | 1,2     |
|        |                   |                                          | +2    | +3  | +2    | +3  | +2    | +3  | 4       |
| 5      | TdTXC(REQ)        | TxC ↓ to W/REQ Valid Delay               | 5     | 8   | 5     | 8   | 5     | 8   | 3       |
| 6      | TdTXC(W)          | TxC ↓ to Wait Inactive Delay             | 5     | 11  | 5     | 11  | 5     | 11  | 1,3     |
| 7      | TdTXC(DRO)        | TxC ↓ DTR/REQ Valid Delay                | 4     | 7   | 4     | 7   | 4     | 7   | 3       |
| 8a.    | TdTXC(INT), Z8530 | TxC ↓ to INT Valid Delay                 | 6     | 10  | 6     | 10  | 6     | 10  | 1,3     |
| 8b.    | TdTXC(INT), Z8030 |                                          | 4     | 6   | 4     | 6   | 4     | 6   | 1,3     |
|        |                   |                                          | +2    | +3  | +2    | +3  | +2    | +3  | 4       |
| 9a.    | TdSY(INT), Z8530  | SYNC Transition to INT Valid Delay       | 2     | 6   | 2     | 6   | 2     | 6   | 1       |
| 9b.    | TdSY(INT), Z8030  |                                          | 2     | 3   | 2     | 3   | 2     | 3   | 1,4     |
| 10a.   | TdEXT(INT), Z8530 | DCD or CTS Transition to INT Valid Delay | 2     | 6   | 2     | 6   | 2     | 6   | 1       |
| 10b.   | TdEXT(INT), Z8030 |                                          | 2     | 3   | 2     | 3   | 2     | 3   | 1,4     |

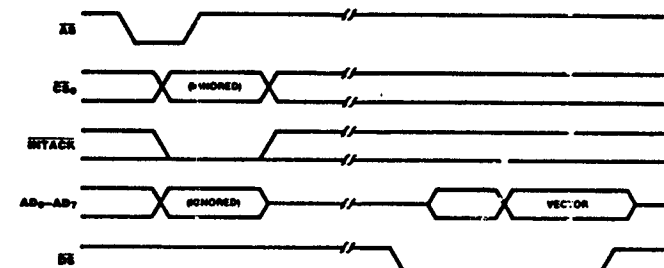
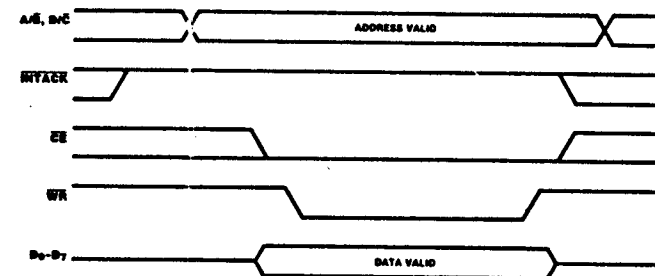
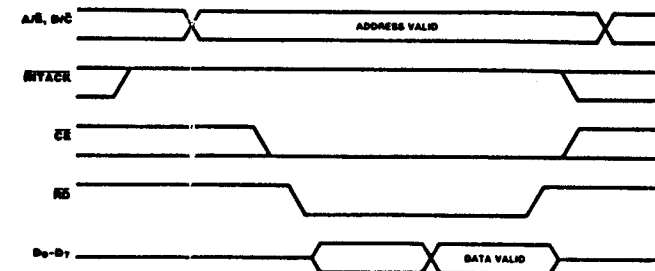
## NOTES:

- Open-drain output, measured with open-drain test load.
- RxC is RTxC or TRxC, whichever is supplying the receive clock.
- TxC is TRxC or RTxC, whichever is supplying the transmit clock.
- Units equal to  $\Delta S$ .

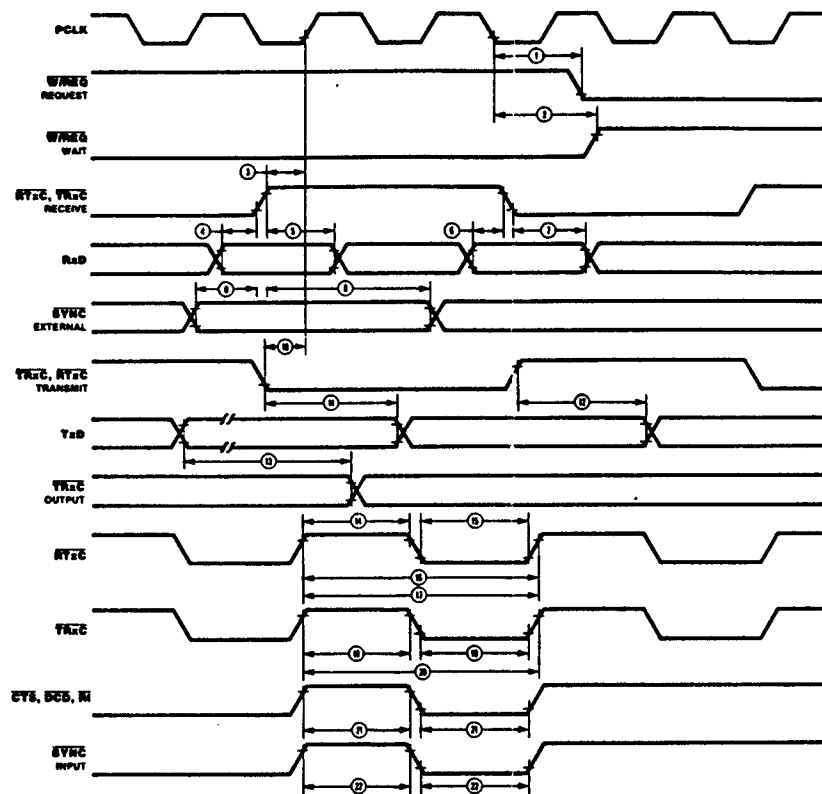
\*Timings are preliminary and subject to change.  
†Units equal to TdPC.



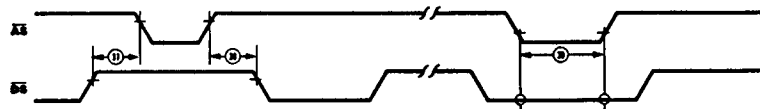
## Z8530 Timing



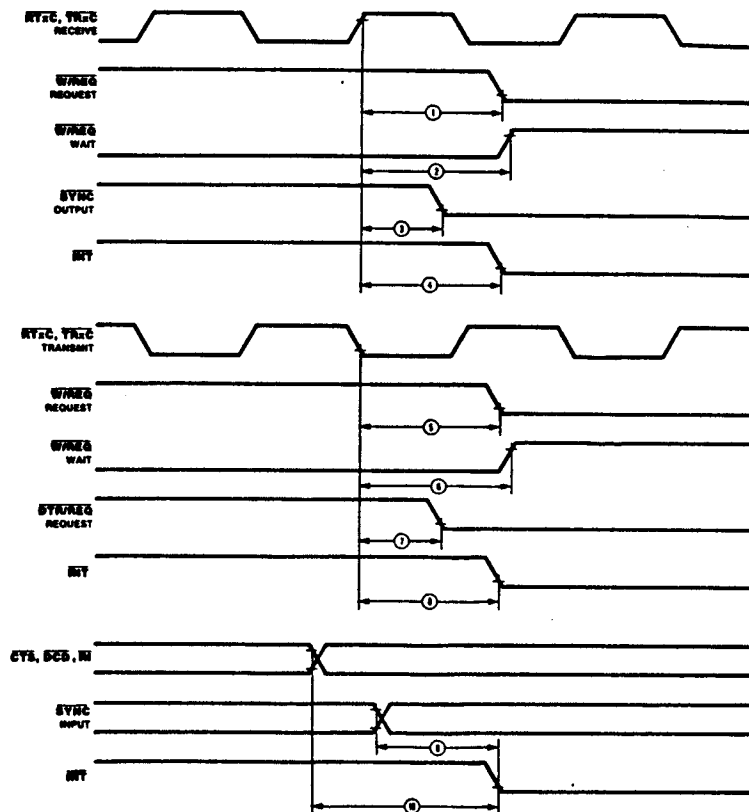
# General Timing



# Reset Timing Z8030



# System Timing



# Z8530 AC CHARACTERISTICS

| Number | Symbol    | Parameter                         | 4 MHz            |                   | 6 MHz            |                   | 8 MHz            |                   | Notes† |
|--------|-----------|-----------------------------------|------------------|-------------------|------------------|-------------------|------------------|-------------------|--------|
|        |           |                                   | Min              | Max               | Min              | Max               | Min              | Max               |        |
| 1      | TwPCI     | PCLK Low Width                    | 105 <sup>a</sup> | 2000 <sup>a</sup> | 70 <sup>a</sup>  | 1000 <sup>a</sup> | 50 <sup>a</sup>  | 1000 <sup>a</sup> |        |
| 2      | TwPCh     | PCLK High Width                   | 105 <sup>a</sup> | 2000 <sup>a</sup> | 70 <sup>a</sup>  | 1000 <sup>a</sup> | 50 <sup>c</sup>  | 1000 <sup>a</sup> |        |
| 3      | TfPC      | PCLK Fall Time                    |                  | 20 <sup>a</sup>   |                  | 10 <sup>a</sup>   |                  | 10 <sup>a</sup>   |        |
| 4      | TrPC      | PCLK Rise Time                    |                  | 20 <sup>a</sup>   |                  | 10 <sup>a</sup>   |                  | 10 <sup>a</sup>   |        |
| 5      | TcPC      | PCLK Cycle Time                   | 250 <sup>a</sup> | 4000 <sup>a</sup> | 165 <sup>a</sup> | 2000 <sup>a</sup> | 125 <sup>a</sup> | 2000 <sup>a</sup> |        |
| 6      | TsA(WR)   | Address to WR ↓ Setup Time        | 80 <sup>a</sup>  |                   | 80 <sup>a</sup>  |                   | 70 <sup>a</sup>  |                   |        |
| 7      | ThA(WR)   | Address to WR ↑ Hold Time         | 0 <sup>c</sup>   |                   | 0 <sup>c</sup>   |                   | 0 <sup>c</sup>   |                   |        |
| 8      | TsA(RD)   | Address to RD ↓ Setup Time        | 80 <sup>a</sup>  |                   | 80 <sup>a</sup>  |                   | 70 <sup>a</sup>  |                   |        |
| 9      | ThA(RD)   | Address to RD ↑ Hold Time         | 0 <sup>c</sup>   |                   | 0 <sup>c</sup>   |                   | 0 <sup>c</sup>   |                   |        |
| 10     | TsIA(PC)  | INTACK to PCLK ↑ Setup Time       | 10 <sup>a</sup>  |                   | 10 <sup>a</sup>  |                   | 10 <sup>a</sup>  |                   |        |
| 11     | TsIA(WR)  | INTACK to WR ↓ Setup Time         | 200 <sup>a</sup> |                   | 160 <sup>a</sup> |                   | 145 <sup>a</sup> |                   | 1      |
| 12     | ThIA(WR)  | INTACK to WR ↑ Hold Time          | 0 <sup>c</sup>   |                   | 0 <sup>c</sup>   |                   | 0 <sup>c</sup>   |                   |        |
| 13     | TsIA(RD)  | INTACK to RD ↓ Setup Time         | 200 <sup>a</sup> |                   | 160 <sup>a</sup> |                   | 145 <sup>a</sup> |                   | 1      |
| 14     | ThIA(RD)  | INTACK to RD ↑ Hold Time          | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   |        |
| 15     | ThIA(PC)  | INTACK to PCLK ↑ Hold Time        | 100 <sup>a</sup> |                   | 100 <sup>a</sup> |                   | 85 <sup>a</sup>  |                   |        |
| 16     | TsCE(WR)  | CE Low to WR ↓ Setup Time         | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   |        |
| 17     | ThCE(WR)  | CE to WR ↑ Hold Time              | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   |        |
| 18     | TsCEh(WR) | CE High to WR ↓ Setup Time        | 100 <sup>a</sup> |                   | 70 <sup>a</sup>  |                   | 60 <sup>a</sup>  |                   |        |
| 19     | TsCE(RD)  | CE Low to RD ↓ Setup Time         | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   | 1      |
| 20     | ThCE(RD)  | CE to RD ↑ Hold Time              | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   | 1      |
| 21     | TsCEh(RD) | CE High to RD ↓ Setup Time        | 100 <sup>a</sup> |                   | 70 <sup>a</sup>  |                   | 60 <sup>a</sup>  |                   | 1      |
| 22     | TwRDI     | RD Low Width                      | 390 <sup>a</sup> |                   | 200 <sup>a</sup> |                   | 150 <sup>a</sup> |                   | 1      |
| 23     | TdRD(DRA) | RD ↓ to Read Data Active Delay    | 0 <sup>c</sup>   |                   | 0 <sup>c</sup>   |                   | 0 <sup>c</sup>   |                   |        |
| 24     | TdRD(DR)  | RD ↑ to Read Data Not Valid Delay | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   | 0 <sup>a</sup>   |                   |        |
| 25     | TdRD(DR)  | RD ↓ to Read Data Valid Delay     |                  | 250 <sup>a</sup>  |                  | 180 <sup>a</sup>  |                  | 140 <sup>a</sup>  |        |
| 26     | TdRD(DRz) | RD ↑ to Read Data Float Delay     |                  | 70 <sup>a</sup>   |                  | 45 <sup>a</sup>   |                  | 40 <sup>a</sup>   | 2      |

## NOTES:

- Parameter does not apply to Interrupt Acknowledge transactions.
- Float delay is defined as the time required for a  $\pm 0.5V$  change at the output with a maximum dc load and minimum ac load.
- \*Timings are preliminary and subject to change.
- †Units in nanoseconds (ns).

# Z8530 AC CHARACTERISTICS (Continued)

| Number | Symbol     | Parameter                                       | 4 MHz            |                                          | 6 MHz            |                                          | 8 MHz            |                                          | Notes† |
|--------|------------|-------------------------------------------------|------------------|------------------------------------------|------------------|------------------------------------------|------------------|------------------------------------------|--------|
|        |            |                                                 | Min              | Max                                      | Min              | Max                                      | Min              | Max                                      |        |
| 27     | TdA(DR)    | Address Required Valid to Read Data Valid Delay |                  | 300 <sup>a</sup>                         |                  | 280 <sup>a</sup>                         |                  | 220 <sup>a</sup>                         |        |
| 28     | TwWR       | WR Low Width                                    | 240 <sup>a</sup> |                                          | 200 <sup>a</sup> |                                          | 150 <sup>a</sup> |                                          |        |
| 29     | TdWR(WR)   | Write Data to WR ↓ Setup Time                   | 10 <sup>a</sup>  |                                          | 10 <sup>a</sup>  |                                          | 10 <sup>a</sup>  |                                          |        |
| 30     | ThDW(WR)   | Write Data to WR ↑ Hold Time                    | 0 <sup>c</sup>   |                                          | 0 <sup>c</sup>   |                                          | 0 <sup>c</sup>   |                                          |        |
| 31     | TdWR(W)    | WR ↓ to Wait 't Valid Delay                     |                  | 240 <sup>a</sup>                         |                  | 200 <sup>a</sup>                         |                  | 170 <sup>a</sup>                         | 4      |
| 32     | TdRD(W)    | RD ↓ Wait Valid Delay                           |                  | 240 <sup>a</sup>                         |                  | 200 <sup>a</sup>                         |                  | 170 <sup>a</sup>                         | 4      |
| 33     | TdWR(REQ)  | WR ↓ to W/REQ Not Valid Delay                   |                  | 240 <sup>a</sup>                         |                  | 200 <sup>a</sup>                         |                  | 170 <sup>a</sup>                         |        |
| 34     | TdRD(REQ)  | RD ↓ to R/REQ Not Valid Delay                   |                  | 240 <sup>a</sup>                         |                  | 200 <sup>a</sup>                         |                  | 170 <sup>a</sup>                         |        |
| 35     | TdWR(REQ)  | WR ↓ to DTR/REQ Not Valid Delay                 |                  | 5TcPC <sup>a</sup><br>+ 300 <sup>a</sup> |                  | 5TcPC <sup>a</sup><br>+ 250 <sup>a</sup> |                  | 5TcPC <sup>a</sup><br>+ 225 <sup>a</sup> |        |
| 36     | TdRD(REQ)  | RD ↓ to DTR/REQ Not Valid Delay                 |                  | 5TcPC <sup>a</sup><br>+ 300 <sup>a</sup> |                  | 5TcPC <sup>a</sup><br>+ 250 <sup>a</sup> |                  | 5TcPC <sup>a</sup><br>+ 200 <sup>a</sup> |        |
| 37     | TdPC(INT)  | PCLK ↓ to INT Valid Delay                       |                  | 500 <sup>a</sup>                         |                  | 500 <sup>a</sup>                         |                  | 500 <sup>a</sup>                         | 4      |
| 38     | TdIA(RD)   | INTACK to RD ↓ (Acknowledge) Delay              | 250 <sup>a</sup> |                                          | 200 <sup>a</sup> |                                          | 150 <sup>a</sup> |                                          | 5      |
| 39     | TwRDA      | RD (Acknowledge) Width                          | 250 <sup>a</sup> |                                          | 200 <sup>a</sup> |                                          | 150 <sup>a</sup> |                                          |        |
| 40     | TdRDA(DR)  | RD ↓ (Acknowledge) to Read Data Valid Delay     |                  | 250 <sup>a</sup>                         |                  | 180 <sup>a</sup>                         |                  | 140 <sup>a</sup>                         |        |
| 41     | TsIE(RDA)  | IEI to RD ↓ (Acknowledge) Setup Time            | 120 <sup>c</sup> |                                          | 100 <sup>c</sup> |                                          | 95 <sup>c</sup>  |                                          |        |
| 42     | ThIE(RDA)  | IEI to RD ↑ (Acknowledge) Hold Time             | 0 <sup>a</sup>   |                                          | 0 <sup>a</sup>   |                                          | 0 <sup>a</sup>   |                                          |        |
| 43     | TdIE(IEO)  | IEI to IEO Delay Time                           |                  | 120 <sup>c</sup>                         |                  | 100 <sup>c</sup>                         |                  | 95 <sup>c</sup>                          |        |
| 44     | TdPC(IEO)  | PCLK ↑ to IE ↓ Delay                            |                  | 250 <sup>a</sup>                         |                  | 250 <sup>a</sup>                         |                  | 200 <sup>a</sup>                         |        |
| 45     | TdRDA(INT) | RD ↓ to INT Inactive Delay                      |                  | 500 <sup>c</sup>                         |                  | 500 <sup>c</sup>                         |                  | 450 <sup>a</sup>                         | 4      |
| 46     | TdRD(WRQ)  | RD ↑ to WR ↓ Delay for No Reset                 | 30 <sup>c</sup>  |                                          | 15 <sup>c</sup>  |                                          | 15 <sup>c</sup>  |                                          |        |
| 47     | TdWRQ(RD)  | WR ↑ to RD ↓ Delay for No Reset                 | 30 <sup>c</sup>  |                                          | 30 <sup>c</sup>  |                                          | 20 <sup>c</sup>  |                                          |        |
| 48     | TwRES      | WR and RD Coincident Low for Reset              | 250 <sup>a</sup> |                                          | 200 <sup>a</sup> |                                          | 150 <sup>a</sup> |                                          |        |
| 49     | Trc        | Valid Access Recovery Time                      |                  | 4TcPC <sup>a</sup>                       |                  | 4TcPC <sup>a</sup>                       |                  | 4TcPC <sup>a</sup>                       | 3      |

## NOTES:

- Parameter applies only between transactions involving the SCC.
- Open-drain output, measured with open-drain test load.
- Parameter is system dependent. For any SCC in the data chain, TdIA(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the data chain, TsIE(RDA) for the SCC, and TdIE(IEO) for each device separating them in the data chain.
- \*Timings are preliminary and subject to change.
- †Units in nanoseconds (ns).

- a Tested  
b Guaranteed by Design  
c Guaranteed by Characterization

# Z8030/Z8530 GENERAL TIMING AC CHARACTERISTICS

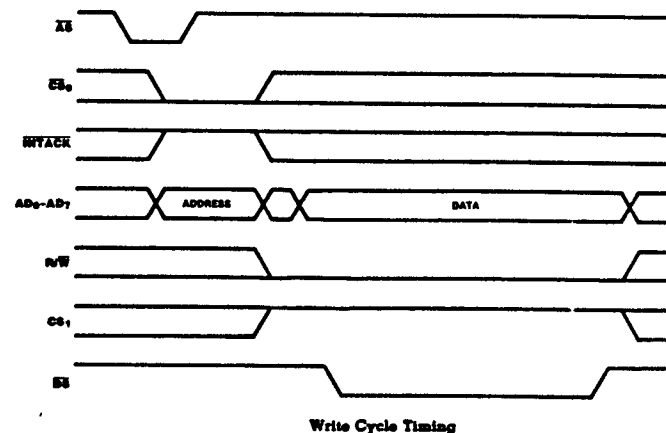
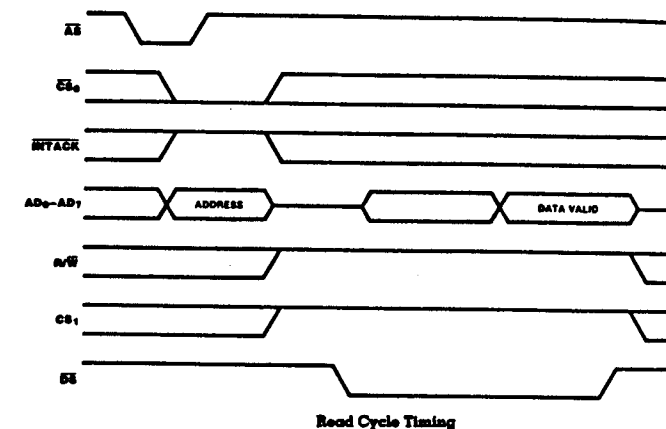
| Number | Symbol      | Parameter                                           | 4 MHz                      |                    | 6 MHz                      |                    | 8 MHz                      |                    | Notes*† |
|--------|-------------|-----------------------------------------------------|----------------------------|--------------------|----------------------------|--------------------|----------------------------|--------------------|---------|
|        |             |                                                     | Min                        | Max                | Min                        | Max                | Min                        | Max                |         |
| 1      | TdPC(REQ)   | PCLK ↓ to $\overline{W}/\overline{REQ}$ Valid Delay |                            | 250 <sup>a</sup>   |                            | 250 <sup>a</sup>   |                            | 250 <sup>a</sup>   |         |
| 2      | TdPC(W)     | PCLK ↓ to Wait Inactive Delay                       |                            | 350 <sup>a</sup>   |                            | 350 <sup>a</sup>   |                            | 350 <sup>a</sup>   |         |
| 3      | TsRXC(PC)   | RxC ↑ to PCLK ↑ Setup Time<br>(PCLK + 4 case only)  | 80                         | TwPCL <sup>c</sup> | 70                         | TwPCL <sup>c</sup> | 60                         | TwPCL <sup>c</sup> | 1,4     |
| 4      | TsRXD(RXCi) | RxD to RxC ↑ Setup Time (X1 Mode)                   | 0 <sup>a</sup>             |                    | 0 <sup>a</sup>             |                    | 0 <sup>a</sup>             |                    | 1       |
| 5      | ThRXD(RXCi) | RxD to RxC ↑ Hold Time (X1 Mode)                    | 150 <sup>a</sup>           |                    | 150 <sup>a</sup>           |                    | 150 <sup>a</sup>           |                    | 1       |
| 6      | TsRXD(RXCf) | RxD to RxC ↓ Setup Time (X1 Mode)                   | 0 <sup>a</sup>             |                    | 0 <sup>a</sup>             |                    | 0 <sup>a</sup>             |                    | 1,5     |
| 7      | ThRXD(RXCf) | RxD to RxC ↓ Hold Time (X1 Mode)                    | 150 <sup>c</sup>           |                    | 150 <sup>c</sup>           |                    | 150 <sup>c</sup>           |                    | 1,5     |
| 8      | TsSY(RXC)   | SYNC to RxC ↑ Setup Time                            | -200 <sup>a</sup>          |                    | -200 <sup>a</sup>          |                    | -200 <sup>a</sup>          |                    | 1       |
| 9      | ThSY(RXC)   | SYNC to RxC ↑ Hold Time                             | 3TcPC <sup>c</sup><br>+400 |                    | 3TcPC <sup>c</sup><br>+320 |                    | 3TcPC <sup>c</sup><br>+250 |                    | 1       |
| 10     | TsTXC(PC)   | TxC ↓ to PCLK ↑ Setup Time                          | 0 <sup>a</sup>             |                    | 0 <sup>a</sup>             |                    | 0 <sup>a</sup>             |                    | 2,4     |
| 11     | TdTXCi(TXD) | TxC ↓ to Tx D Delay (X1 Mode)                       |                            | 300 <sup>a</sup>   |                            | 230 <sup>a</sup>   |                            | 200 <sup>a</sup>   | 2       |
| 12     | TdTXCf(TXD) | TxC ↑ to Tx D Delay (X1 Mode)                       |                            | 300 <sup>a</sup>   |                            | 230 <sup>a</sup>   |                            | 200 <sup>a</sup>   | 2,5     |
| 13     | TdTXD(TRX)  | TxD to TRxC Delay (Send Clock Echo)                 |                            | 200 <sup>a</sup>   |                            | 200 <sup>a</sup>   |                            | 200 <sup>a</sup>   |         |
| 14     | TwRTXh      | TRxC High Width                                     | 180 <sup>a</sup>           |                    | 180 <sup>a</sup>           |                    | 150 <sup>a</sup>           |                    | 6       |
| 15     | TwRTXi      | TRxC Low Width                                      | 180 <sup>a</sup>           |                    | 180 <sup>a</sup>           |                    | 150 <sup>a</sup>           |                    | 6       |
| 16     | TcRTX       | TRxC Cycle Time (RxD, Tx D)                         | 1000 <sup>a</sup>          |                    | 640 <sup>a</sup>           |                    | 500 <sup>a</sup>           |                    | 6,7     |
| 17     | TcRTXX      | Crystal Oscillator Period                           | 250 <sup>c</sup>           | 1000 <sup>c</sup>  | 165 <sup>c</sup>           | 1000 <sup>c</sup>  | 125 <sup>c</sup>           | 1000 <sup>c</sup>  | 3       |
| 18     | TwTRXh      | TRxC High Width                                     | 180 <sup>a</sup>           |                    | 180 <sup>a</sup>           |                    | 150 <sup>a</sup>           |                    | 6       |
| 19     | TwTRXi      | TRxC Low Width                                      | 180 <sup>a</sup>           |                    | 180 <sup>a</sup>           |                    | 150 <sup>a</sup>           |                    | 6       |
| 20     | TcTRX       | TRxC Cycle Time                                     | 1000 <sup>a</sup>          |                    | 640 <sup>a</sup>           |                    | 500 <sup>a</sup>           |                    | 6,7     |
| 21     | TwEXT       | DCD or CTS Pulse Width                              | 200 <sup>a</sup>           |                    | 200 <sup>a</sup>           |                    | 200 <sup>a</sup>           |                    |         |
| 22     | TwSY        | SYNC Pulse Width                                    | 200 <sup>a</sup>           |                    | 200 <sup>a</sup>           |                    | 200 <sup>a</sup>           |                    |         |

## NOTES:

1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. Tx C is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 30 pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or Tx C and PCLK is required.

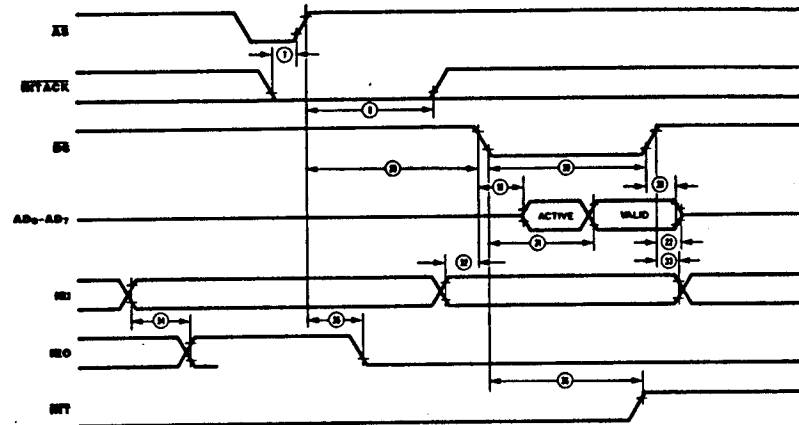
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.  
\*Timings are preliminary and subject to change.  
†Units in nanoseconds (ns).

## Z8030 Timing

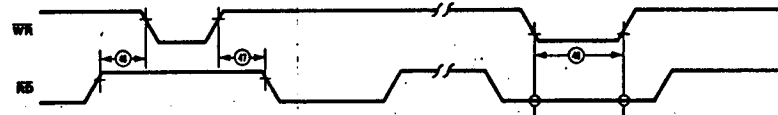


- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization

**Interrupt  
Acknowledge  
Timing  
Z8030**



**Reset  
Timing  
Z8530**



**Cycle  
Timing  
Z8530**

