S6B33B2

132 RGB Segment & 162 Common Driver For 65,536 Color STN LCD

Jan. 05. 2004
Ver. 1.1

S6B33B2 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Oct. 2002
0.1	Added OTP Calibration Mode	Nov.2002
0.2	Added pad coordinate and pad configuration and pad dimension	Jan.2003
0.3	Modify pad name(p6,7) : Dummy<9:8> -> dmy_test<1:0>, Dummy<14:13> -> dmy_test<3:2> Add the dmy_test pin description (p14) Add the Series Specifications (p71) Add the discharge resistor at the system application diagram (P72)	Jun.2003
0.4	Modify the read status flag (P54)	July.2003
1.0	Definition of TBD items Change DLN initial value (P29)	Nov.2003
1.1	Modify the AC Characteristics (P68,69)	Jan.2004
1.2	Modify the AC Characteristics (Data hold Time, P68/P69)	Jan.2004

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INTRODUCTION

S6B33B2 is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip CR oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the LCD driving signal (132 RGB X 162 output) corresponding to the display data and the internal bit-map display RAM of 132 ×163 ×16-bit, S6B33B2 is capable of operating max. 132 RGB x 162 dot LCD panels in low-power consumption. Being the segment RGB 3-output, one pixel is 16-bit data and S6B33B2 can max display 65,536 color.

FEATURES

Driver Output

– 132 RGB x 162

Gray Scale Function

– 65,536 color display of R: 32 gray scale, G: 64 gray scale, B: 32 gray scale
– 4,096 color display of R: 16 gray scale, G: 16 gray scale, B: 16 gray scale
– 256 color display of R: 8 gray scale, G: 8 gray scale, B: 4 gray scale

On-chip Display Data RAM

– Capacity: 132 x 16 x 162 = 342.144k bits
– Burst RAM write function

Display Mode

– Normal display mode: Entire duty displaying, Partial display mode: Partial duty displaying
– Area scroll mode: Particular area scrolling, Standby mode: Internal display clocks off

Microprocessor Interface

– 8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
– 3/4 Pin SPI (only write operation)

On-chip Low Power Analog Circuit

– On-chip CR oscillator (Internal cap. & external resistor), external clock available
– Voltage converter / Voltage regulator / Voltage follower
– On-chip electronic contrast control (256 steps)

Operating Voltage Range

– VDD : 1.8 to 3.3 [V] (without Internal Regulator), 2.4 to 3.3 [V] (With internal Regulator)
– VIN1: 2.4 to 3.6 [V]
– Display operating voltage(V1): 2.0 to 4.0 V
– LCD Operating Voltage Range : Max. 20 V

Low Power Consumption

– 750 μA Typ. (Refer to DC CHARACTERISTICS (2))

Package Type

COG (Output Pad Pitch Min. 40 μm)

Special Features

– Non-Volatile Memory for V1 Calibration

BLOCK DIAGRAM

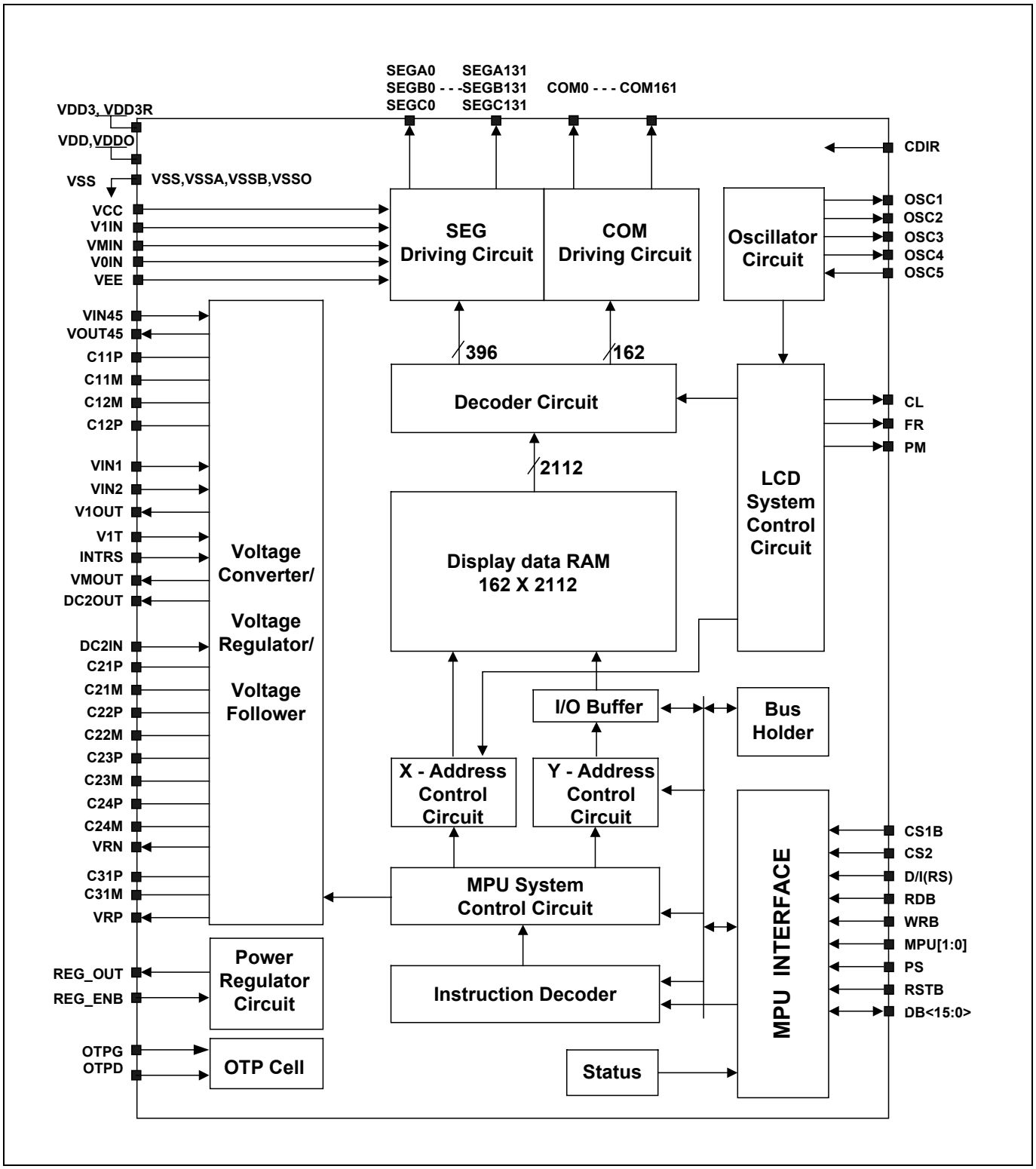


Figure 1. Block Diagram

SAMSUNG ELECTRONICS

PAD CONFIGURATION

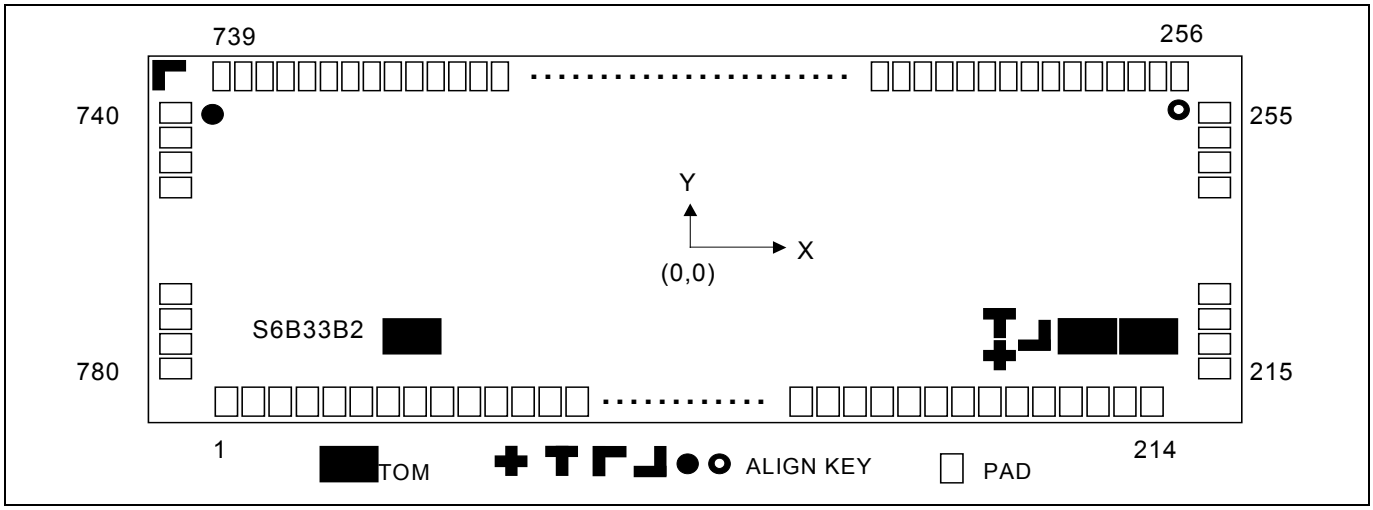


Figure 2. S6B33B2 Chip Pad Configuration

Table 1. S6B33B2 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size (with S/L 120μm)		19960	2130	μm
Pad pitch	1 to 214	90		
	215 to 780	40		
Bumped pad size	1 to 214	70	70	
	215 to 255, 740 to 780	150	25	
	256 to 739	25	150	
Bumped pad height	All pad	17		

COG Align Key Coordinate

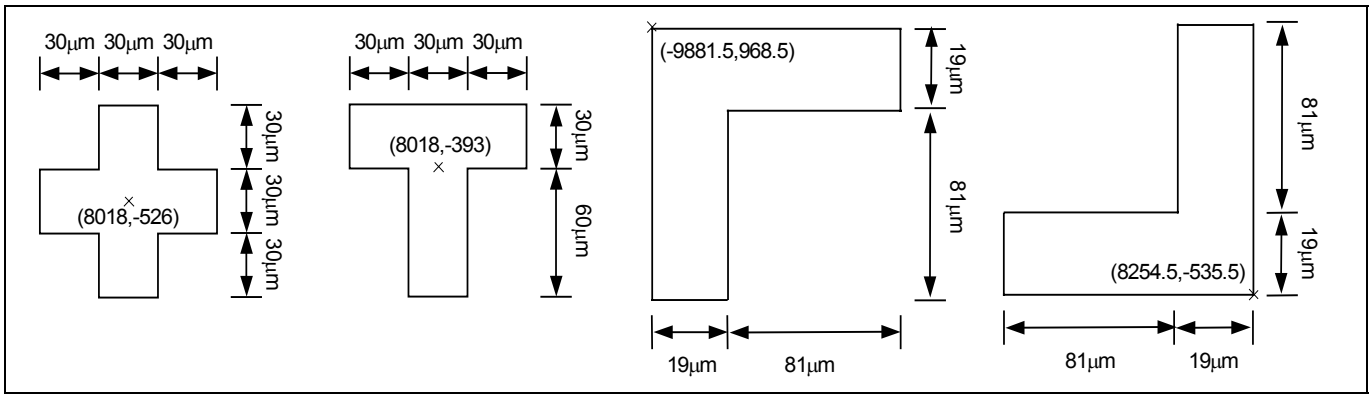
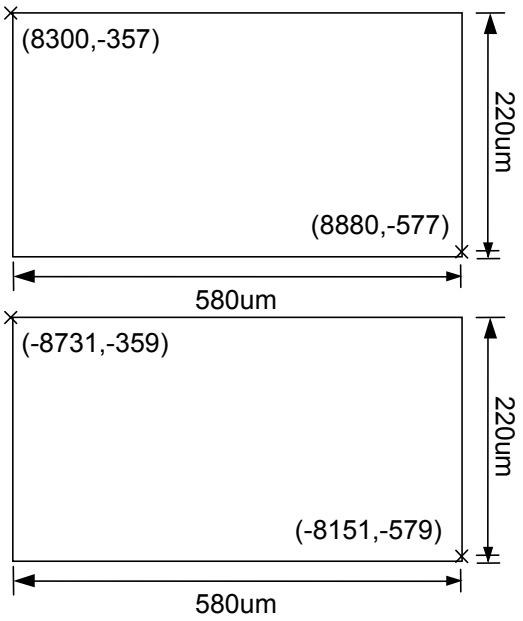


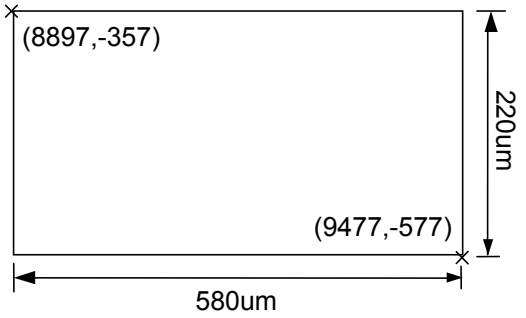
Figure 3. COG Align Key Coordinate

ILB Align Key Coordinate

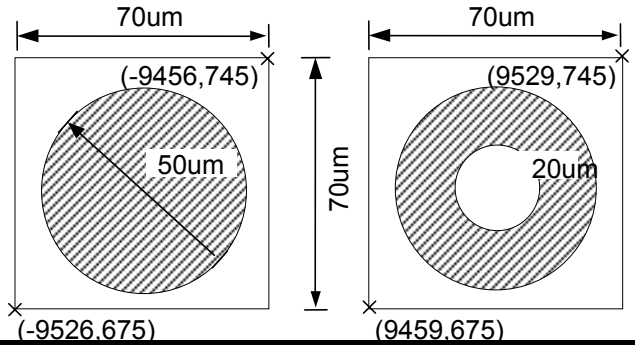
Figure 4. ILB Align Key Coordinate

TOM(TEG On Main chip) Coordinate





COF Align Key Coordinate



SAMSUNG ELECTRONICS

PIN CONFIGURATION

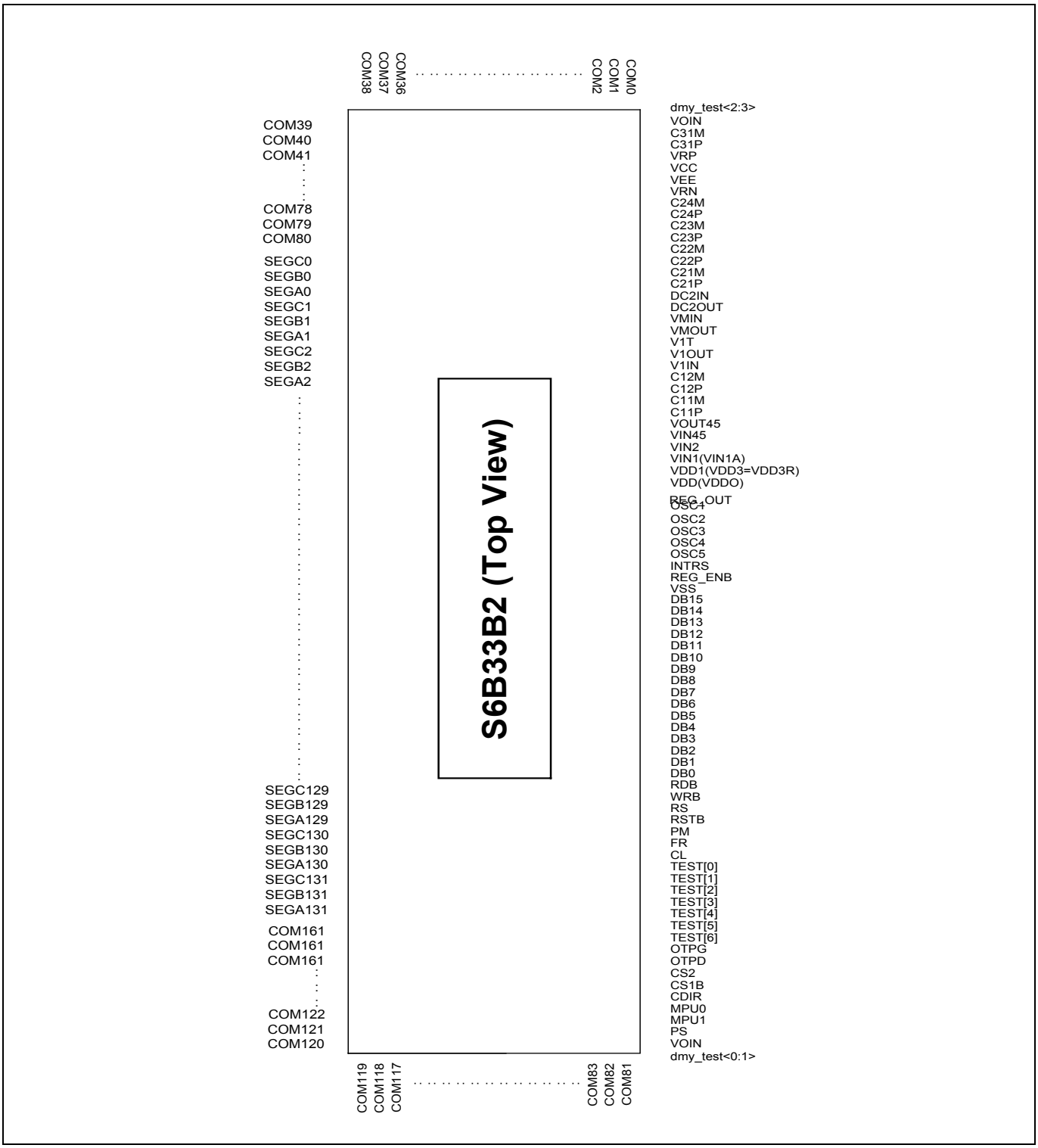


Figure 5. S6B33B2 Chip Pin Configuration

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
1	-9585	-950	dmy_test<0>	51	-5085	-950	DB<12>	101	-585	-950	VDD3R
2	-9495	-950	dmy_test<1>	52	-4995	-950	DB<13>	102	-495	-950	VDD3R
3	-9405	-950	V0IN	53	-4905	-950	DB<14>	103	-405	-950	VDD3
4	-9315	-950	V0IN	54	-4815	-950	DB<15>	104	-315	-950	VDD3
5	-9225	-950	V0IN	55	-4725	-950	VSS	105	-225	-950	VDD3
6	-9135	-950	VSS	56	-4635	-950	VSS	106	-135	-950	VDD3
7	-9045	-950	PS	57	-4545	-950	VSS	107	-45	-950	VIN1A
8	-8955	-950	VDD3	58	-4455	-950	VSS	108	45	-950	VIN1A
9	-8865	-950	MPU<1>	59	-4365	-950	VSS	109	135	-950	VIN1A
10	-8775	-950	VSS	60	-4275	-950	VSS	110	225	-950	VIN1A
11	-8685	-950	MPU<0>	61	-4185	-950	VSS	111	315	-950	VIN1
12	-8595	-950	VDD3	62	-4095	-950	VSS	112	405	-950	VIN1
13	-8505	-950	CDIR	63	-4005	-950	VSSA	113	495	-950	VIN1
14	-8415	-950	VSS	64	-3915	-950	VSSA	114	585	-950	VIN1
15	-8325	-950	CS1B	65	-3825	-950	VSSA	115	675	-950	VIN1
16	-8235	-950	CS2	66	-3735	-950	VSSA	116	765	-950	VIN1
17	-8145	-950	VDD3	67	-3645	-950	VSSO	117	855	-950	VIN1
18	-8055	-950	OTPD	68	-3555	-950	VSSO	118	945	-950	VIN1
19	-7965	-950	OTPD	69	-3465	-950	VSSB	119	1035	-950	VIN2
20	-7875	-950	OTPG	70	-3375	-950	VSSB	120	1125	-950	VIN2
21	-7785	-950	OTPG	71	-3285	-950	VSSB	121	1215	-950	VIN2
22	-7695	-950	TEST<6>	72	-3195	-950	VSSB	122	1305	-950	VIN2
23	-7605	-950	TEST<5>	73	-3105	-950	VSSB	123	1395	-950	VIN45
24	-7515	-950	TEST<4>	74	-3015	-950	VSSB	124	1485	-950	VIN45
25	-7425	-950	TEST<3>	75	-2925	-950	VSSB	125	1575	-950	VIN45
26	-7335	-950	TEST<2>	76	-2835	-950	VSSB	126	1665	-950	VOUT45
27	-7245	-950	TEST<1>	77	-2745	-950	REG_ENB	127	1755	-950	VOUT45
28	-7155	-950	TEST<0>	78	-2655	-950	VDD3	128	1845	-950	VOUT45
29	-7065	-950	VDD3	79	-2565	-950	INTRS	129	1935	-950	C11P
30	-6975	-950	CL	80	-2475	-950	OSC5	130	2025	-950	C11P
31	-6885	-950	FR	81	-2385	-950	VSS	131	2115	-950	C11P
32	-6795	-950	PM	82	-2295	-950	OSC4	132	2205	-950	C11M
33	-6705	-950	RSTB	83	-2205	-950	OSC3	133	2295	-950	C11M
34	-6615	-950	RS	84	-2115	-950	OSC2	134	2385	-950	C11M
35	-6525	-950	VSS	85	-2025	-950	OSC1	135	2475	-950	C12P
36	-6435	-950	WRB	86	-1935	-950	REG_OUT	136	2565	-950	C12P
37	-6345	-950	RDB	87	-1845	-950	REG_OUT	137	2655	-950	C12P
38	-6255	-950	VDD3	88	-1755	-950	REG_OUT	138	2745	-950	C12M
39	-6165	-950	DB<0>	89	-1665	-950	REG_OUT	139	2835	-950	C12M
40	-6075	-950	DB<1>	90	-1575	-950	VDDO	140	2925	-950	C12M
41	-5985	-950	DB<2>	91	-1485	-950	VDDO	141	3015	-950	V1IN
42	-5895	-950	DB<3>	92	-1395	-950	VDD	142	3105	-950	V1IN
43	-5805	-950	DB<4>	93	-1305	-950	VDD	143	3195	-950	V1IN
44	-5715	-950	DB<5>	94	-1215	-950	VDD	144	3285	-950	V1OUT
45	-5625	-950	DB<6>	95	-1125	-950	VDD	145	3375	-950	V1OUT
46	-5535	-950	DB<7>	96	-1035	-950	VDD	146	3465	-950	V1OUT
47	-5445	-950	DB<8>	97	-945	-950	VDD	147	3555	-950	V1T
48	-5355	-950	DB<9>	98	-855	-950	VDD	148	3645	-950	V1T
49	-5265	-950	DB<10>	99	-765	-950	VDD3R	149	3735	-950	VMOUT
50	-5175	-950	DB<11>	100	-675	-950	VDD3R	150	3825	-950	VMOUT

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
151	3915	-950	VMOUT	201	8415	-950	VRP	251	9824	618	COM<35>
152	4005	-950	VMOUT	202	8505	-950	C31P	252	9824	658	COM<36>
153	4095	-950	VMIN	203	8595	-950	C31P	253	9824	698	COM<37>
154	4185	-950	VMIN	204	8685	-950	C31P	254	9824	738	COM<38>
155	4275	-950	VMIN	205	8775	-950	C31M	255	9824	778	DUMMY<1>
156	4365	-950	VMIN	206	8865	-950	C31M	256	9660	910	DUMMY<2>
157	4455	-950	DC2OUT	207	8955	-950	C31M	257	9620	910	COM<39>
158	4545	-950	DC2OUT	208	9045	-950	DUMMY<12	258	9580	910	COM<40>
159	4635	-950	DC2OUT	209	9135	-950	VSS	259	9540	910	COM<41>
160	4725	-950	DC2IN	210	9225	-950	V0IN	260	9500	910	COM<42>
161	4815	-950	DC2IN	211	9315	-950	V0IN	261	9460	910	COM<43>
162	4905	-950	DC2IN	212	9405	-950	V0IN	262	9420	910	COM<44>
163	4995	-950	C21P	213	9495	-950	dmy_test<2>	263	9380	910	COM<45>
164	5085	-950	C21P	214	9585	-950	dmy_test<3>	264	9340	910	COM<46>
165	5175	-950	C21P	215	9824	-822	DUMMY<0>	265	9300	910	COM<47>
166	5265	-950	C21M	216	9824	-782	COM<0>	266	9260	910	COM<48>
167	5355	-950	C21M	217	9824	-742	COM<1>	267	9220	910	COM<49>
168	5445	-950	C21M	218	9824	-702	COM<2>	268	9180	910	COM<50>
169	5535	-950	C22P	219	9824	-662	COM<3>	269	9140	910	COM<51>
170	5625	-950	C22P	220	9824	-622	COM<4>	270	9100	910	COM<52>
171	5715	-950	C22P	221	9824	-582	COM<5>	271	9060	910	COM<53>
172	5805	-950	C22M	222	9824	-542	COM<6>	272	9020	910	COM<54>
173	5895	-950	C22M	223	9824	-502	COM<7>	273	8980	910	COM<55>
174	5985	-950	C22M	224	9824	-462	COM<8>	274	8940	910	COM<56>
175	6075	-950	C23P	225	9824	-422	COM<9>	275	8900	910	COM<57>
176	6165	-950	C23P	226	9824	-382	COM<10>	276	8860	910	COM<58>
177	6255	-950	C23P	227	9824	-342	COM<11>	277	8820	910	COM<59>
178	6345	-950	C23M	228	9824	-302	COM<12>	278	8780	910	COM<60>
179	6435	-950	C23M	229	9824	-262	COM<13>	279	8740	910	COM<61>
180	6525	-950	C23M	230	9824	-222	COM<14>	280	8700	910	COM<62>
181	6615	-950	C24P	231	9824	-182	COM<15>	281	8660	910	COM<63>
182	6705	-950	C24P	232	9824	-142	COM<16>	282	8620	910	COM<64>
183	6795	-950	C24P	233	9824	-102	COM<17>	283	8580	910	COM<65>
184	6885	-950	C24M	234	9824	-62	COM<18>	284	8540	910	COM<66>
185	6975	-950	C24M	235	9824	-22	COM<19>	285	8500	910	COM<67>
186	7065	-950	C24M	236	9824	18	COM<20>	286	8460	910	COM<68>
187	7155	-950	VRN	237	9824	58	COM<21>	287	8420	910	COM<69>
188	7245	-950	VRN	238	9824	98	COM<22>	288	8380	910	COM<70>
189	7335	-950	VRN	239	9824	138	COM<23>	289	8340	910	COM<71>
190	7425	-950	VEE	240	9824	178	COM<24>	290	8300	910	COM<72>
191	7515	-950	VEE	241	9824	218	COM<25>	291	8260	910	COM<73>
192	7605	-950	VEE	242	9824	258	COM<26>	292	8220	910	COM<74>
193	7695	-950	VEE	243	9824	298	COM<27>	293	8180	910	COM<75>
194	7785	-950	DUMMY<10	244	9824	338	COM<28>	294	8140	910	COM<76>
195	7875	-950	DUMMY<11	245	9824	378	COM<29>	295	8100	910	COM<77>
196	7965	-950	VCC	246	9824	418	COM<30>	296	8060	910	COM<78>
197	8055	-950	VCC	247	9824	458	COM<31>	297	8020	910	COM<79>
198	8145	-950	VCC	248	9824	498	COM<32>	298	7980	910	COM<80>
199	8235	-950	VRP	249	9824	538	COM<33>	299	7940	910	DUMMY<3>
200	8325	-950	VRP	250	9824	578	COM<34>	300	7900	910	SEGC<0>

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
301	7860	910	SEGB<0>	351	5860	910	SEGC<17>	401	3860	910	SEGA<33>
302	7820	910	SEGA<0>	352	5820	910	SEGB<17>	402	3820	910	SEGC<34>
303	7780	910	SEGC<1>	353	5780	910	SEGA<17>	403	3780	910	SEGB<34>
304	7740	910	SEGB<1>	354	5740	910	SEGC<18>	404	3740	910	SEGA<34>
305	7700	910	SEGA<1>	355	5700	910	SEGB<18>	405	3700	910	SEGC<35>
306	7660	910	SEGC<2>	356	5660	910	SEGA<18>	406	3660	910	SEGB<35>
307	7620	910	SEGB<2>	357	5620	910	SEGC<19>	407	3620	910	SEGA<35>
308	7580	910	SEGA<2>	358	5580	910	SEGB<19>	408	3580	910	SEGC<36>
309	7540	910	SEGC<3>	359	5540	910	SEGA<19>	409	3540	910	SEGB<36>
310	7500	910	SEGB<3>	360	5500	910	SEGC<20>	410	3500	910	SEGA<36>
311	7460	910	SEGA<3>	361	5460	910	SEGB<20>	411	3460	910	SEGC<37>
312	7420	910	SEGC<4>	362	5420	910	SEGA<20>	412	3420	910	SEGB<37>
313	7380	910	SEGB<4>	363	5380	910	SEGC<21>	413	3380	910	SEGA<37>
314	7340	910	SEGA<4>	364	5340	910	SEGB<21>	414	3340	910	SEGC<38>
315	7300	910	SEGC<5>	365	5300	910	SEGA<21>	415	3300	910	SEGB<38>
316	7260	910	SEGB<5>	366	5260	910	SEGC<22>	416	3260	910	SEGA<38>
317	7220	910	SEGA<5>	367	5220	910	SEGB<22>	417	3220	910	SEGC<39>
318	7180	910	SEGC<6>	368	5180	910	SEGA<22>	418	3180	910	SEGB<39>
319	7140	910	SEGB<6>	369	5140	910	SEGC<23>	419	3140	910	SEGA<39>
320	7100	910	SEGA<6>	370	5100	910	SEGB<23>	420	3100	910	SEGC<40>
321	7060	910	SEGC<7>	371	5060	910	SEGA<23>	421	3060	910	SEGB<40>
322	7020	910	SEGB<7>	372	5020	910	SEGC<24>	422	3020	910	SEGA<40>
323	6980	910	SEGA<7>	373	4980	910	SEGB<24>	423	2980	910	SEGC<41>
324	6940	910	SEGC<8>	374	4940	910	SEGA<24>	424	2940	910	SEGB<41>
325	6900	910	SEGB<8>	375	4900	910	SEGC<25>	425	2900	910	SEGA<41>
326	6860	910	SEGA<8>	376	4860	910	SEGB<25>	426	2860	910	SEGC<42>
327	6820	910	SEGC<9>	377	4820	910	SEGA<25>	427	2820	910	SEGB<42>
328	6780	910	SEGB<9>	378	4780	910	SEGC<26>	428	2780	910	SEGA<42>
329	6740	910	SEGA<9>	379	4740	910	SEGB<26>	429	2740	910	SEGC<43>
330	6700	910	SEGC<10>	380	4700	910	SEGA<26>	430	2700	910	SEGB<43>
331	6660	910	SEGB<10>	381	4660	910	SEGC<27>	431	2660	910	SEGA<43>
332	6620	910	SEGA<10>	382	4620	910	SEGB<27>	432	2620	910	SEGC<44>
333	6580	910	SEGC<11>	383	4580	910	SEGA<27>	433	2580	910	SEGB<44>
334	6540	910	SEGB<11>	384	4540	910	SEGC<28>	434	2540	910	SEGA<44>
335	6500	910	SEGA<11>	385	4500	910	SEGB<28>	435	2500	910	SEGC<45>
336	6460	910	SEGC<12>	386	4460	910	SEGA<28>	436	2460	910	SEGB<45>
337	6420	910	SEGB<12>	387	4420	910	SEGC<29>	437	2420	910	SEGA<45>
338	6380	910	SEGA<12>	388	4380	910	SEGB<29>	438	2380	910	SEGC<46>
339	6340	910	SEGC<13>	389	4340	910	SEGA<29>	439	2340	910	SEGB<46>
340	6300	910	SEGB<13>	390	4300	910	SEGC<30>	440	2300	910	SEGA<46>
341	6260	910	SEGA<13>	391	4260	910	SEGB<30>	441	2260	910	SEGC<47>
342	6220	910	SEGC<14>	392	4220	910	SEGA<30>	442	2220	910	SEGB<47>
343	6180	910	SEGB<14>	393	4180	910	SEGC<31>	443	2180	910	SEGA<47>
344	6140	910	SEGA<14>	394	4140	910	SEGB<31>	444	2140	910	SEGC<48>
345	6100	910	SEGC<15>	395	4100	910	SEGA<31>	445	2100	910	SEGB<48>
346	6060	910	SEGB<15>	396	4060	910	SEGC<32>	446	2060	910	SEGA<48>
347	6020	910	SEGA<15>	397	4020	910	SEGB<32>	447	2020	910	SEGC<49>
348	5980	910	SEGC<16>	398	3980	910	SEGA<32>	448	1980	910	SEGB<49>
349	5940	910	SEGB<16>	399	3940	910	SEGC<33>	449	1940	910	SEGA<49>
350	5900	910	SEGA<16>	400	3900	910	SEGB<33>	450	1900	910	SEGC<50>

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
451	1860	910	SEGB<50>	501	-140	910	SEGC<67>	551	-2140	910	SEGA<83>
452	1820	910	SEGA<50>	502	-180	910	SEGB<67>	552	-2180	910	SEGC<84>
453	1780	910	SEGC<51>	503	-220	910	SEGA<67>	553	-2220	910	SEGB<84>
454	1740	910	SEGB<51>	504	-260	910	SEGC<68>	554	-2260	910	SEGA<84>
455	1700	910	SEGA<51>	505	-300	910	SEGB<68>	555	-2300	910	SEGC<85>
456	1660	910	SEGC<52>	506	-340	910	SEGA<68>	556	-2340	910	SEGB<85>
457	1620	910	SEGB<52>	507	-380	910	SEGC<69>	557	-2380	910	SEGA<85>
458	1580	910	SEGA<52>	508	-420	910	SEGB<69>	558	-2420	910	SEGC<86>
459	1540	910	SEGC<53>	509	-460	910	SEGA<69>	559	-2460	910	SEGB<86>
460	1500	910	SEGB<53>	510	-500	910	SEGC<70>	560	-2500	910	SEGA<86>
461	1460	910	SEGA<53>	511	-540	910	SEGB<70>	561	-2540	910	SEGC<87>
462	1420	910	SEGC<54>	512	-580	910	SEGA<70>	562	-2580	910	SEGB<87>
463	1380	910	SEGB<54>	513	-620	910	SEGC<71>	563	-2620	910	SEGA<87>
464	1340	910	SEGA<54>	514	-660	910	SEGB<71>	564	-2660	910	SEGC<88>
465	1300	910	SEGC<55>	515	-700	910	SEGA<71>	565	-2700	910	SEGB<88>
466	1260	910	SEGB<55>	516	-740	910	SEGC<72>	566	-2740	910	SEGA<88>
467	1220	910	SEGA<55>	517	-780	910	SEGB<72>	567	-2780	910	SEGC<89>
468	1180	910	SEGC<56>	518	-820	910	SEGA<72>	568	-2820	910	SEGB<89>
469	1140	910	SEGB<56>	519	-860	910	SEGC<73>	569	-2860	910	SEGA<89>
470	1100	910	SEGA<56>	520	-900	910	SEGB<73>	570	-2900	910	SEGC<90>
471	1060	910	SEGC<57>	521	-940	910	SEGA<73>	571	-2940	910	SEGB<90>
472	1020	910	SEGB<57>	522	-980	910	SEGC<74>	572	-2980	910	SEGA<90>
473	980	910	SEGA<57>	523	-1020	910	SEGB<74>	573	-3020	910	SEGC<91>
474	940	910	SEGC<58>	524	-1060	910	SEGA<74>	574	-3060	910	SEGB<91>
475	900	910	SEGB<58>	525	-1100	910	SEGC<75>	575	-3100	910	SEGA<91>
476	860	910	SEGA<58>	526	-1140	910	SEGB<75>	576	-3140	910	SEGC<92>
477	820	910	SEGC<59>	527	-1180	910	SEGA<75>	577	-3180	910	SEGB<92>
478	780	910	SEGB<59>	528	-1220	910	SEGC<76>	578	-3220	910	SEGA<92>
479	740	910	SEGA<59>	529	-1260	910	SEGB<76>	579	-3260	910	SEGC<93>
480	700	910	SEGC<60>	530	-1300	910	SEGA<76>	580	-3300	910	SEGB<93>
481	660	910	SEGB<60>	531	-1340	910	SEGC<77>	581	-3340	910	SEGA<93>
482	620	910	SEGA<60>	532	-1380	910	SEGB<77>	582	-3380	910	SEGC<94>
483	580	910	SEGC<61>	533	-1420	910	SEGA<77>	583	-3420	910	SEGB<94>
484	540	910	SEGB<61>	534	-1460	910	SEGC<78>	584	-3460	910	SEGA<94>
485	500	910	SEGA<61>	535	-1500	910	SEGB<78>	585	-3500	910	SEGC<95>
486	460	910	SEGC<62>	536	-1540	910	SEGA<78>	586	-3540	910	SEGB<95>
487	420	910	SEGB<62>	537	-1580	910	SEGC<79>	587	-3580	910	SEGA<95>
488	380	910	SEGA<62>	538	-1620	910	SEGB<79>	588	-3620	910	SEGC<96>
489	340	910	SEGC<63>	539	-1660	910	SEGA<79>	589	-3660	910	SEGB<96>
490	300	910	SEGB<63>	540	-1700	910	SEGC<80>	590	-3700	910	SEGA<96>
491	260	910	SEGA<63>	541	-1740	910	SEGB<80>	591	-3740	910	SEGC<97>
492	220	910	SEGC<64>	542	-1780	910	SEGA<80>	592	-3780	910	SEGB<97>
493	180	910	SEGB<64>	543	-1820	910	SEGC<81>	593	-3820	910	SEGA<97>
494	140	910	SEGA<64>	544	-1860	910	SEGB<81>	594	-3860	910	SEGC<98>
495	100	910	SEGC<65>	545	-1900	910	SEGA<81>	595	-3900	910	SEGB<98>
496	60	910	SEGB<65>	546	-1940	910	SEGC<82>	596	-3940	910	SEGA<98>
497	20	910	SEGA<65>	547	-1980	910	SEGB<82>	597	-3980	910	SEGC<99>
498	-20	910	SEGC<66>	548	-2020	910	SEGA<82>	598	-4020	910	SEGB<99>
499	-60	910	SEGB<66>	549	-2060	910	SEGC<83>	599	-4060	910	SEGA<99>
500	-100	910	SEGA<66>	550	-2100	910	SEGB<83>	600	-4100	910	SEGC<100>

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME	NO	X	Y	NAME	NO	X	Y	NAME
601	-4140	910	SEGB<100>	651	-6140	910	SEGC<117>	701	-8140	910	COM<157>
602	-4180	910	SEGA<100>	652	-6180	910	SEGB<117>	702	-8180	910	COM<156>
603	-4220	910	SEGC<101>	653	-6220	910	SEGA<117>	703	-8220	910	COM<155>
604	-4260	910	SEGB<101>	654	-6260	910	SEGC<118>	704	-8260	910	COM<154>
605	-4300	910	SEGA<101>	655	-6300	910	SEGB<118>	705	-8300	910	COM<153>
606	-4340	910	SEGC<102>	656	-6340	910	SEGA<118>	706	-8340	910	COM<152>
607	-4380	910	SEGB<102>	657	-6380	910	SEGC<119>	707	-8380	910	COM<151>
608	-4420	910	SEGA<102>	658	-6420	910	SEGB<119>	708	-8420	910	COM<150>
609	-4460	910	SEGC<103>	659	-6460	910	SEGA<119>	709	-8460	910	COM<149>
610	-4500	910	SEGB<103>	660	-6500	910	SEGC<120>	710	-8500	910	COM<148>
611	-4540	910	SEGA<103>	661	-6540	910	SEGB<120>	711	-8540	910	COM<147>
612	-4580	910	SEGC<104>	662	-6580	910	SEGA<120>	712	-8580	910	COM<146>
613	-4620	910	SEGB<104>	663	-6620	910	SEGC<121>	713	-8620	910	COM<145>
614	-4660	910	SEGA<104>	664	-6660	910	SEGB<121>	714	-8660	910	COM<144>
615	-4700	910	SEGC<105>	665	-6700	910	SEGA<121>	715	-8700	910	COM<143>
616	-4740	910	SEGB<105>	666	-6740	910	SEGC<122>	716	-8740	910	COM<142>
617	-4780	910	SEGA<105>	667	-6780	910	SEGB<122>	717	-8780	910	COM<141>
618	-4820	910	SEGC<106>	668	-6820	910	SEGA<122>	718	-8820	910	COM<140>
619	-4860	910	SEGB<106>	669	-6860	910	SEGC<123>	719	-8860	910	COM<139>
620	-4900	910	SEGA<106>	670	-6900	910	SEGB<123>	720	-8900	910	COM<138>
621	-4940	910	SEGC<107>	671	-6940	910	SEGA<123>	721	-8940	910	COM<137>
622	-4980	910	SEGB<107>	672	-6980	910	SEGC<124>	722	-8980	910	COM<136>
623	-5020	910	SEGA<107>	673	-7020	910	SEGB<124>	723	-9020	910	COM<135>
624	-5060	910	SEGC<108>	674	-7060	910	SEGA<124>	724	-9060	910	COM<134>
625	-5100	910	SEGB<108>	675	-7100	910	SEGC<125>	725	-9100	910	COM<133>
626	-5140	910	SEGA<108>	676	-7140	910	SEGB<125>	726	-9140	910	COM<132>
627	-5180	910	SEGC<109>	677	-7180	910	SEGA<125>	727	-9180	910	COM<131>
628	-5220	910	SEGB<109>	678	-7220	910	SEGC<126>	728	-9220	910	COM<130>
629	-5260	910	SEGA<109>	679	-7260	910	SEGB<126>	729	-9260	910	COM<129>
630	-5300	910	SEGC<110>	680	-7300	910	SEGA<126>	730	-9300	910	COM<128>
631	-5340	910	SEGB<110>	681	-7340	910	SEGC<127>	731	-9340	910	COM<127>
632	-5380	910	SEGA<110>	682	-7380	910	SEGB<127>	732	-9380	910	COM<126>
633	-5420	910	SEGC<111>	683	-7420	910	SEGA<127>	733	-9420	910	COM<125>
634	-5460	910	SEGB<111>	684	-7460	910	SEGC<128>	734	-9460	910	COM<124>
635	-5500	910	SEGA<111>	685	-7500	910	SEGB<128>	735	-9500	910	COM<123>
636	-5540	910	SEGC<112>	686	-7540	910	SEGA<128>	736	-9540	910	COM<122>
637	-5580	910	SEGB<112>	687	-7580	910	SEGC<129>	737	-9580	910	COM<121>
638	-5620	910	SEGA<112>	688	-7620	910	SEGB<129>	738	-9620	910	COM<120>
639	-5660	910	SEGC<113>	689	-7660	910	SEGA<129>	739	-9660	910	DUMMY<5>
640	-5700	910	SEGB<113>	690	-7700	910	SEGC<130>	740	-9824	778	DUMMY<6>
641	-5740	910	SEGA<113>	691	-7740	910	SEGB<130>	741	-9824	738	COM<119>
642	-5780	910	SEGC<114>	692	-7780	910	SEGA<130>	742	-9824	698	COM<118>
643	-5820	910	SEGB<114>	693	-7820	910	SEGC<131>	743	-9824	658	COM<117>
644	-5860	910	SEGA<114>	694	-7860	910	SEGB<131>	744	-9824	618	COM<116>
645	-5900	910	SEGC<115>	695	-7900	910	SEGA<131>	745	-9824	578	COM<115>
646	-5940	910	SEGB<115>	696	-7940	910	DUMMY<4>	746	-9824	538	COM<114>
647	-5980	910	SEGA<115>	697	-7980	910	COM<161>	747	-9824	498	COM<113>
648	-6020	910	SEGC<116>	698	-8020	910	COM<160>	748	-9824	458	COM<112>
649	-6060	910	SEGB<116>	699	-8060	910	COM<159>	749	-9824	418	COM<111>
650	-6100	910	SEGA<116>	700	-8100	910	COM<158>	750	-9824	378	COM<110>

SAMSUNG ELECTRONICS

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	X	Y	NAME
751	-9824	338	COM<109>
752	-9824	298	COM<108>
753	-9824	258	COM<107>
754	-9824	218	COM<106>
755	-9824	178	COM<105>
756	-9824	138	COM<104>
757	-9824	98	COM<103>
758	-9824	58	COM<102>
759	-9824	18	COM<101>
760	-9824	-22	COM<100>
761	-9824	-62	COM<99>
762	-9824	-102	COM<98>
763	-9824	-142	COM<97>
764	-9824	-182	COM<96>
765	-9824	-222	COM<95>
766	-9824	-262	COM<94>
767	-9824	-302	COM<93>
768	-9824	-342	COM<92>
769	-9824	-382	COM<91>
770	-9824	-422	COM<90>
771	-9824	-462	COM<89>
772	-9824	-502	COM<88>
773	-9824	-542	COM<87>
774	-9824	-582	COM<86>
775	-9824	-622	COM<85>
776	-9824	-662	COM<84>
777	-9824	-702	COM<83>
778	-9824	-742	COM<82>
779	-9824	-782	COM<81>
780	-9824	-822	DUMMY<7>

PIN DESCRIPTION

Table 3. Power Supply Pins

Name	I/O	Description
VDD3	Supply	Main power supply
VDD3R	Supply	Internal regulator power supply This pin is connected to VDD3.
VDD	Supply	Regulated power supply input pin for internal digital and DDRAM block. This pin is connected to REG_OUT outside the chip with stabilization capacitor. When the internal regulator is not used, VDD1 should be tied to VDD directly.
VDDO	Supply	Internal oscillator power supply This pin is connected to VDD.
VSS VSSO VSSA VSSB	GND	Ground
V1IN / V1OUT	I / O	LCD segment high selected driving voltage input / output pin
VMIN / VMOUT	I / O	LCD common/segment non-selected driving voltage input / output pin
V0IN	I	LCD segment low selected driving voltage input pin
VCC / VRP	I / O	LCD common high selected driving voltage input / output pin
VEE / VRN	I / O	LCD common low selected driving voltage input / output pin The relationship between VCC, V1, VM, V0 and VEE: VCC > V1 > VM > V0(=VSS) > VEE (V1 - VM = VM – V0, VCC –VM = VM - VEE)
VIN1 VIN1A	I	Power supply for 1’st booster circuit and VM amp
VIN2	I	Power supply for 2’nd booster circuit
VOUT45	O	1’st booster output pin
VIN45	I	Power supply for V1. Connect to VOUT45 or VIN1
C11P C11M C12P C12M	O	External capacitor connection pins used for 1’st booster circuit
V1T	I	Thermistor resistor connection pin
INTRS	I	External resister select pin for temperature compensation circuit - INTRS = L : External resistor mode, INTRS = H : Internal resistor mode
DC2IN	I	Power supply for 2’nd booster. Connect to DC2OUT pin
DC2OUT	O	Power output pin for 2’nd booster input
C21P C21M C22P C22M C23P C23M C24P C24M	O	External capacitor connection pins used for 2’nd booster circuit
C31P C31M	O	External capacitor connection pins used for 3’rd booster circuit
OTPG	I	Gate Voltage for OTP programming
OTPD	I	Drain Voltage for OTP programming

Table 4. MPU Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin.
When RSTB is “L”, initialization is executed.</td></tr>
<tr><td>PS
MPU[1:0]</td><td>I</td><td>MPU interface select pin
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU[0]</th><th>Description</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>8080-series 8bit interface</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>8080-series 16bit interface</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>6800-series 8bit interface</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>6800-series 16bit interface</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>3 pin SPI(Write only)</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>4 pin SPI(Write only)</td></tr>
</table></td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB15 may be high impedance.</td></tr>
<tr><td>D/I
(RS)</td><td>I</td><td>Data / Instruction select input pin
– D/I = “H”: DB0 to DB15 are display data
– D/I = “L”: DB0 to DB7 are instruction data</td></tr>
<tr><td>WRB
(R/W)</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>PS</th><th>MPU</th><th>MPU Type</th><th>WRB</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>ReadWRBite control input pin
– R/W = “H”: read
– R/W = “L”: write</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>WRB</td><td>Write enable clock input pin
The data on DB0 to DB15 are latched at the rising edge of the WRB signal.</td></tr>
</table></td></tr>
<tr><td>RDB
(E)</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU[1]</th><th>MPU type</th><th>RDB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– R/W = “H”: When E is “H”, DB0 to DB15 are in an output status.
– R/W = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>RDB</td><td>Read enable clock input pin
When RDB is “L”, DB0 to DB15 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB[15:8]
DB[7]/SDI
DB[6]/SCL
DB[5:0]</td><td>I/O</td><td>-DB[15:0]: 16-bit bi-directional data bus.
-SDI: Serial data input pin. The data is latched at the rising edge of SCL.
-SCL: Serial clock input pin.</td></tr>
<tr><td>CDIR</td><td>I</td><td>Common direction select pin.</td></tr>
</table>

Table 5. Oscillator and Power Regulator Pins

Name	I/O	Description
OSC1 OSC2 OSC3 OSC4	O	CR oscillator output pin When the internal CR oscillator is used, connect to OSC1, OSC3 through a resistor. OSC1 – OSC2: Using in normal display mode, partial display mode 0 OSC3 – OSC4: Using in partial display mode 1 When an external oscillator is used, OSC1 pin is connected to VDD or VSS.
OSC5	I	External clock input pin When an external input is used, it is input to this pin. But the internal oscillator is used, this pin is connected to VDD3 or VSS.
REG_ENB	I	Internal regulator enable/disable input pin - REG_ENB = “L” (tied to VSS) : enable internal regulator - REG_ENB = “H” (tied to VDD3) : disable internal regulator
REG_OUT	O	Internal voltage regulator output pin The regulator output port from this pin is used as a power supplier for an internal digital block via VDD pins.

Table 6. Timing signal Pins for monitoring

Name	I/O	Description
CL	O	Shift clock output pin
PM	O	Field delimiter output pin
FR	O	Liquid crystal alternating current output pin

Table 7. LCD driver output pins

Name	I/O	Description
SEGA0 to 131	O	LCD driving segment output (Red or Blue)
SEGB0 to 131	O	LCD driving segment output (Green)
SEGC0 to131	O	LCD driving segment output (Blue or Red)
COM0 to 161	O	LCD common outputs

Table 8. Test pins

Name	I/O	Description
TEST[3:0]	I	Don’t use these pins. IC maker’s test pins These pins must be tied to VDD3 or VSS.
TEST[6:4]	O	Don’t use these pins. IC maker’s test pins These pins must be open.
dmy_test<3:0>	O	Don’t use these pins. IC maker’s test pins These pins must be open.

FUNCTIONAL DESCRIPTION

MPU INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B33B2 can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, D/I, RDB, and WRB inputs are disabled and DB0 to DB15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel/Serial Interface

The S6B33B2 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table9.

Table 9. Parallel / Serial Interface Mode.

PS	MPU[1]	CS1B	CS2	MPU bus type
H	L	CS1B	CS2	8080-Series MPU
	H			6800-Series MPU
L	L	CS1B	CS2	3–Pin SPI
	H			4-Pin SPI

Parallel Interface (PS=”H”)

The 8-bit/16-bit bi-directional data bus is used in parallel interface. The type of MPU is selected by MPU[1] and the mode of data-bus is controlled by MPU[0] as shown in below. In accessing internal registers (D/I = “L”), only DB[7:0] are valid.

Table 10. Microprocessor Selection for Parallel Interface

MPU[1]	MPU[0]	CS1B	CS2	RDB	WRB	Data Bus	MPU bus type
L	L	CS1B	CS2	RDB	WRB	DB[7:0]	8080-series MPU
	H					DB[15:0]	
H	L	CS1B	CS2	E	R/W	DB[7:0]	6800-series MPU
	H					DB[15:0]	

Table 11. Parallel Data Transfer

D/I	6800-series		8080-series		Description
	RDB	WRB	RDB	WRB	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data

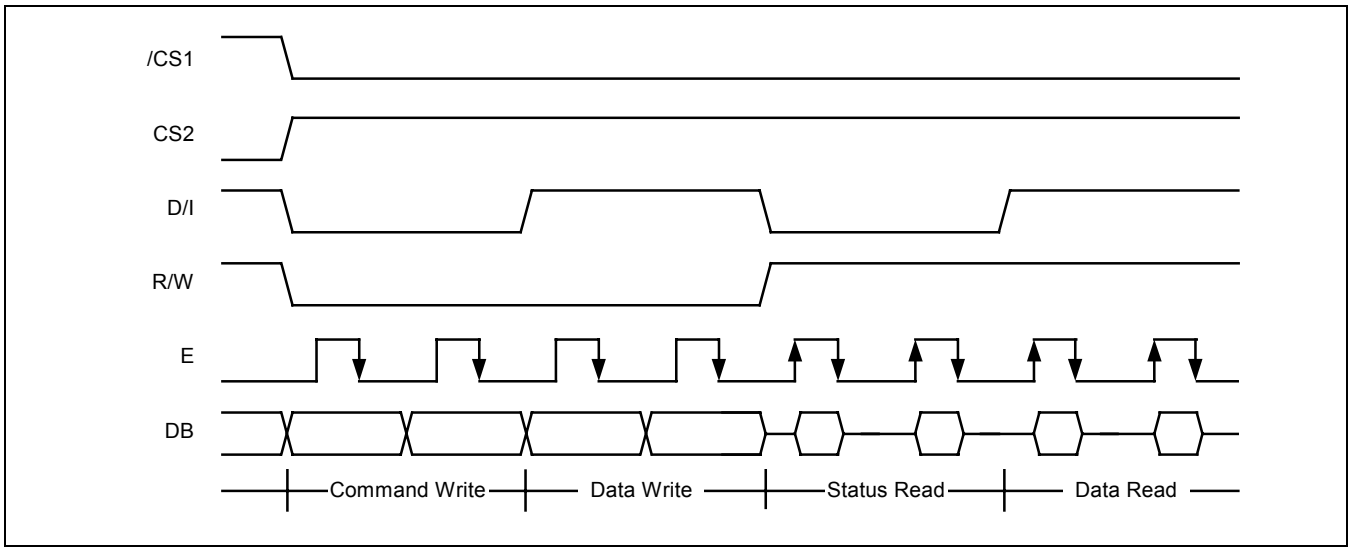


Figure 6. 6800-Series MPU Interface protocol (MPU[1]="H")

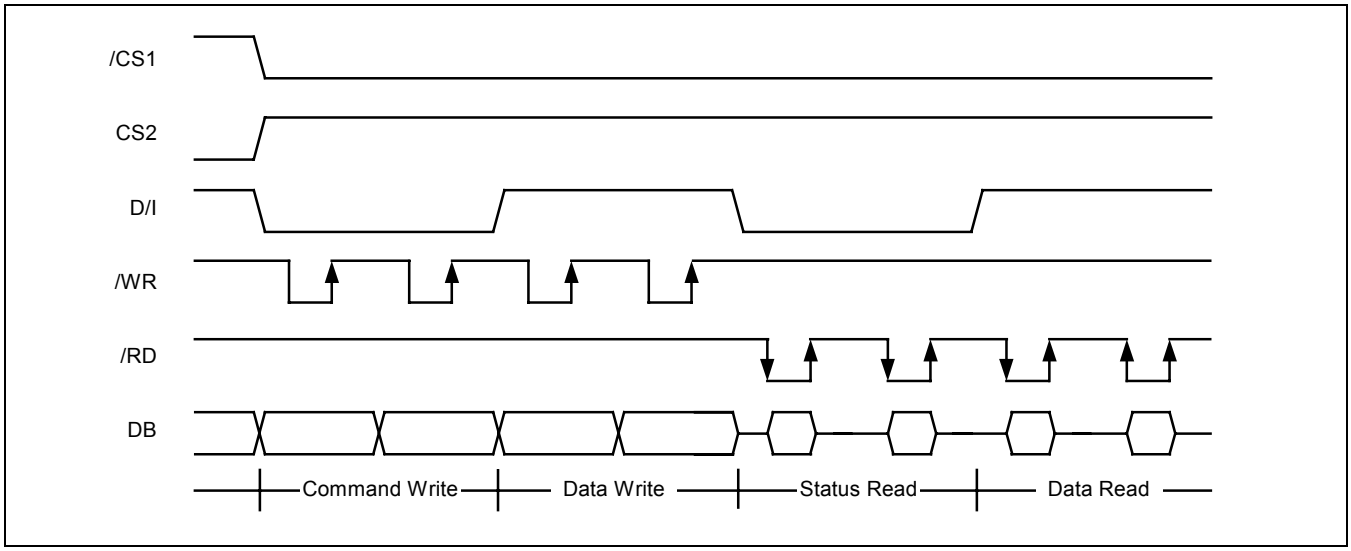


Figure 7. 8080-Series MPU Interface Protocol (MPU[1]="L")

Serial Interface(PS="L")

Communication with the microprocessor occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (CS1B = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8 bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And Invalid, the internal shift register and the counter are reset.
The serial interface type is selected by setting PS as shown in Table12.

Table 12. Microprocessor Selection for Serial Interface

PS	MPU[1]	CS1B	CS2	D/I	Serial Data	Serial Clock	SPI Mode
L	L	CS1B	CS2	By S/W	DB[7]	DB[6]	3-Pin
	H	CS1B	CS2	D/I			4-Pin

3-Pin SPI Interface (PS = "L" & MPU[1] = "L")

In 3-Pin SPI Interface mode, the pre-defined instruction called Display Data Length is used to indicate whether serial data input is display or instruction data instead of D/I pin. The data is handled as instruction data until the Display Data Length instruction is issued. This Display Data Length instruction consists of three bytes instruction. The first byte instruction enables the next instruction to be valid, and data of the second two bytes indicate that a specified number of display data bytes(1 to 65536) are to be transmitted. Next two bytes after the display data string is handled as instruction data. For details, refer the Figure 8.

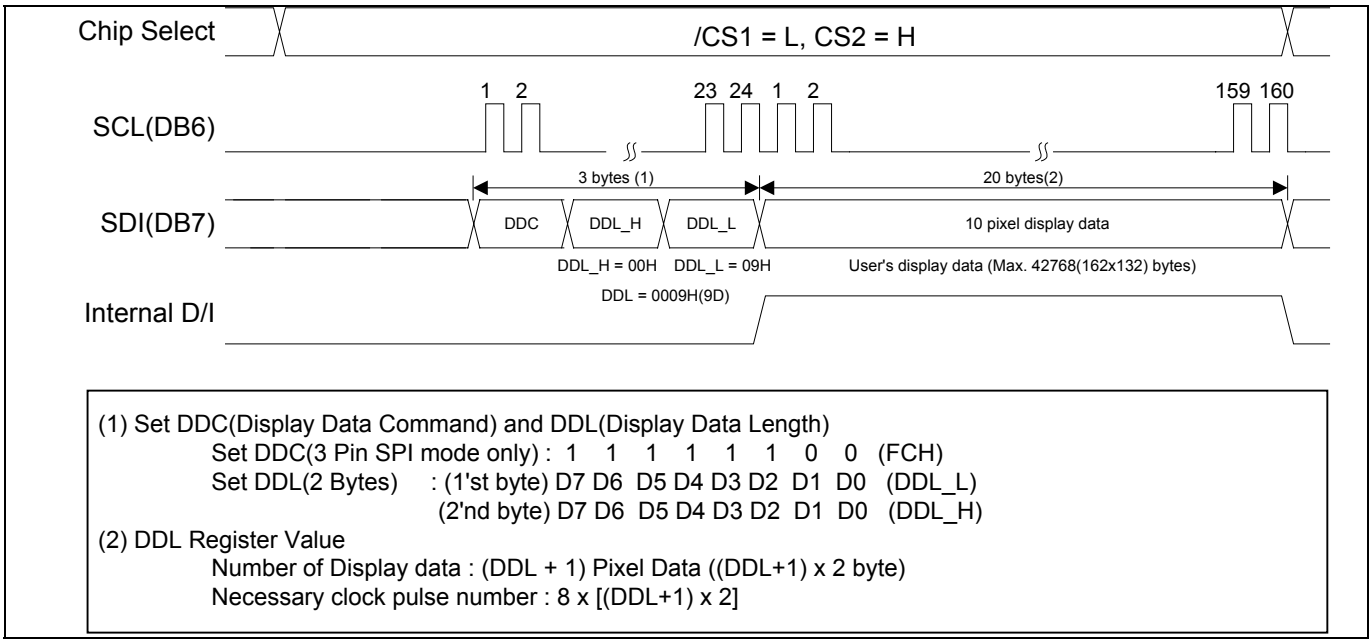


Figure 8. 3-Pin SPI Timing (D/I is not used)

4-Pin Serial Interface (PS="L" & MPU[1]="H")

In 4-pin SPI interface mode, D/I pin is used for indicating whether serial data input is display or instruction data. Data is display data when D/I is high and instruction data when D/I is low.
Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock.

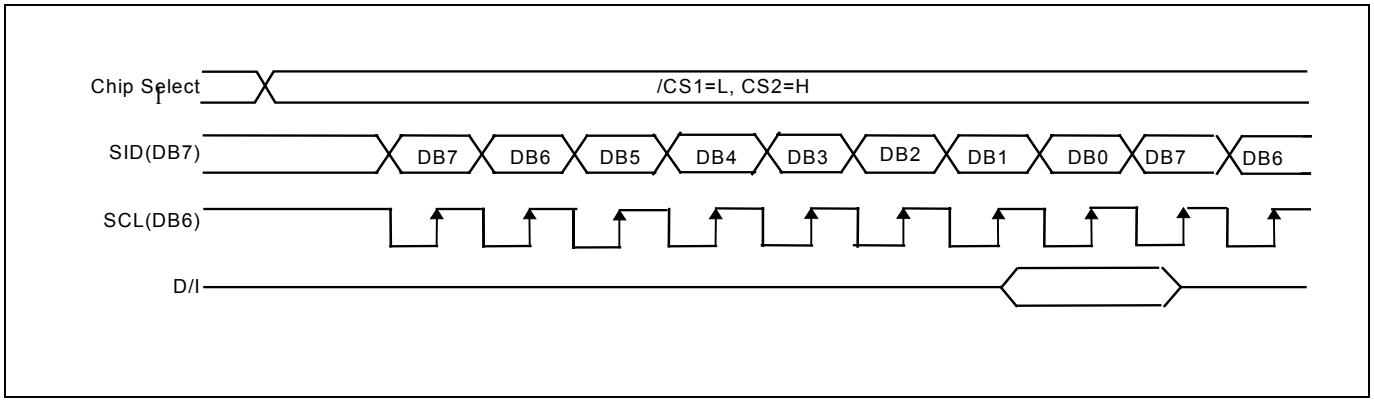


Figure 9. 4-Pin Serial Interface Timing

DISPLAY DATA RAM

The on-chip display data RAM of S6B33B2 is a static RAM that is stored the data for the display. It is a 2,304 x 176 structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

DDRAM Address Area Selection

A part of DDRAM address area of S6B33B2 can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.

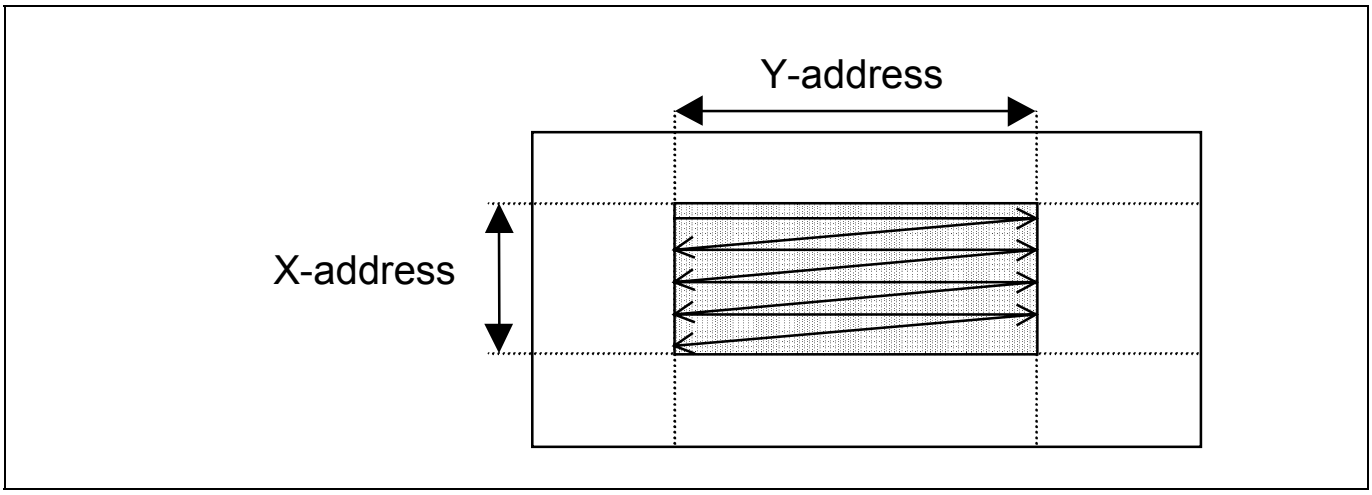


Figure 10. DDRAM Address Area

Table 13. X address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	0	0	0	1
P1	X start address set(Initial Status = 00H)							
P2	X end address set(Initial Status = A1H)							

Table 14. Y address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	1	0	0	0	1
P1	Y start address set (Initial status = 00H)							
P2	Y end address set (Initial status =83H)							

RAM Addressing Count up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

Y address count mode (Y address = 00h to 83h, X address = 00h to A1h)

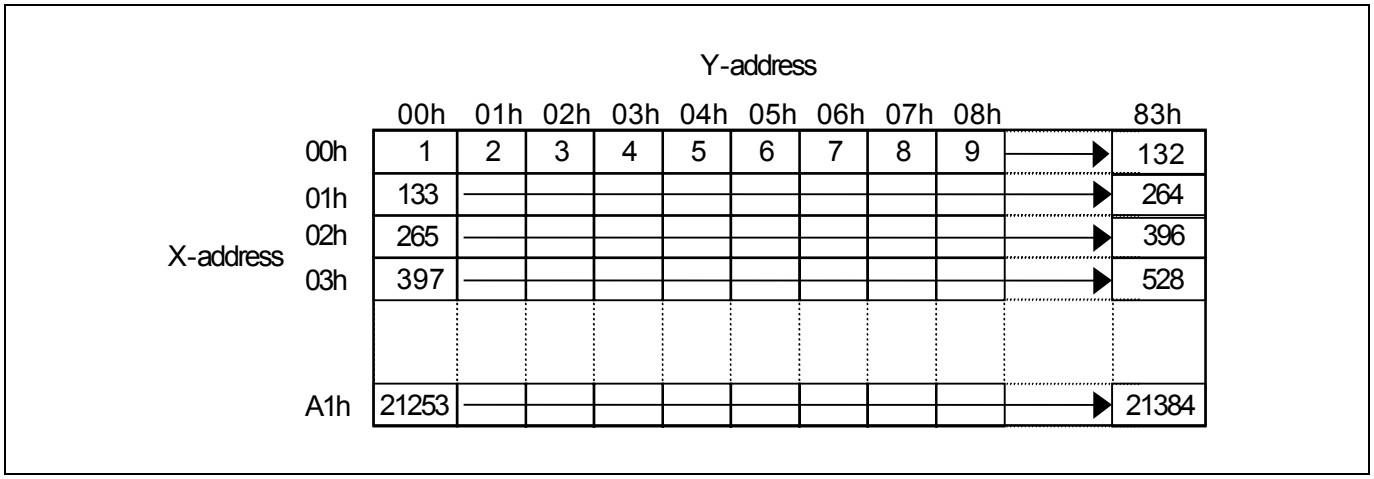


Figure 11. Y address count mode

X address count mode (Y address =00h to 83h, X address = 00h to A1h)

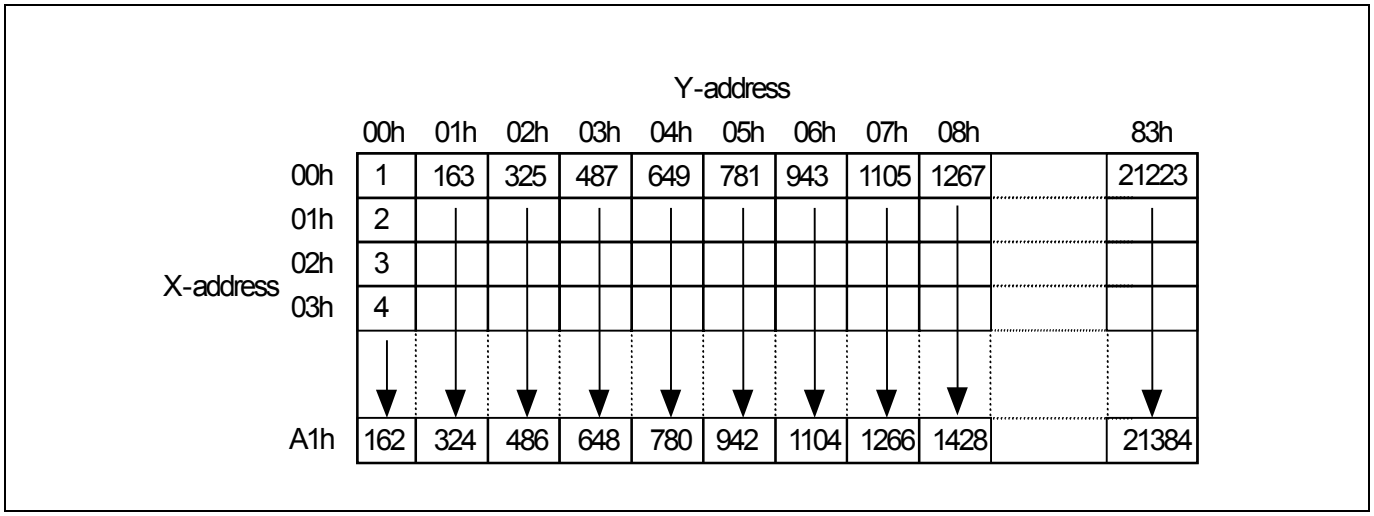


Figure 12. X address count mode

XA Address	YA Address																
	00H	01H	02H	03H	04H	05H	06H	07H	08H	- - - - - - -	7DH	7EH	7FH	80H	81H	82H	83H
00H										- - - - - - -							
01H										- - - - - - -							
02H										- - - - - - -							
03H										- - - - - - -							
04H										- - - - - - -							
05H										- - - - - - -							
06H										- - - - - - -							
07H										- - - - - - -							
08H										- - - - - - -							
09H										- - - - - - -							
0AH										- - - - - - -							
0BH										- - - - - - -							
0CH										- - - - - - -							
0DH										- - - - - - -							
0EH										- - - - - - -							
0FH										- - - - - - -							
⋮										⋮							
B2H										- - - - - - -							
B3H										- - - - - - -							
B4H										- - - - - - -							
B5H										- - - - - - -							
B6H										- - - - - - -							
B7H										- - - - - - -							
B8H										- - - - - - -							
B9H										- - - - - - -							
BAH										- - - - - - -							
BBH										- - - - - - -							
BCH										- - - - - - -							
BDH										- - - - - - -							
BEH										- - - - - - -							
BFH										- - - - - - -							
A0H										- - - - - - -							
A1H										- - - - - - -							

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Red					Green						Blue				

Figure 13. Display Data RAM Map

Partial Display Mode

The S6B33B2 realizes the partial display function with low duty driving for saving power consumption and showing the various display duties. It is set as display start/end line number.

Area Scroll Function

The S6B33B2 realizes the specific area scroll function. (1/162 duty case).

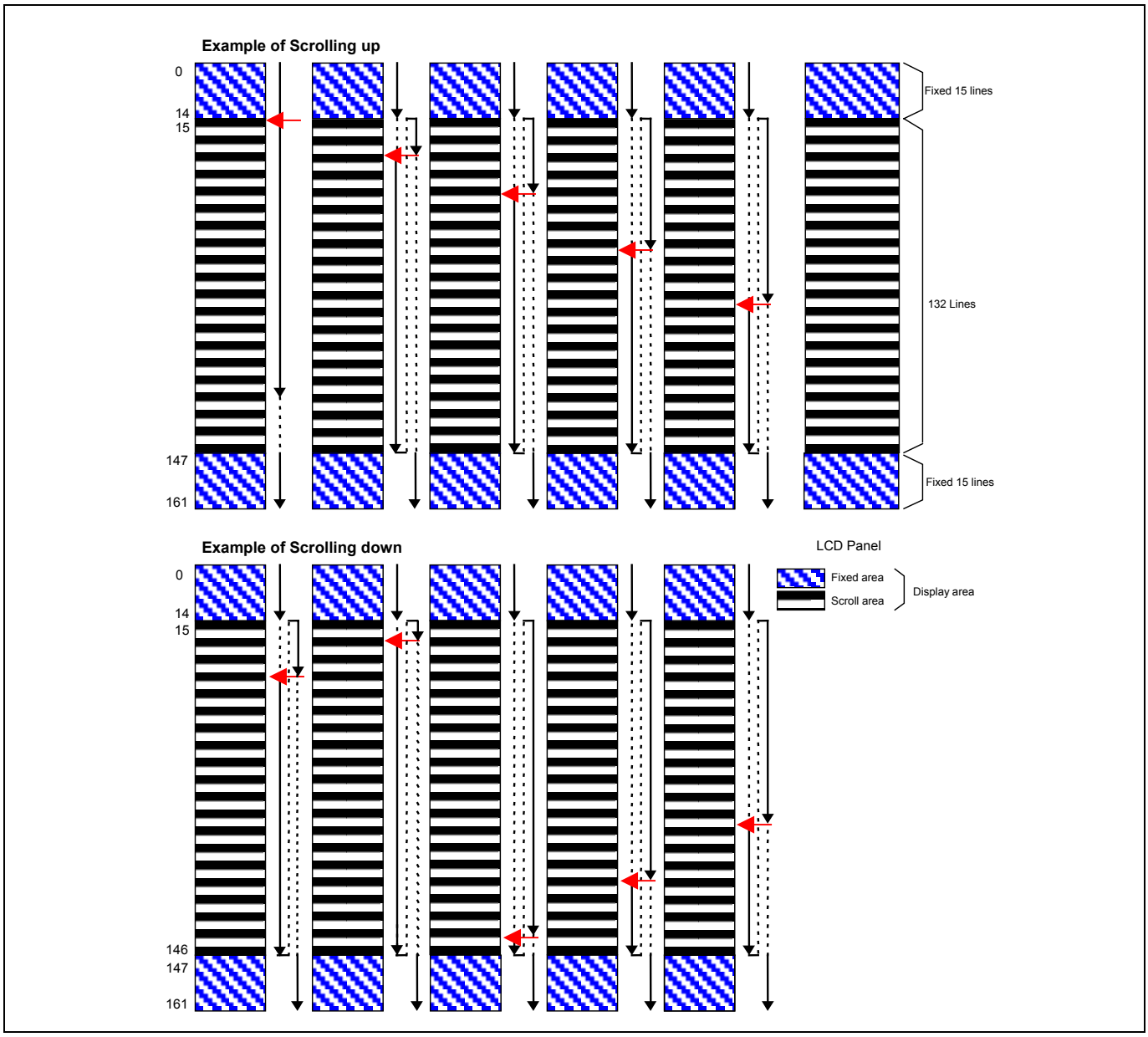


Figure 14. Area scroll examples (duty = 1/162, center scroll mode)

Display Direction

SDIR

The SDIR flag of Driver Output Mode Set instruction selects the direction of segment display.

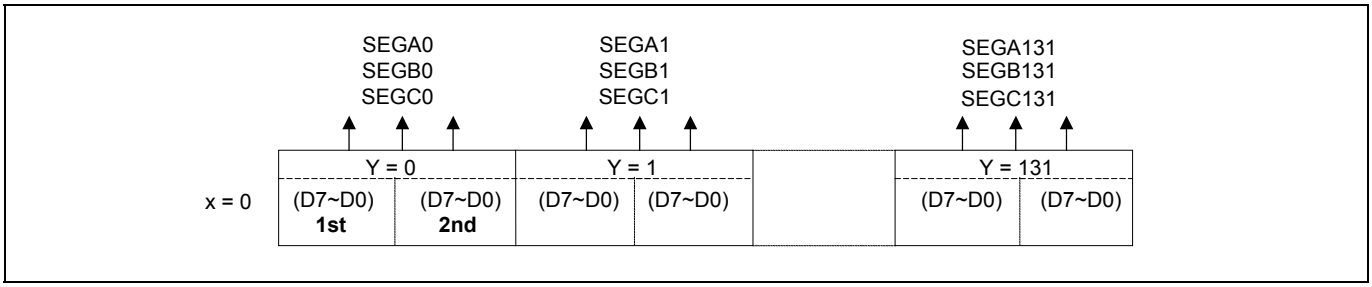


Figure 15. 8-bit data bus mode when SDIR = L

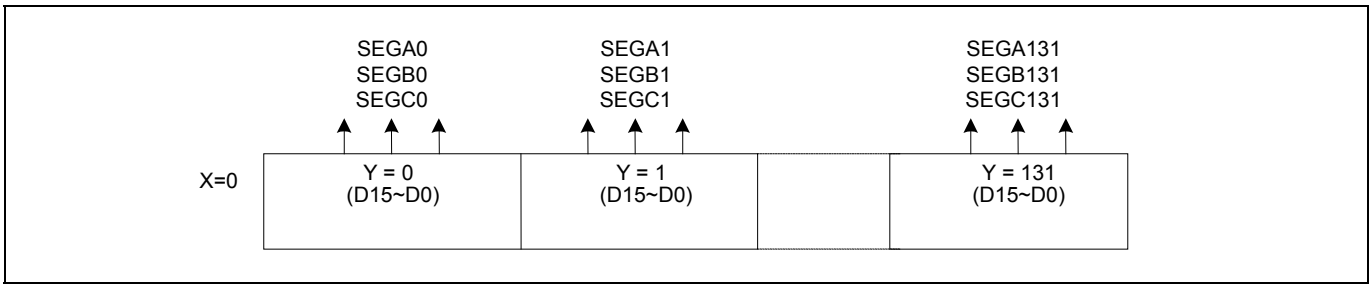


Figure 16. 16-bit data bus mode when SDIR = L

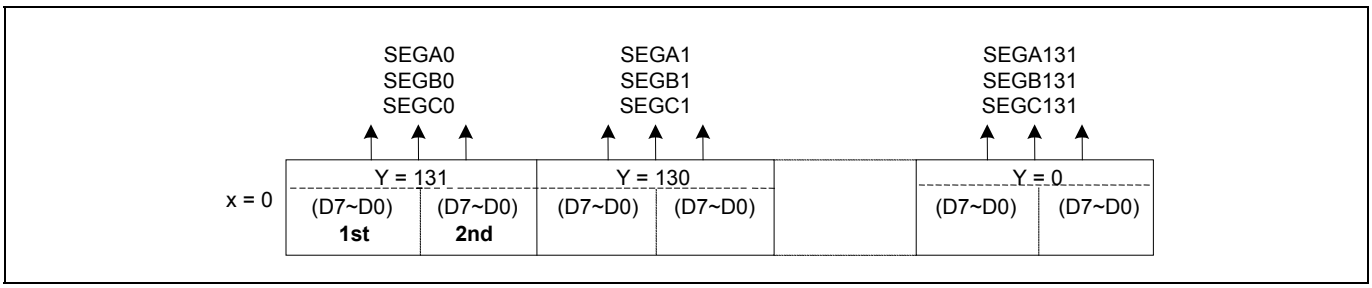


Figure 17. 8-bit data bus mode when SDIR = H

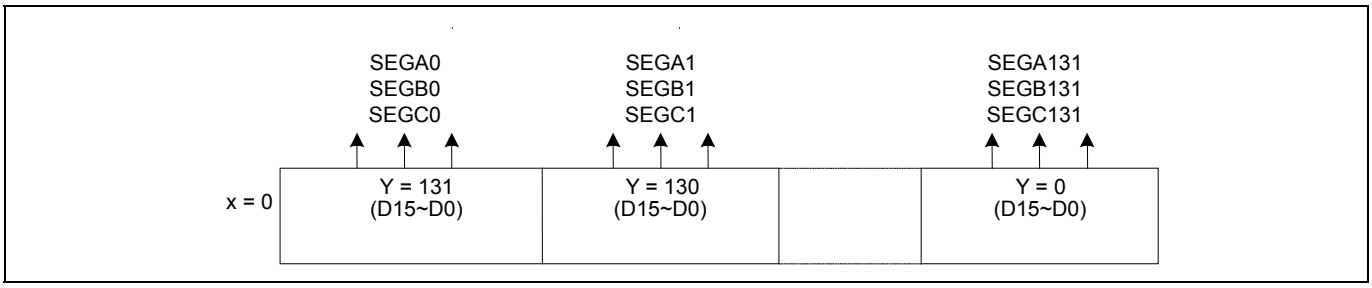
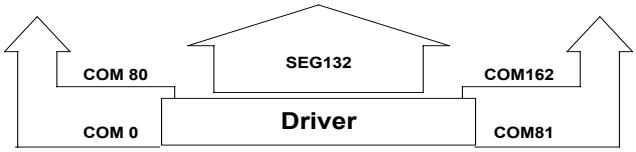


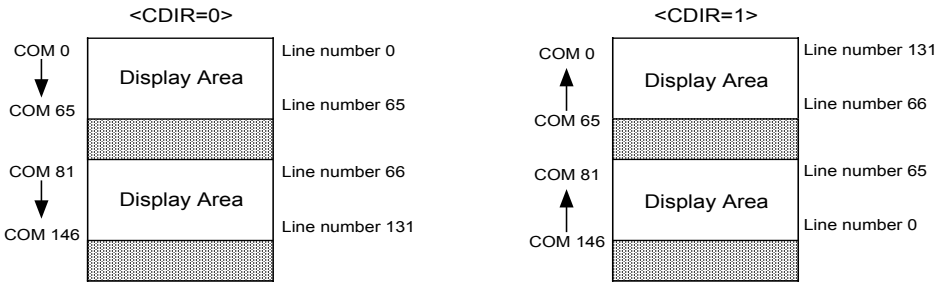
Figure 18. 16-bit data bus mode when SDIR = H

CDIR

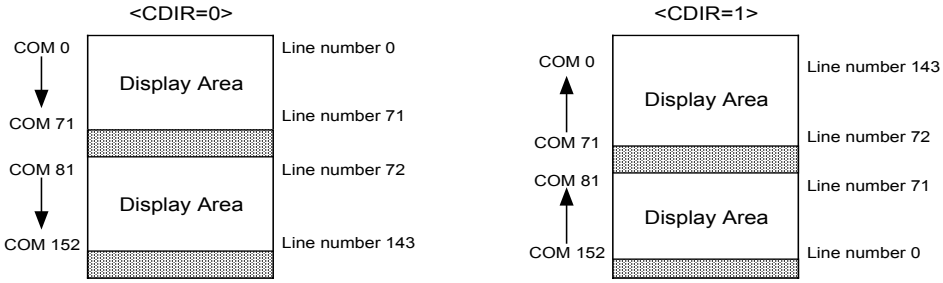
The direction of common scanning is selected by CDIR pin.



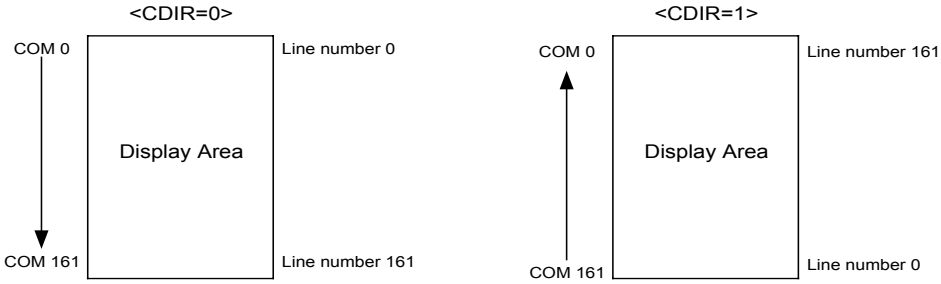
132 Display Lines (DLN=00)



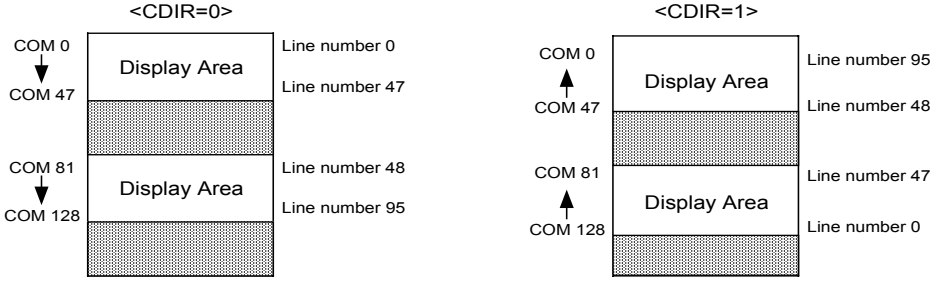
144 Display Lines (DLN=01)



162 Display Lines (DLN=10)



96 Display Lines (DLN=11)



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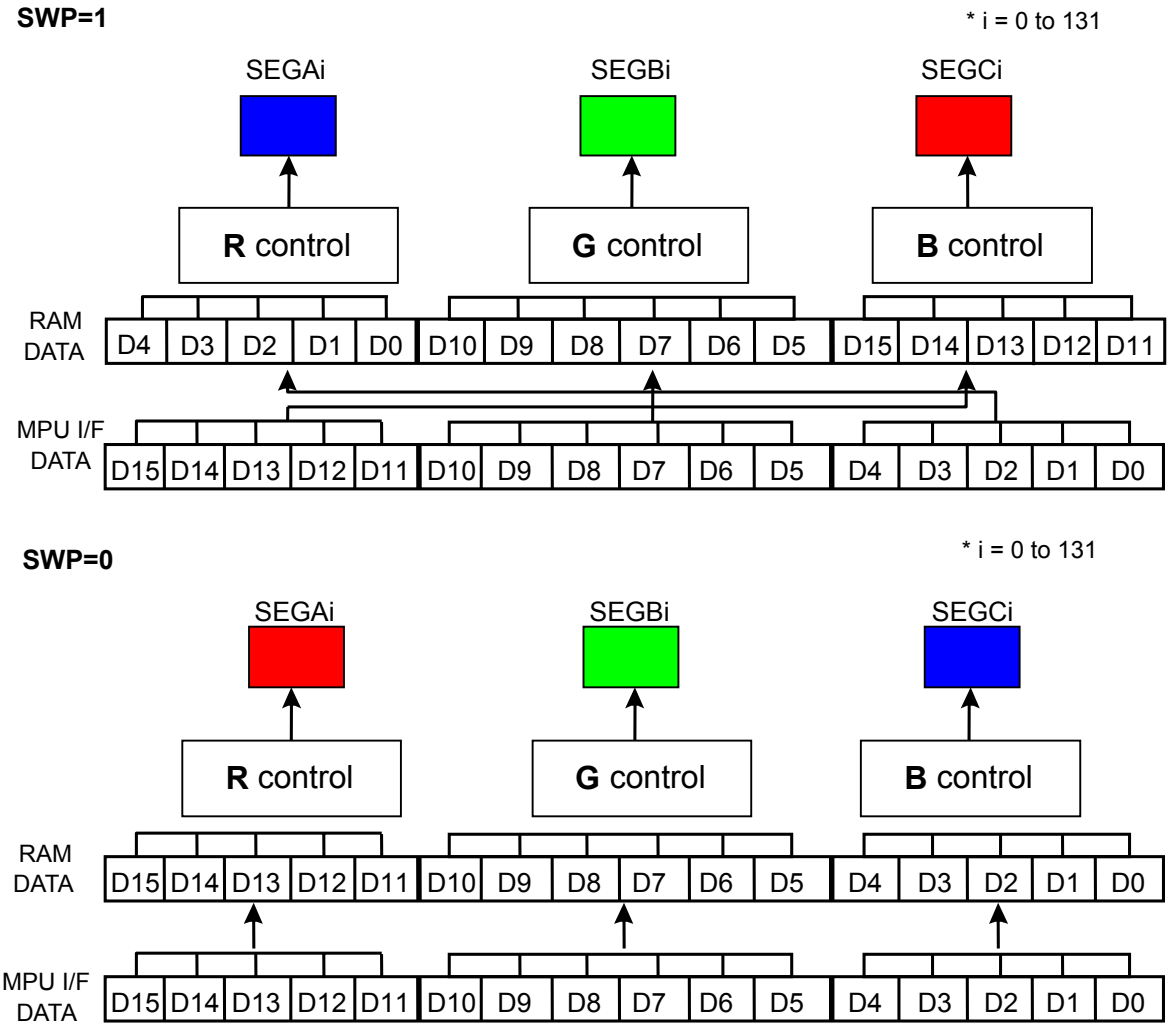
SWP

The SWP flag of Driver Output Mode Set instruction selects the swapping of segment display.

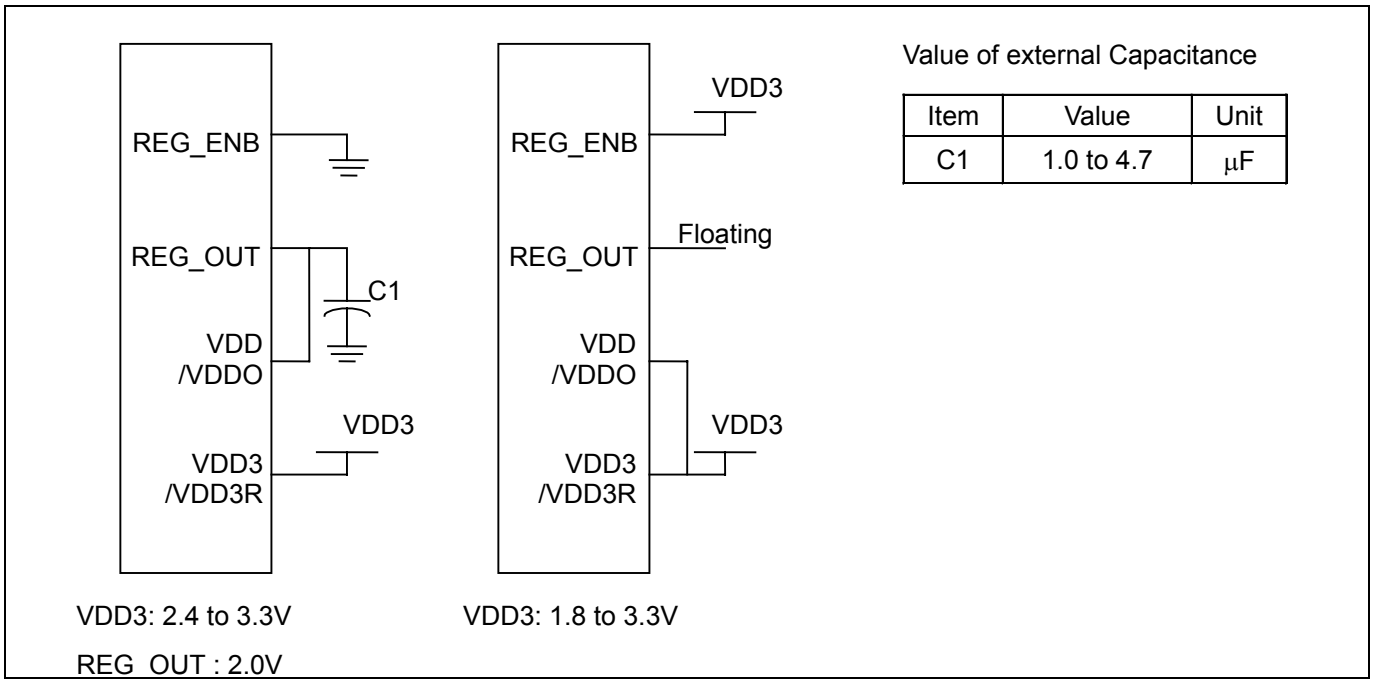


	SEGAi	SEGBi	SEGCi	
SWP = 0	RED	GREEN	BLUE	Color
	D15 ~ D11	D10~ D5	D4 ~ D0	Assigned Bit
SWP = 1	BLUE	GREEN	RED	Color
	D4~ D0	D10 ~ D5	D15 ~ D11	Assigned Bit

Figure 19. The relationship between SEG outputs and RGB color

On-Chip Regulator Configuration

The output voltage of regulator circuit(REG_OUT) is ranging from 1.8V to 2.2V and nominal value is 2.0V.



Value of external Capacitance

Item	Value	Unit
C1	1.0 to 4.7	μF

Figure 20. Regulator Application

Oscillator Circuit

When internal oscillator is used(EXT=0), the selection of oscillator resistor is determined by display mode.

- Normal display mode/ Partial display mode 0 : resistor1 between OSC1 and OSC2
- Partial display mode 1 : resistor2 between OSC3 and OSC4

When external clock is used (EXT=1), clock frequency should be adjusted to display mode that is selected.

Example of external oscillator application

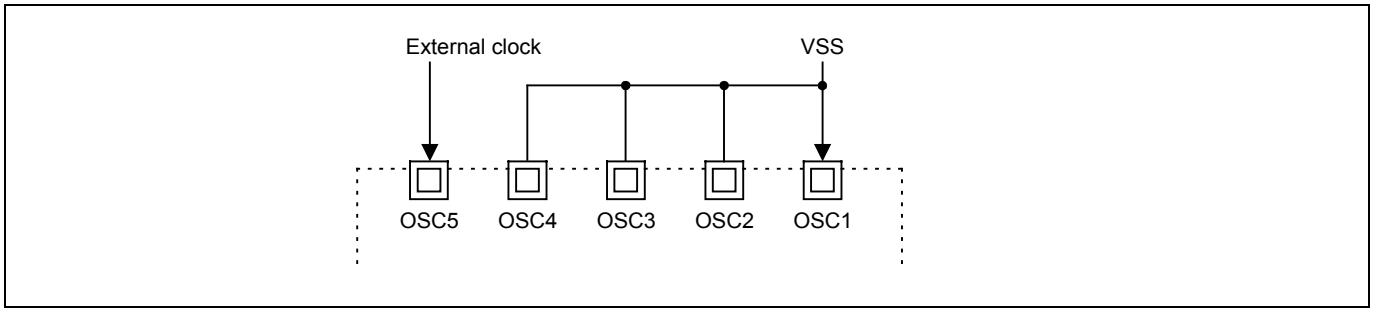
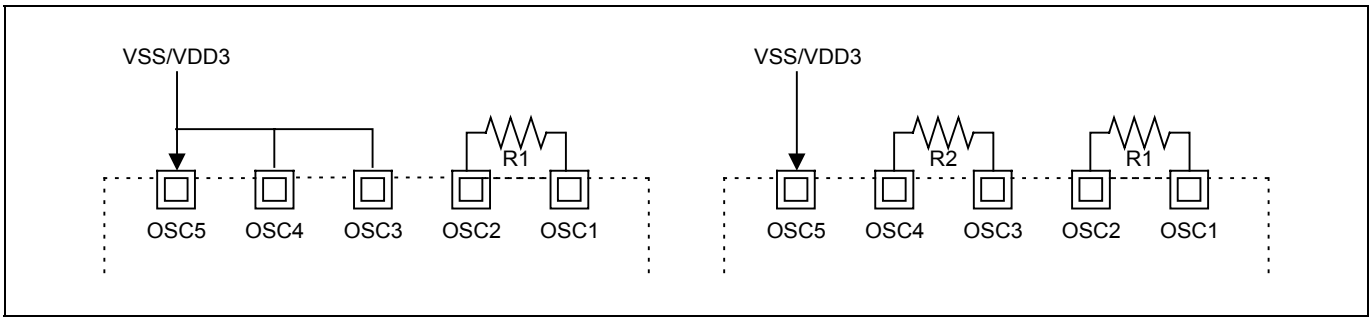


Figure 21. External oscillator application

Example of internal oscillator application

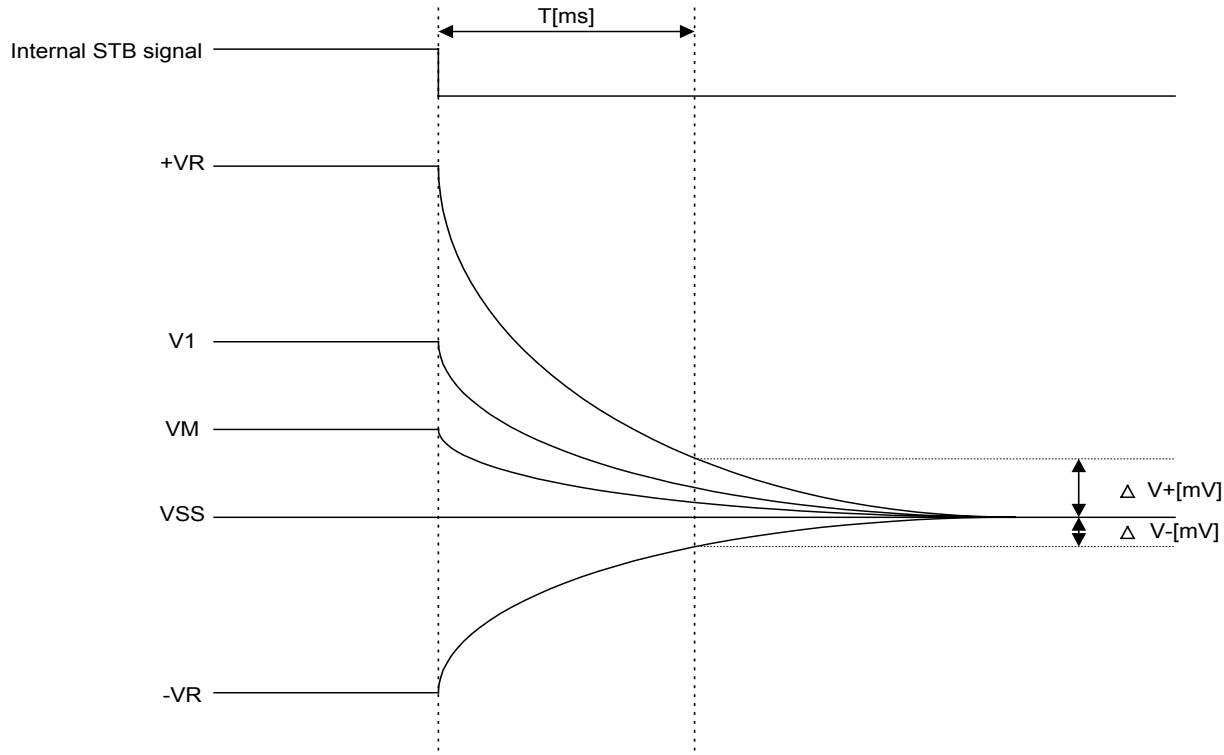


When partial display mode 1 is not used. When partial display mode 1 is used.

Figure 22. Internal oscillator application

Discharge Circuit

Driving voltage level discharge time at standby ON.



The relation between voltage level and discharge time from when “Standby ON” command is inputted.

LEVEL	CONDITION	T[ms]	ΔV+,ΔV-[mV]
+VR,V1,VM,-VR	+VR=12.0V, V1=3.0V, VM=1.5V, -VR=-9.0V at T=0	100	< 50
		300	< 20

INSTRUCTION DESCRIPTION

Table 15. Instruction Table

Instruction Name	D/I	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.	Parameter
Non Operation	0	0	1	*	0	0	0	0	0	0	0	0	00	
Oscillation Mode Set	0	0	1	*	0	0	0	0	0	0	1	0	02	1Byte
Driver Output Mode Set	0	0	1	*	0	0	0	1	0	0	0	0	10	1Byte
DC-DC Select	0	0	1	*	0	0	1	0	0	0	0	0	20	1Byte
Bias Set	0	0	1	*	0	0	1	0	0	0	1	0	22	1Byte
DCDC Clock Division Set	0	0	1	*	0	0	1	0	0	1	0	0	24	1Byte
DCDC and AMP ON/OFF set	0	0	1	*	0	0	1	0	0	1	1	0	26	1Byte
Temperature Compensation Set	0	0	1	*	0	0	1	0	1	0	0	0	28	1Byte
Contrast Control(1)	0	0	1	*	0	0	1	0	1	0	1	0	2A	1Byte
Contrast Control(2)	0	0	1	*	0	0	1	0	1	0	1	1	2B	1Byte
Standby Mode OFF	0	0	1	*	0	0	1	0	1	1	0	0	2C	-
Standby Mode ON	0	0	1	*	0	0	1	0	1	1	0	1	2D	-
DDRAM Burst Mode OFF	0	0	1	*	0	0	1	0	1	1	1	0	2E	-
DDRAM Burst Mode ON	0	0	1	*	0	0	1	0	1	1	1	1	2F	-
Addressing Mode Set	0	0	1	*	0	0	1	1	0	0	0	0	30	1Byte
ROW Vector Mode Set	0	0	1	*	0	0	1	1	0	0	1	0	32	1Byte
N-line Inversion Set	0	0	1	*	0	0	1	1	0	1	0	0	34	1Byte
Frame Frequency control	0	0	1	*	0	0	1	1	0	1	1	0	36	1Byte
Entry Mode Set	0	0	1	*	0	1	0	0	0	0	0	0	40	1Byte
X-address Area Set	0	0	1	*	0	1	0	0	0	0	1	0	42	2Byte
Y-address Area Set	0	0	1	*	0	1	0	0	0	0	1	1	43	2Byte
RAM Skip Area Set	0	0	1	*	0	1	0	0	0	1	0	1	45	1Byte
Display OFF	0	0	1	*	0	1	0	1	0	0	0	0	50	-
Display ON	0	0	1	*	0	1	0	1	0	0	0	1	51	-
Specified Display Pattern Set	0	0	1	*	0	1	0	1	0	0	1	1	53	1Byte
Partial Display Mode Set	0	0	1	*	0	1	0	1	0	1	0	1	55	1Byte
Partial Display Start Line Set	0	0	1	*	0	1	0	1	0	1	1	0	56	1Byte
Partial Display End Line Set	0	0	1	*	0	1	0	1	0	1	1	1	57	1Byte
Area Scroll Mode Set	0	0	1	*	0	1	0	1	1	0	0	1	59	4Byte
Scroll Start Line Set	0	0	1	*	0	1	0	1	1	0	1	0	5A	1Byte
Set Display Data Length	X	X	X	*	1	1	1	1	1	1	0	0	FC	1Byte
Display Data Write	1	0	1	Display Data Write									-	-
Display Data Read	1	1	0	Display Data Read									-	-
Status Read	0	1	0	0	Status Data Read								-	-
Test Mode1	0	0	1	*	1	1	1	1	1	1	1	1	FF	1Byte
Test Mode2	0	0	1	*	1	1	1	1	1	1	1	0	FE	1Byte
Test Mode3	0	0	1	*	1	1	1	1	1	1	0	1	FD	1Byte
Test Mode4	0	0	1	*	1	1	1	1	1	0	1	1	FB	1Byte
Test Mode5	0	0	1	*	1	1	1	1	1	0	1	0	FA	1Byte
Test Mode6	0	0	1	*	1	1	1	1	1	0	0	1	F9	1Byte
OTP Mode Off	0	0	1	*	1	1	1	0	1	0	1	0	EA	-
OTP Mode On	0	0	1	*	1	1	1	0	1	0	1	1	EB	-
Offset Volume Set	0	0	1	*	1	1	1	0	1	1	0	1	ED	1Byte
OTP Write Enable	0	0	1	*	1	1	1	0	1	1	1	1	EF	-

*: Don't care

Parameter: The number of parameter bytes that follows instruction data.

Non Operation (00H)

This instruction is Non operation.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	0

Oscillation Mode Set (02H)

Setting internal function mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1	0
			0	0	0	0	0	0	EXT	OSC

EXT: External clock selecting
EXT = 0: Internal clock mode (Initial status)
EXT = 1: External clock mode

OSC: Internal oscillator ON/OFF
OSC = 0: Internal oscillator OFF(Initial status)
OSC = 1: Internal oscillator ON

Driver Output Mode Set(10H)

This instruction sets the display direction.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	0
			0	0	DLN		0	SDIR	SWP	0

DLN: Display Line number selecting

DB5	DB4	Display Duty
0	0	1/132 (Initial status)
0	1	1/144
1	0	1/162
1	1	1/96

SDIR: Segment direction
This bit is for controlling the direction of segment driver.
SDIR = 0 (Initial status)

SWP: Swap segment output SEGAi and SEGCi
This bit is for swapping the output of segment driver.
SWP = 0 (Initial status)

DC-DC Select (20H)

Selects DC-DC step-up of the common driver in normal and partial mode

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	0	0
			0	0	0	0	DC(2)		DC(1)	

DC(1) : 1'st DC-DC booster boosting step select for V1 generation in normal mode and partial mode 0.
DC(2) : 1'st DC-DC booster boosting step select for V1 generation in partial mode 1.

DC(2) : In partial mode 1		
DB3	DB2	DC-DC step up
0	0	X1.0
0	1	X1.5
1	0	X2.0
1	1	X2.0

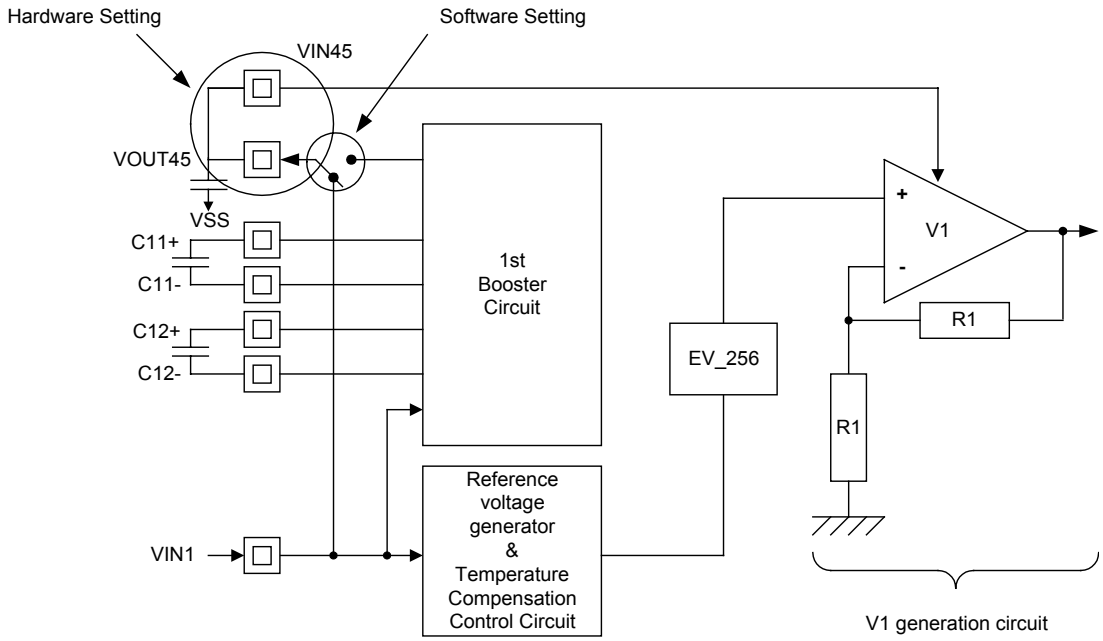
DC(1) : In normal mode, partial mode 0		
DB1	DB0	DC-DC step up
0	0	X1.0
0	1	X1.5
1	0	X2.0
1	1	X2.0

DC-DC Select and power supply for V1 Op-Amp.

Even if VIN45 is connected to VOUT45 or VIN1, a setup by software must be able to be performed. Power supply for V1 Op-Amp. is decided by Hardware setting and Software setting.

The example of usage is shown below.

Figure28. Example : Hardware Setting : VIN45 connected to VOUT45
Software Setting : Power supply for V1 Op.Amp. uses VIN1 (not VOUT45).



Hardware setting : VIN45 connected to (1) VIN1 (when 1'st boosting is not used)
(2) VOUT45 (when 1'st boosting is used)
Software setting : DC-DC Select(20H) - DC(1), DC(2)
Set value "00" Power supply for V1 Op-Amp. uses VIN1 directly.
Set value "01" or "10" Power supply for V1 Op-Amp. uses VOUT45.

Bias Set (22H)

This instruction set up the value of bias in normal mode and in partial mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	1	0
			0	0	Bias(2)		0	0	Bias(1)	

Bias(1): Bias value selecting in normal mode and partial mode0.
Bias(2): Bias value selecting in partial mode1.

Bias (2) : In partial mode 1			
DB5	DB4	Bias(2)	2'nd boosting step
0	0	1/4	x(-3)
0	1	1/5	x(-4)
1	0	1/6	x(-4)
1	1	1/7	x(-5)

Bias (1) : In normal mode, partial mode 0			
DB1	DB0	Bias(1)	2'nd boosting step
0	0	1/4	x(-3)
0	1	1/5	x(-4)
1	0	1/6	x(-4)
1	1	1/7	x(-5)

DCDC Clock Division Set(24H)

This instruction sets the internal booster clock frequency.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	0	0
			0	0	DIV(2)		0	0	DIV(1)	

DIV(1) : DC-DC Charge Pump Division Ratio in Normal Mode Display and Partial Display Mode0
- DIV(1) = 10 (Initial status)

DIV(2) : Division Ratio in Partial Display Mode1
- DIV(2) = 10 (Initial status)

DB5	DB4	DIV(2)
0	0	fPCK = fOSC/4
0	1	fPCK = fOSC/8
1	0	fPCK = fOSC/16
1	1	fPCK = fOSC/32

DB1	DB0	DIV(1)
0	0	fPCK = fOSC/4
0	1	fPCK = fOSC/8
1	0	fPCK = fOSC/16
1	1	fPCK = fOSC/32

Note: fOSC = (ROUNDUP (Duty/3) + dummy) x 4 x 8 x frame frequency

DC/DC and AMP ON/OFF Set (26H)

This instruction set up the DC/DC and Op-amp in common start up setting.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	1	1	0
			0	0	0	0	AMP	DCDC3	DCDC2	DCDC1

AMP: Built-in OP-AMP ON/OFF.
- AMP=0: OP-AMP OFF (Initial status)
- AMP=1: OP-AMP ON

DCDC1: Built-in 1'st Booster ON/OFF
- DCDC1= 0: 1'st Booster OFF (Initial status)
- DCDC1= 1: 1'st Booster ON

DCDC2: Built-in 2'nd Booster ON/OFF
- DCDC2= 0: 2'nd Booster OFF (Initial status)
- DCDC2= 1: 2'nd Booster ON

DCDC3: Built-in 3'rd Booster ON/OFF
- DCDC3= 0: 3'rd Booster OFF (Initial status)
- DCDC3= 1: 3'rd Booster ON

Temperature Compensation Set (28H)

This Instruction sets up the driving voltage slope for temperature compensation.

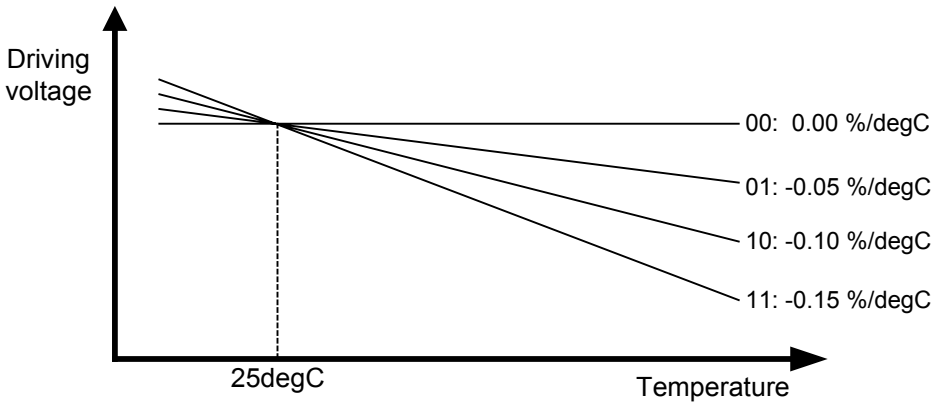
D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	0	0
			0	0	0	0	0	0	TCS	

TCS: Temperature compensation slope set
- TCS = 00 : 0.00%/degC (Initial status)
- TCS = 01 : -0.05%/degC
- TCS = 10 : -0.10%/degC
- TCS = 11 : -0.15%/degC

Product code	Temp. Coefficient	TCS Register Set *
S6B33B2X01-B0CY	0.00%/°C	00
S6B33B2X02-B0CY	-0.05%/°C	01
S6B33B2X03-B0CY	-0.10%/°C	10
S6B33B2X04-B0CY	-0.15%/°C	11

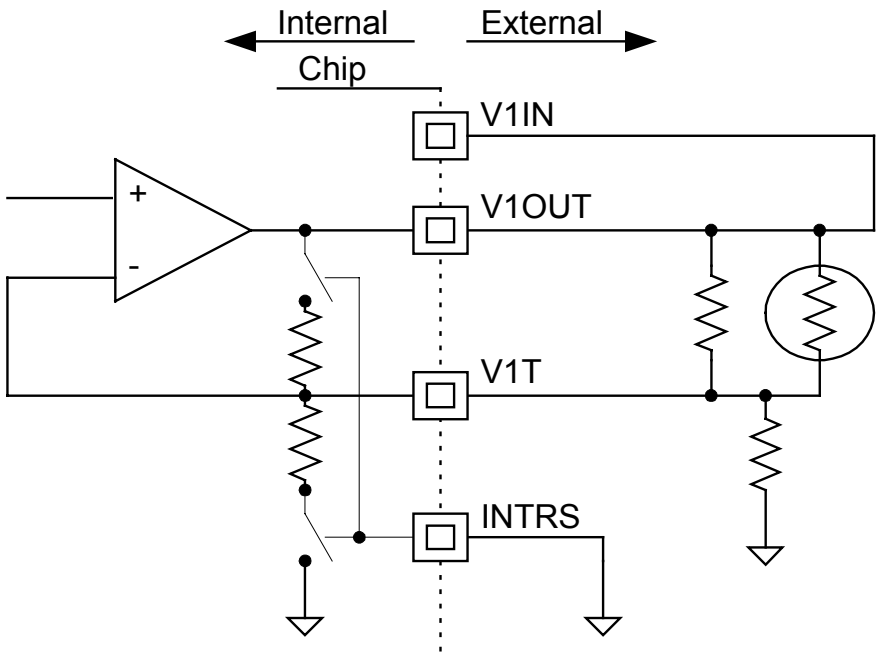
* Note :

In case of S6B33B2X01-B0CY, SEC guarantees only 0.00%/°C, not –0.05 and –0.10, -0.15%/°C.
In case of S6B33B2X02-B0CY, SEC guarantees only -0.05%/°C, not –0.00 and –0.1, -0.15%/°C.
In case of S6B33B2X03-B0CY, SEC guarantees only -0.10%/°C, not –0.00 and –0.05, -0.15%/°C.
In case of S6B33B2X04-B0CY, SEC guarantees only -0.15%/°C, not –0.00 and –0.05, -0.10%/°C.



Temperature Compensation

If external temperature compensation is needed, circuit diagram is described as below.
To use temperature compensation, two resistors and one thermistor are needed.



Contrast Control (1) (2AH)

This instruction updates the contrast control value in normal display mode and partial display mode 0.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	0
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast(1) set value (3bit step case)

Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]	Contrast(1) (HEX)	V1 [V]
00h	2.000	30h	2.376	60h	2.753	90h	3.129	C0h	3.506	F0h	3.882
08h	2.063	38h	2.439	68h	2.816	98h	3.192	C8h	3.569	F8h	3.945
10h	2.125	40h	2.502	70h	2.878	A0h	3.255	D0h	3.631	FFh	4.000
18h	2.188	48h	2.565	78h	2.941	A8h	3.318	D8h	3.694		
20h	2.251	50h	2.627	80h	3.004	B0h	3.380	E0h	3.757		
28h	2.314	58h	2.690	88h	3.067	B8h	3.443	E8h	3.820		

Contrast Control (2) (2BH)

This instruction updates the contrast control value in partial display mode 1.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	1
			Contrast control value (0 to 255)							

The relation between V1 voltage (typ.) and Contrast(2) set value (3 bit step case)

Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]	Contrast(2) (HEX)	V1 [V]
00h	2.000	30h	2.376	60h	2.753	90h	3.129	C0h	3.506	F0h	3.882
08h	2.063	38h	2.439	68h	2.816	98h	3.192	C8h	3.569	F8h	3.945
10h	2.125	40h	2.502	70h	2.878	A0h	3.255	D0h	3.631	FFh	4.000
18h	2.188	48h	2.565	78h	2.941	A8h	3.318	D8h	3.694		
20h	2.251	50h	2.627	80h	3.004	B0h	3.380	E0h	3.757		
28h	2.314	58h	2.690	88h	3.067	B8h	3.443	E8h	3.820		

Note :
S6B33B2 has a hardware protection for "2VR < 20V". It means the limitation of contrast value in each bias.
If 1/6 bias is set, max contrast value is limited to A9h, and if 1/7 bias is set, max contrast value is limited to 6Dh.

Standby Mode OFF (2CH)

This instruction releases the standby mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	0

The internal statuses during standby off are as following:

- All common and segment output: VSS or V1
- Oscillator circuit: On (EXT = 0, OSC=1),OFF (others)
- Displaying clocks (FR, PM, CL): In operation

Function and Pin condition at standby OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
COM outputs	+VR or VM or VSS or -VR
SEG outputs	V1 or VSS

Standby Mode ON (2DH)

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (Initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	1

The internal statuses during standby on are as following:

- All common and segment output: VSS
- Oscillator circuit: OFF
- Displaying clocks (FR, PM, CL) are held.

Function and Pin condition at standby ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	OFF
SEG and COM outputs	VSS

LCD driving power output condition at Standby ON.

level	Condition
+VR	VSS
V1	VSS
VM	VSS
-VR	VSS

DDRAM Burst Mode OFF(2EH) /ON(2FH)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	1	BM

BM: Internal DDRAM Burst Mode Interface Off/On Control
- 0 : Burst Mode Interface Off(Initial Status)
- 1 : Burst Mode Interface On

When BM=0, If MPU[0] is 0 then internal DDRAM I/F bpw(bits per word) is 8 bits.
Else MPU[0] is 1 then internal DDRAM I/F bpw(bits per word) is 16bits.
When BM=1, Regardless of MPU[0] bit, Internal DDRAM I/F bpw(bits per word) is 32 bits.

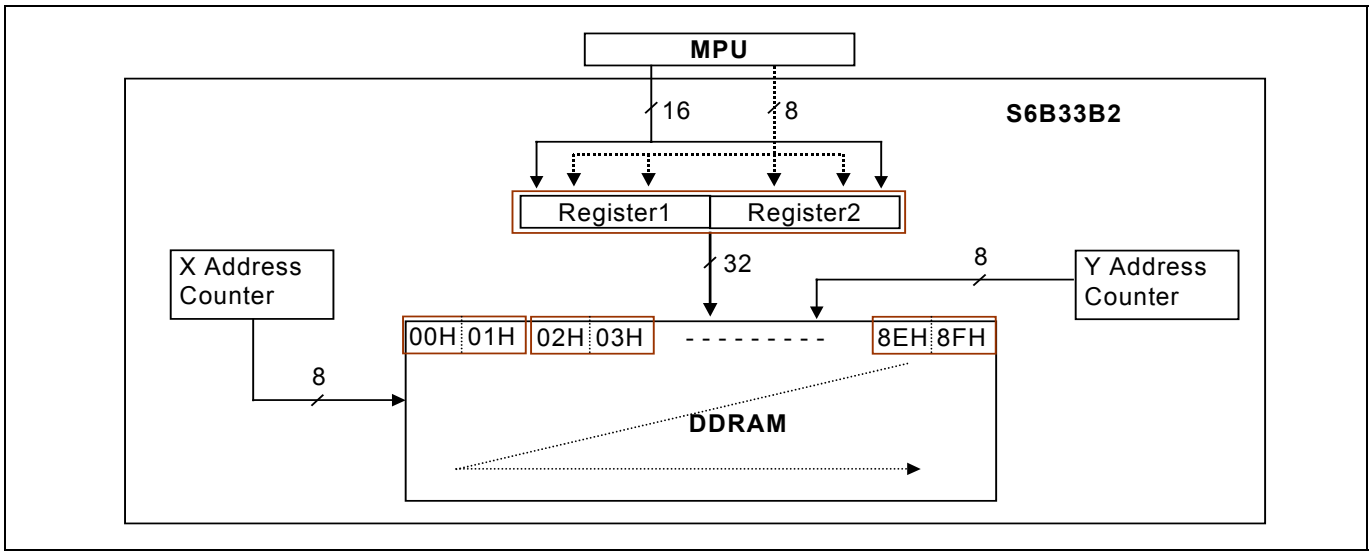


Figure 23. Burst mode writing to DDRAM

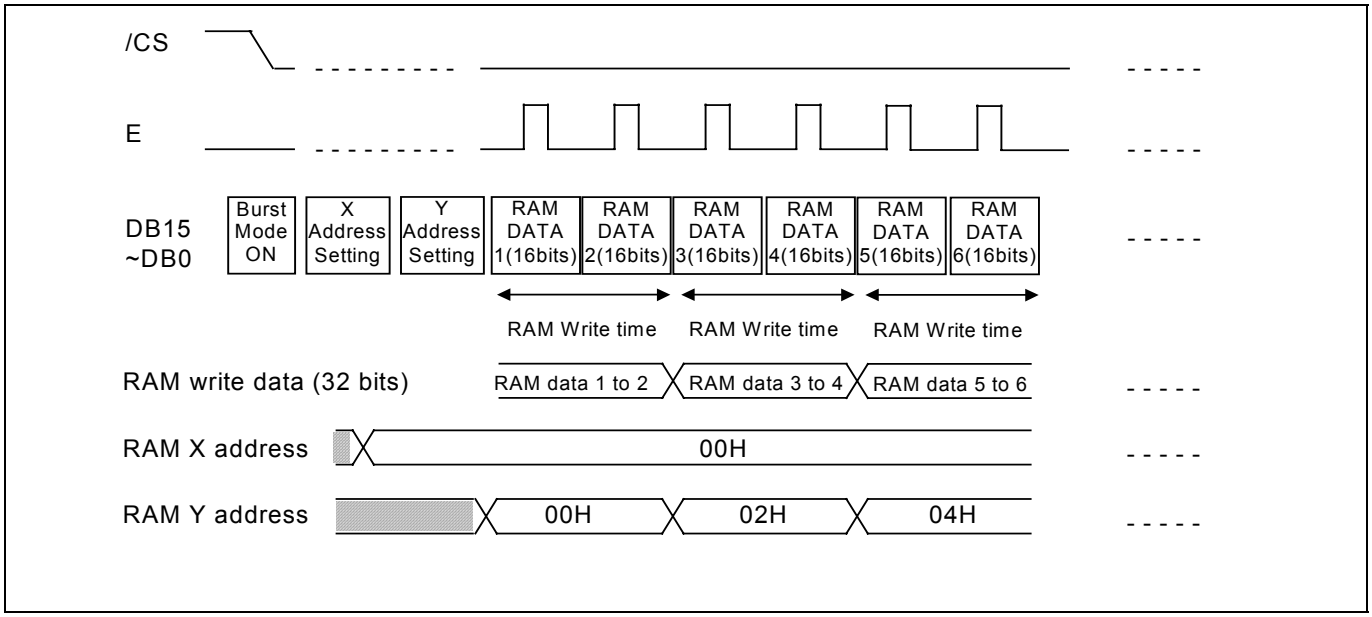


Figure 24. Example of the Burst mode writing to DDRAM (68-mode 16-bit parallel interface)

When DDRAM burst mode is used, note the following.

Notes:

1. Data is written to DDRAM each two words. If only one word data is written to DDRAM, the data will not be written.
   So, the number of word data must be even. It means that Y start address must be even and Y end address must be odd.
2. X address count mode can't be used.
3. Burst mode and normal mode write operation cannot be executed at the same time.
4. In the read data mode and serial interface mode, the burst mode can't be used.
5. In the 256 color mode with 16-bit data bus mode and 4,096 color mode with 8-bit data bus mode, The address is counted as burst mode enable. So these modes are influenced by above notes.

Addressing Mode Set (30H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	0	0
			0	GSM		DSG	SGF	SGP		SGM

GSM: Gray Scale Mode
- 00: 65,536 color mode (Initial status)
- 01: 4,096 color mode* (refer to “Data Format Select (60H/61H)”)
- 10: 256 color mode*
- 11: 256 color mode*

* In the 256 color mode with 16-bit data bus mode and 4,096 color mode with 8-bit data format B, the address is counted as burst mode enable. So, In this case, refer to notes of burst mode at page 39.

DSG: Duty Adjust Setting
- 0: Dummy subgroup is one subgroup
- 1: Dummy subgroup is none (Initial status)

SGF: Sub Group Frame Inversion mode setting
- 0: SG Frame inversion OFF
- 1: SG Frame inversion ON (Initial status)

SGM: Sub Group inversion mode setting
- 0: SG inversion OFF
- 1: SG inversion ON (Initial status)

SGP: Sub Group Phase mode setting
- 00: Same phase in all pixels
- 01: Different phase by 1pixel-unit
- 10: Different phase by 2pixel-unit (Initial status)
- 11: Different phase by 4pixel-unit

Row Vector Mode Set (32H)

Setting ROW function.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	1	0
			0	0	0	0	INC			VEC

INC: Row Vector Increment Mode. This Parameter set up Row vector increment period

DB3	DB2	DB1	Row Vector Increment Period
0	0	0	Every subgroup
0	0	1	Every 2subgroup
0	1	0	Every 4subgroup
0	1	1	Every 8subgroup
1	0	0	Every 16subgroup
1	0	1	Every 16subgroup
1	1	0	Every 16subgroup
1	1	1	Every sub-frame (initial status)

VEC: ROW Vector Sequence Mode
- 0: R1->R2->R3->R4 -> R1… (Initial status)
- 1: R1->R3->R2->R4 -> R1...

N-block inversion Set (34H)

This instruction set up N block inversion for AC driving.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	0	0
			FIM	FIP	0	N-block inversion				

FIM: Forcing Inversion Mode
FIM = 0: Forcing Inversion OFF
FIM = 1: Forcing Inversion ON (Initial status)
FIP: Forcing Inversion Period
FIP = 0: Forcing Inversion Period is one frame (Initial status)
FIP = 1: Forcing Inversion Period is two frame
N-block Inversion: This parameter indicates the basic period of polarity inversion.
The whole period of polarity inversion is decided by FIM, FIP and this parameter.
(Initial status: 01101)

DB7	DB6	DB5	DB4 – DB0	Polarity Inversion Period
x	X	x	0	every frame
0	X	x	1	every 1 block
:	:	:	:	:
0	X	x	31	every 31 blocks
1	0	x	1	every 1 block and every frame
:	:	:	:	:
1	0	x	31	every 31 blocks and every frame
1	1	x	1	every 1 block and every 2 frames
:	:	:	:	:
1	1	x	31	every 31 blocks and every 2 frames

Frame Frequency Control (36H)

This instruction controls the internal frame frequency.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	1	0
			0	0	0	0	0	0	0	LFS

LFS: Low frame frequency set for low power consumption.
LFS = 0 : Low frequency set OFF (Initial status)
LFS = 1 : Low frequency set ON

Note: fFR @(LFS=1) = fFR @(LFS=0) / 2

256 Color Mode Palettes

At 256-color mode, the instruction and parameter below set each Gray Scale level of the Red/Green/Blue. Gray scale level is determined by GS data.

Red Palette (38H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	0	0
			0	0	0	GS data “000” to RAM data				
			0	0	0	GS data “001” to RAM data				
			0	0	0	GS data “010” to RAM data				
			0	0	0	GS data “011” to RAM data				
			0	0	0	GS data “100” to RAM data				
			0	0	0	GS data “101” to RAM data				
			0	0	0	GS data “110” to RAM data				
			0	0	0	GS data “111” to RAM data				

Green Palette (3AH)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	1	0
			0	0	GS data “000” to RAM data					
			0	0	GS data “001” to RAM data					
			0	0	GS data “010” to RAM data					
			0	0	GS data “011” to RAM data					
			0	0	GS data “100” to RAM data					
			0	0	GS data “101” to RAM data					
			0	0	GS data “110” to RAM data					
			0	0	GS data “111” to RAM data					

Blue Palette (3CH)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	1	0	0
			0	0	0	GS data “00” to RAM data				
			0	0	0	GS data “01” to RAM data				
			0	0	0	GS data “10” to RAM data				
			0	0	0	GS data “11” to RAM data				

Initial value for each Palette

Gray Scale Data	Initial Gray Scale Level		
	Red	Green	Blue
000	0	0	0
001	8	16	12
010	12	24	20
011	16	32	31
100	20	40	-
101	24	48	-
110	28	56	-
111	31	63	-

The relationship between Gray Scale level and RAM data for Red/Blue

RAM Data					GS Level	RAM Data					GS Level
DB4	DB3	DB2	DB1	DB0		DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	1	0	0	0	0	16
0	0	0	0	1	1	1	0	0	0	1	17
0	0	0	1	0	2	1	0	0	1	0	18
0	0	0	1	1	3	1	0	0	1	1	19
0	0	1	0	0	4	1	0	1	0	0	20
0	0	1	0	1	5	1	0	1	0	1	21
0	0	1	1	0	6	1	0	1	1	0	22
0	0	1	1	1	7	1	0	1	1	1	23
0	1	0	0	0	8	1	1	0	0	0	24
0	1	0	0	1	9	1	1	0	0	1	25
0	1	0	1	0	10	1	1	0	1	0	26
0	1	0	1	1	11	1	1	0	1	1	27
0	1	1	0	0	12	1	1	1	0	0	28
0	1	1	0	1	13	1	1	1	0	1	29
0	1	1	1	0	14	1	1	1	1	0	30
0	1	1	1	1	15	1	1	1	1	1	31

The relationship between Gray Scale level and Gray Scale data for Green

GS Data						GS Level	GS Data						GS Level
DB5	DB4	DB3	DB2	DB1	DB0		DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	1	0	0	0	0	0	32
0	0	0	0	0	1	1	1	0	0	0	0	1	33
0	0	0	0	1	0	2	1	0	0	0	1	0	34
0	0	0	0	1	1	3	1	0	0	0	1	1	35
0	0	0	1	0	0	4	1	0	0	1	0	0	36
0	0	0	1	0	1	5	1	0	0	1	0	1	37
0	0	0	1	1	0	6	1	0	0	1	1	0	38
0	0	0	1	1	1	7	1	0	0	1	1	1	39
0	0	1	0	0	0	8	1	0	1	0	0	0	40
0	0	1	0	0	1	9	1	0	1	0	0	1	41
0	0	1	0	1	0	10	1	0	1	0	1	0	42
0	0	1	0	1	1	11	1	0	1	0	1	1	43
0	0	1	1	0	0	12	1	0	1	1	0	0	44
0	0	1	1	0	1	13	1	0	1	1	0	1	45
0	0	1	1	1	0	14	1	0	1	1	1	0	46
0	0	1	1	1	1	15	1	0	1	1	1	1	47
0	1	0	0	0	0	16	1	1	0	0	0	0	48
0	1	0	0	0	1	17	1	1	0	0	0	1	49
0	1	0	0	1	0	18	1	1	0	0	1	0	50
0	1	0	0	1	1	19	1	1	0	0	1	1	51
0	1	0	1	0	0	20	1	1	0	1	0	0	52
0	1	0	1	0	1	21	1	1	0	1	0	1	53
0	1	0	1	1	0	22	1	1	0	1	1	0	54
0	1	0	1	1	1	23	1	1	0	1	1	1	55
0	1	1	0	0	0	24	1	1	1	0	0	0	56
0	1	1	0	0	1	25	1	1	1	0	0	1	57
0	1	1	0	1	0	26	1	1	1	0	1	0	58
0	1	1	0	1	1	27	1	1	1	0	1	1	59
0	1	1	1	0	0	28	1	1	1	1	0	0	60
0	1	1	1	0	1	29	1	1	1	1	0	1	61
0	1	1	1	1	0	30	1	1	1	1	1	0	62
0	1	1	1	1	1	31	1	1	1	1	1	1	63

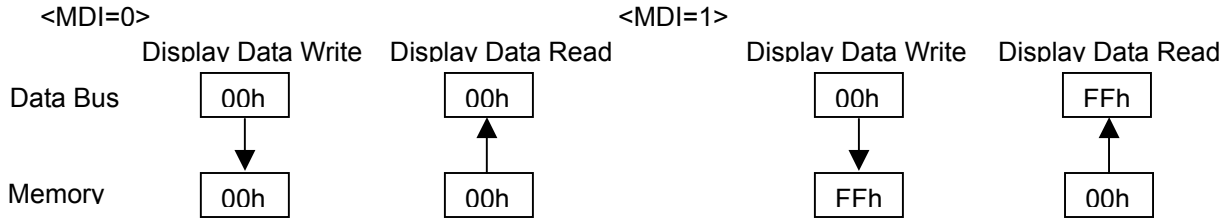
Entry Mode Set (40H)

Setting internal function mode.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0	0
			0	0	0	0	HL	MDI	X/Y	RMW

HL: When GSM is 10 or 11 (256 color mode),
Exchange higher and lower byte in 16-bit data bus mode only for “Display Data Write/Read”
HL = 0: Not exchanged status (Initial status)
HL = 1: Exchanged status

MDI: Memory data inversion setting for low power consumption.
MDI = 0: Memory data inversion OFF (Initial status)
MDI = 1: Memory data inversion ON



X/Y: Memory address counter mode setting
X/Y = 0: Y address counter mode (Initial status)
X/Y = 1: X address counter mode

RMW: Read modify write mode ON/OFF select
RMW = 0: Read modify write OFF (Initial status)
RMW = 1: Read modify write ON. When this mode is on, X(Y) address of on-chip display RAM is not increment in reading display data but in writing display data.

X Address Area Set (42H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	0
			X start address set (Initial Status = 00H)							
			X end address set (Initial Status = A1H)							

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X address count mode (X/Y = “H”), the X address is increased from X start address to X end address. When X address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start address. The X start and X end addresses must be set as a pair and X start address must be less than X end address.

Y Address Area Set (43H)

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	1
			Y start address set (Initial Status = 00H)							
			Y end address set (Initial Status = 83H)							

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (X/Y = “L”), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end address must be set as a pair and Y start address must be less than Y end address.

RAM Skip Area Set (45H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

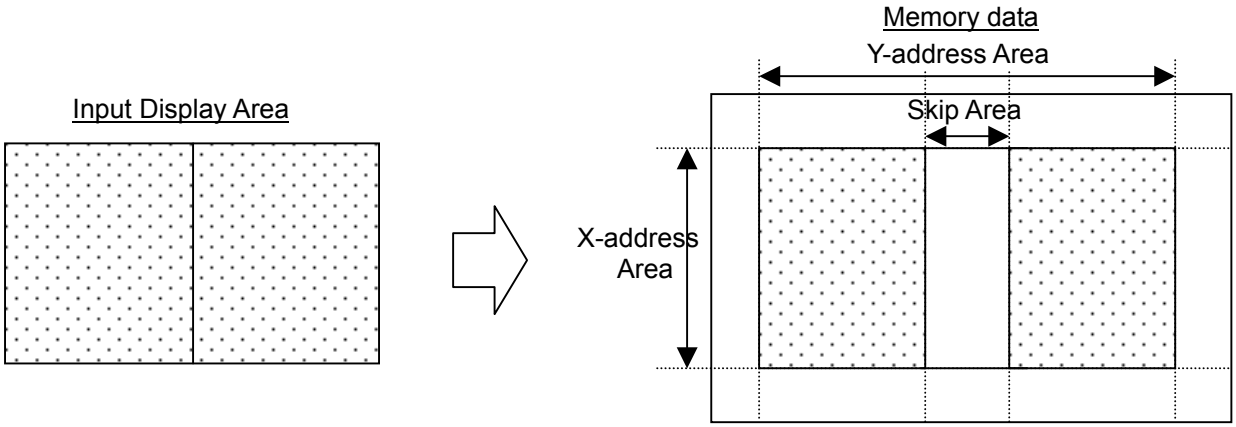
D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	0	1
			0	0	0	0	0	0	RSK	

RSK : RAM Skip function ON/OFF set

- RSK = 00 : No Skip
- RSK = 01 : Y address 40h - 43h skip
- RSK = 10 : Y address 3Ch - 47h skip
- RSK = 11 : Reserved

RAM Skip Area Set

RAM Skip Area Set can skip a part of RAM Y-address area. After setting RAM skip area, Y-address count skip this area and count. In other words, Y address after skip area is changed into Y address which added a part for skip area.



Display OFF (50H)

Turn the display OFF(Initial status).
When display is off, all segment and common output are VSS level.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	0

Function and Pin condition at Display OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
SEG and COM outputs	VSS

Display ON (51H)

Turns the display ON.
In case of being standby mode, this instruction does not work. This instruction is executed after standby mode off.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1

Function and Pin condition at Display ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON(Operate)
COM outputs	+VR or VM or -VR
SEG outputs	V1 or VSS

Specified Display Pattern Set (53H)

This instruction sets the specified display pattern.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	1	1
			0	0	0	0	0	0	SDP	

SDP : Specified Display Pattern set
- SDP = 00 : Normal display
- SDP = 01 : Reverse display : Display data reversing mode setting without the contents of the display RAM
- SDP = 10 : Whole display pattern becomes OFF regardless of the RAM data.
- SDP = 11 : Whole display pattern becomes ON regardless of the RAM data.

Partial Display Mode Set (55H)

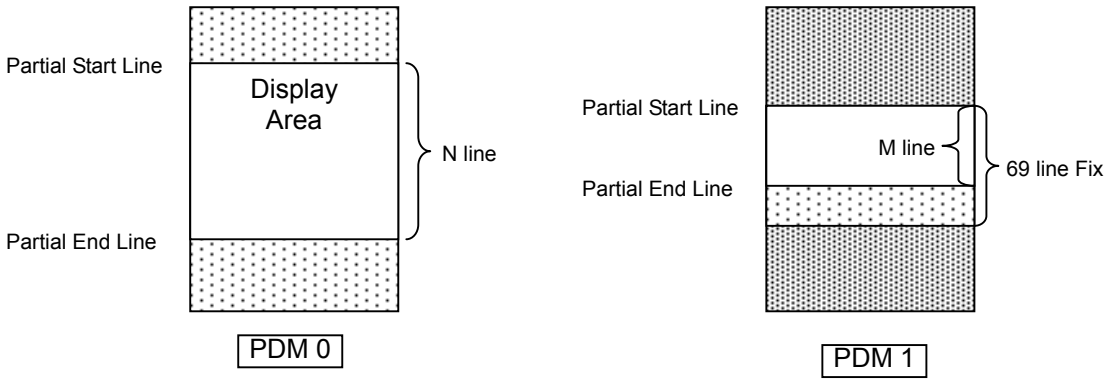
D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	0	1
			0	0	0	0	0	0	PDM	PT

PT: Partial Display ON/OFF
- PT = 0: Partial display OFF = Normal mode (Initial status)
- PT = 1: Partial display ON

PDM: Partial Display mode set
- PDM = 0: Partial mode 0 : Duty ratio is same as Normal display mode(initial status)
- PDM = 1: Partial mode 1 : Duty ratio is changed from Normal display mode
  (DSG = 0 : 69 line fixed(including 1 dummy subgroup),
  DSG = 1 : 66 line fixed(no dummy subgroup))

Applied parameter in PDM0 and PDM1 are summarized as below

PDM	Contrast	Duty	Bias	DC-DC Select	OSC	PCK
0	Contrast control(1)	Normal	Bias(1)	DC(1)	OSC1-OSC2	DIV(1)
1	Contrast control(2)	1/69	Bias(2)	DC(2)	OSC3-OSC4	DIV(2)



Operation in Partial Display Mode 0 (PDM=0)

On scanning except partial display area
- SEG output select V0 or V1 level depend on “FR” value. Refer to Page50.
- All of COM output is fixed VM level.

On scanning partial display area
- It is equal to be in normal mode

Operation in Partial Display Mode 1 (PDM=1)

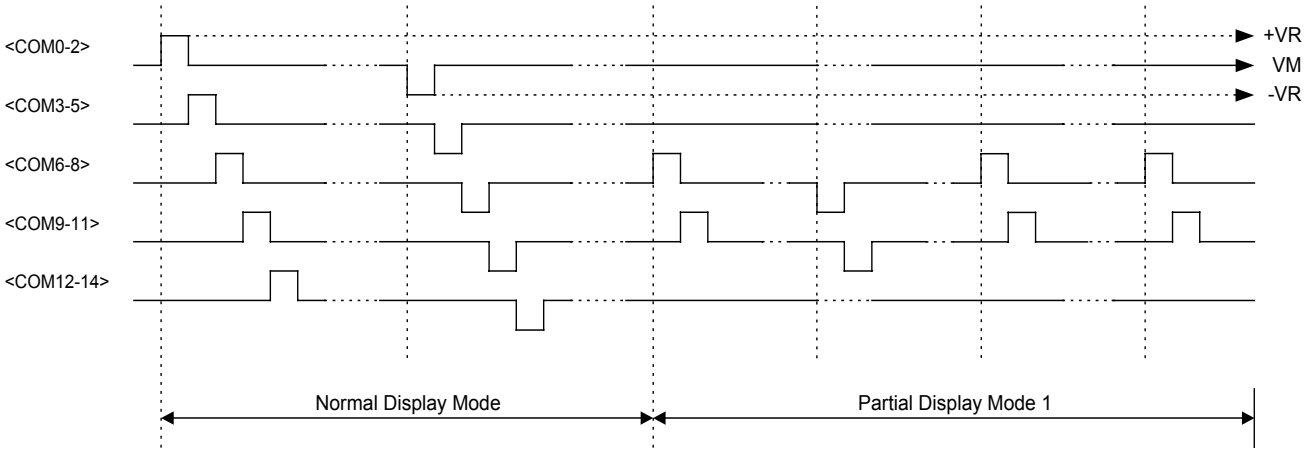
Display area is from partial start line to partial end line.
(COM driver output is fixed VM except display area, only max69 line output COM signal.
On scanning except partial display area
- SEG output select V0 or V1 level depend on “FR” value. Refer to Page50.
- All of COM output is fixed VM level.

On scanning partial display area
- It is equal to be in normal mode

Partial Display Mode0

Item	Partial Display Area	Out of Partial Display Area
Duty	Same as normal display mode	
Bias	Same as normal display mode (Bias(1) setting)	
Contrast	Same as normal display mode (Contrast(1) setting)	
Oscillator	Same as normal display mode (OSC1 – OSC2)	
SEG Output level	Same as normal mode (V1,V0)	Depends on Internal “FR” signal See page 50
COM Output level	Same as normal mode (+VR,VM,-VR)	VM fixed

In case of COM 6 to COM11 Partial display



Partial display mode1

Item	Partial Display Area	Out of Partial Display Area	Out of Display Area
Duty	1/69duty		
Bias	Bias(2) setting		
Contrast	Contrast(2) setting		
Oscillator	(OSC3 – OSC4) setting value		
SEG Output level	Same as normal mode (V1,V0)	Depends on “FR” signal See page 50	-
COM Output level	Same as normal mode (+VR, VM, -VR)	VM fixed	VM fixed

Partial Display Start Line Set (56H), Partial Display End Line Set(57H)

These 2 instructions set the partial display area and it is possible to display a part.

Partial Display Start Line Set (56H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	0
			Partial start line							

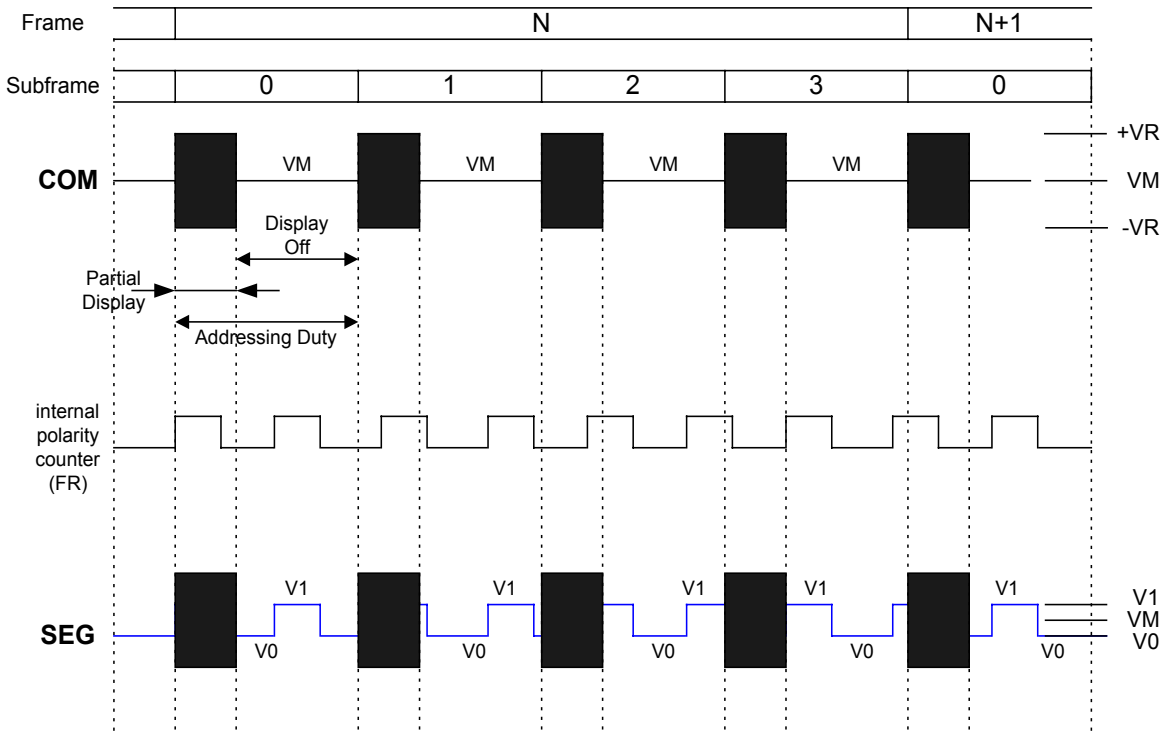
Partial Display End Line Set (57H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	1
			Partial end line							

COM 0	line 0
COM 1	line 1
COM 2	line 2
COM 3	line 3
	:
	:
	:
COM 158	line 158
COM 159	line 159
COM 160	line 160
COM 161	line 161

Parameter set appoints display line number. At PDM 0, Parameter Size is able to be in a number of Display lines. But that is not able to be over max 69 line at PDM 1. Partial end line must set bigger number than Partial start line.

Example of Segment Voltage in non-display area



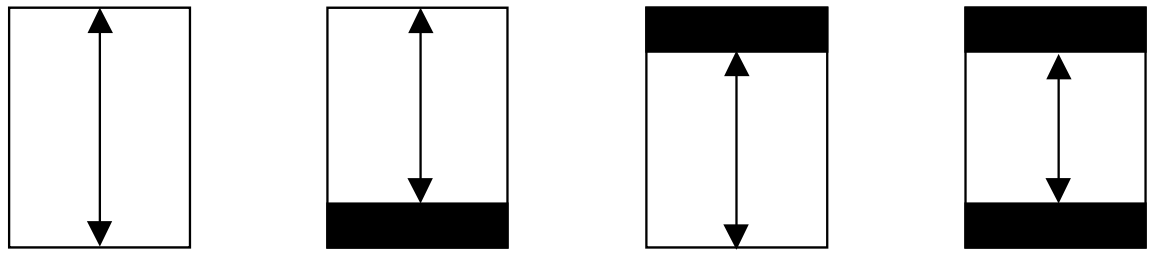
Area scroll Set (59H)

This instruction sets up area scroll field (start line, end line, Lower fixed line number), and it is possible to make screen to display as partial scroll field.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	0	1
			0	0	0	0	0	0	SCM	
			Scroll area start line							
			Scroll area end line							
			Lower fixed number							

SCM: Scroll mode setting

DB1	DB0	Mode
0	0	Entire display(Initial status)
0	1	Upper scroll display
1	0	Lower scroll display
1	1	Center scroll display



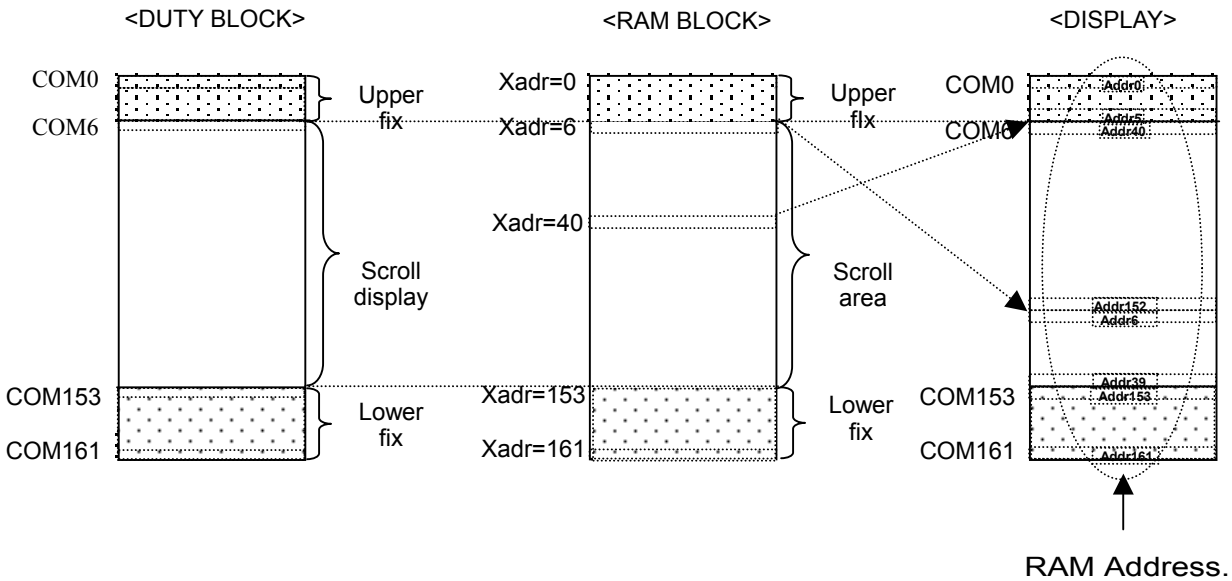
Scroll Start Line Set (5AH)

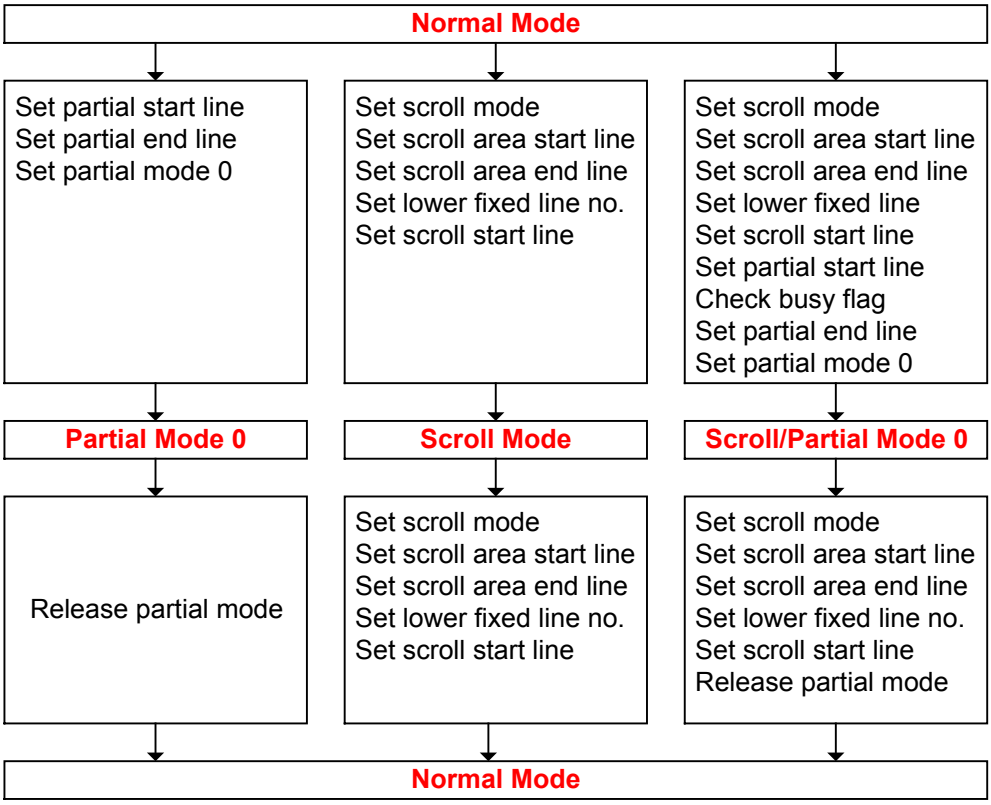
This instruction and parameter set up scroll start line. On this instruction, scroll start line becomes the first of area scroll field. Scroll operation is occurred every issue of this instruction.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	1	0
			Scroll start line							

<Example>

-DLN : 2'b10 (1/162 duty)
-SCM : 2'b11 (Center display mode)
-Scroll area start line : 6
-Scroll area end line : 152
-Lower fixed number : 9
-Scroll start line : 40





Data Format Select (60H/61H)

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	0	0	0	0	DFS

DFS: 4,096 Color Mode Data Format Select
- 0 : 4,096 Color Data Format A (Initial Status)
  - 8 bit mode :
    - DB[7:0] : XXXXRRRR (1'st write)
    - DB[7:0] : GGGGBBBB(2'nd write)
  - 16 bit mode :
    - DB[15:0] :XXXXRRRRGGGGBBBB (12 bit)
- 1 : 4,096 Color Data Format B
  - 8 bit mode :
    - DB[7:0] : RRRRGGGG(1'st write)
    - DB[7:0] : BBBBRRRR (2'nd write)
    - DB[7:0] : GGGGBBBB(3'rd write)
  - 16 bit mode :
    - DB[15:0] :RRRRGGGGBBBBXXXX (12 bit)

Display Data Write/Read

D/I	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Display RAM write in data								
1	1	0	Display RAM read out data								

GSM = 00(65,536 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
2'nd cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3
2'nd cycle	G2	G1	G0	B4	B3	B2	B1	B0
3'rd cycle	R4	R3	R2	R1	R0	G5	G4	G3
4'th cycle	G2	G1	G0	B4	B3	B2	B1	B0

GSM = 01(4,096 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2'nd cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0
2'nd cycle	G3	G2	G1	G0	B3	B2	B1	B0
3'rd cycle	X	X	X	X	R3	R2	R1	R0
4'th cycle	G3	G2	G1	G0	B3	B2	B1	B0

GSM = 10 or 11 (256 Color Mode)

(1) 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R2	R1	R0	G2	G1	G0	B1	B0	R2	R1	R0	G2	G1	G0	B1	B0
2'nd cycle	R2	R1	R0	G2	G1	G0	B1	B0	R2	R1	R0	G2	G1	G0	B1	B0

(2) 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R2	R1	R0	G2	G1	G0	B1	B0
2'nd cycle	R2	R1	R0	G2	G1	G0	B1	B0
3'rd cycle	R2	R1	R0	G2	G1	G0	B1	B0
4'th cycle	R2	R1	R0	G2	G1	G0	B1	B0

Status Read

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	BSY	X/Y	OPRT	PDM	PT	STB	REV	DP

This instruction indicates the internal status of the S6B33B2.

DP: (0 : Display OFF Status, 1 : Display ON Status)
REV: (0 : Display Image Non-Reversing, 1 : Display Image Reversing)
STB: (0 : Standby Mode OFF Status, 1 : Standby Mode ON Status)
PT: (0 : Partial Display Mode OFF Status, 1 : Partial Display Mode ON Status)
PDM: (0 : Partial Display Mode 0, 1 : Partial Display Mode 1)
OPRT: (0: OTP mode non-protection status, 1: OTP mode protection status)
X/Y: (0 : Y-address Count Mode, 1 : X-address Count Mode)
BSY: (0 : No Busy, 1 : Busy)

Set Display Data Length (FCH)

This Instruction is only used in 3-pin SPI MPU interface mode(PS="L", MPU[1]="L"). It consists of two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second and third bytes will be number of data bytes will be write. When DI is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted.
The next byte after the display data string is handled as command data.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	1	0	0
			Number of display data upper 8bits (DDL_H)							
			Number of display data lower 8bits (DDL_L)							

OTP Mode On (EBH)

This command is used to turn OTP mode on. (Initial status)

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	0	1	0

OTP Mode Off (EAH)

This command is used to turn OTP mode off

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	0	1	1

Offset Volume Set (EDH)

This command is used to set offset value x (-32 to +31) to electronic volume by 2s complement.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	0	1
0	0	0	OPRT	P15	P14	P13	P12	P11	P10

OPRT : OTP mode protection bit

0 : OTP cell is able to be programmed

1 : OTP cell isn't able to be programmed

P15	P14	P13	P12	P11	P10	Offset Volume(x)
0	1	1	1	1	1	31
:	:	:	:	:	:	
0	0	0	0	0	1	1
0	0	0	0	0	0	0
1	1	1	1	1	1	-1
	:	:	:	:	:	:
1	0	0	0	0	0	-32

OTP Write Enable (EFH)

This command is used to write offset value (OV) into EPROM cells.

RS	RW_WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	1

Test Mode1 (FFH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	1	1	1

Test Mode2 (FEH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	1	1	0

Test Mode3 (FDH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	1	0	1

Test Mode4 (FBH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	0	1	1

Test Mode5 (FAH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	0	1	0

Test Mode6 (F9H)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	0	0	1

Test Mode7(F8)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

D/I	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	1	0	0	0

INSTRUCTION PARAMETER

Table 16. Instruction Parameter

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Oscillation Mode Set	02H	1	0	0	0	0	0	0	EXT	OSC
			*	*	*	*	*	*	0	0
Driver Output Mode Set	10H	1	0	0	DLN		0	SDIR	SWP	0
			*	*	0	0	*	0	0	0
DC-DC Set	20H	1	0	0	0	0	DC(2)		DC(1)	
			0	0	0	0	0	0	0	0
Bias Set	22H	1	0	0	Bias(2)		0	0	Bias(1)	
			0	*	0	0	*	*	0	0
DCDC Clock Division Set	24H	1	0	0	DIV(2)		0	0	DIV(1)	
			*	*	1	0	*	*	1	0
DCDC and AMP ON/OFF Set	26H	1	0	0	0	0	AMP	DCDC3	DCDC2	DCDC1
			*	*	*	*	0	0	0	0
Temperature Compensation Set	28H	1	0	0	0	0	0	0	TCS	
			*	*	*	*	*	*	0	0
Contrast Control (1)	2AH	1	Contrast control value in normal and partial display mode0(0 to 255)							
			0	0	0	0	0	0	0	0
Contrast Control(2)	2BH	1	Contrast control value in partial display mode 1(0 to 255)							
			0	0	0	0	0	0	0	0
Addressing Mode Set	30H	1	0	GSM		DSG	SGF	SGP		SGM
			*	0	0	1	1	1	0	1
ROW Vector Mode Set	32H	1	0	0	0	0	INC			VEC
			*	*	*	*	1	1	1	0
N-line Inversion Set	34H	1	FIM	FIP	0	N-block Inversion				
			1	0	*	0	1	1	0	1
Frame Frequency Control	36H	1	0	0	0	0	0	0	0	LFS
			*	*	*	*	*	*	*	0
Entry Mode Set	40H	1	0	0	0	0	HL	MDI	X/Y	RMW
			*	*	*	*	*	0	0	0
X-address Area Set	42H	2	X Start address set							
			0	0	0	0	0	0	0	0
			X end address set							
			1	0	1	0	0	0	0	1
Y-address Area Set	43H	2	Y start address set							
			0	0	0	0	0	0	0	0
			Y end address set							
			1	0	0	0	0	0	1	1
RAM Skip Area Set	42H	1	0	0	0	0	0	0	RSK	
			*	*	*	*	*	*	0	0
Set Display Data Length	FCH	2	Number of display data DDL_H							
			Number of display data DDL_L							
Specified Display Pattern Set	53H	1	0	0	0	0	0	0	SDP	
			*	*	*	*	*	*	0	0
Partial Display Mode Set	55H	1	0	0	0	0	0	0	PDM	PT
			*	*	*	*	*	*	0	0
Partial Display Start Line Set	56H	1	Partial start line							
			0	0	0	0	0	0	0	0
Partial Display End Line Set	57H	1	Partial end line							
			0	0	0	0	0	0	0	0

Table 16. Instruction Parameter (Continued)

Instruction	Hex	Para.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Area Scroll Mode Set	59H	4	0	0	0	0	0	0	SCM	
			*	*	*	*	*	*	0	0
			Scroll area start line							
			0	0	0	0	0	0	0	0
			Scroll area end line							
			1	0	1	0	0	0	0	1
			Lower Fixed number							
			0	0	0	0	0	0	0	0
Scroll Start Line Set	5AH	1	Scroll start line							
			0	0	0	0	0	0	0	0
Offset Volume Set	EDH	1	1	1	1	0	1	1	0	1
			*	*	*	0	0	0	0	0

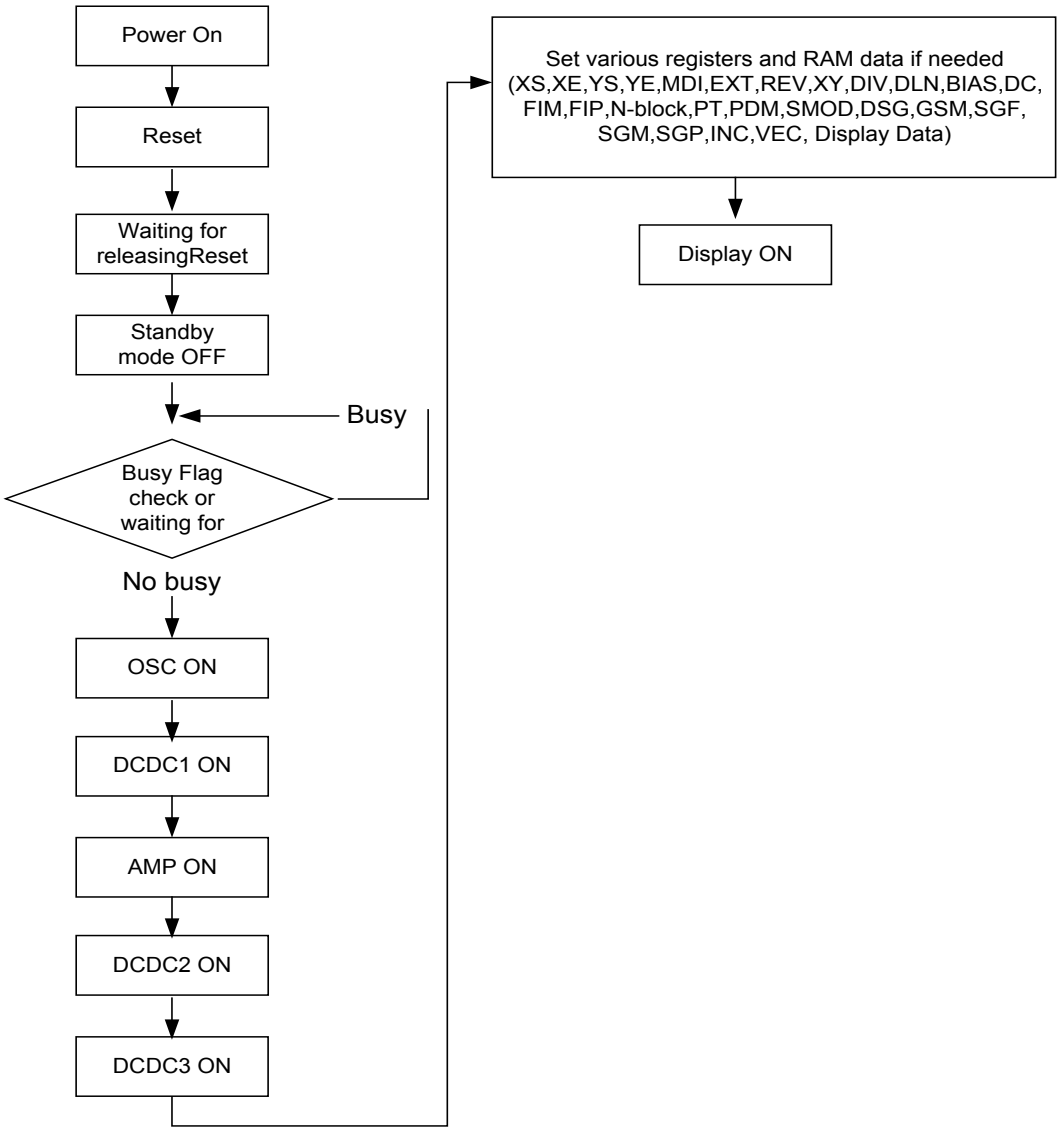
Reset Operation

When RSTB becomes “L”, following procedure is occurred.

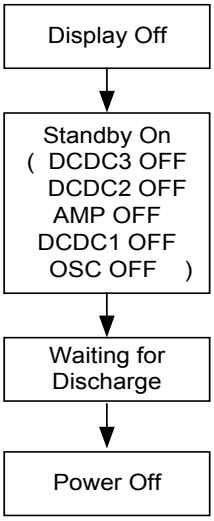
- X start address: 0, X end address: 161, - Y start address: 0, Y end address: 131
- Display OFF
- Read Modify Write Mode OFF
- Function Mode Set
  MDI = 0: Memory Data Inversion OFF
  OSC = 0: Oscillator OFF
  EXT = 0: Internal Oscillator Mode
  REV = 0: Reversing mode OFF
  X/Y = 0: Y-address Count Mode
  Standby Mode ON
- DCDC Clock Division Set
  DIV(1) = 10: fPCK = fOSC/16x
  DIV(2) = 10: fPCK = fOSC/16x
- Duty Set
  Display Duty = 00: 1/132 duty
- DC-DC Select
  DC(1) = 0: X1 step-up
  DC(2) = 0: X1 step-up
- Bias Set
  Bias(1) = 0H: 1/4 bias
  Bias(2) = 0H: 1/4 bias
- DC/DC and AMP ON/OFF Set
  AMP =0: Built-in OP-AMP OFF
  DCDC1 =0: Built-in 1’st booster OFF
  DCDC2 =0: Built-in 2’nd booster OFF
  DCDC3 =0: Built-in 3’rd booster OFF
- N-block inversion
  FIM =1: Forcing Inversion ON
  FIP =0: Forcing Inversion Period in one frame
  N-block inversion = 0DH: 13 block inversion
- Frame Frequency Control
  LFS =0: Low Frequency Set OFF
- Partial Display Mode
  PT = 0: Partial Display Mode OFF
- Partial Display Area Set
  Partial start line = 00H
  Partial end line = 00H
-Area Scroll Set
  Mode = 00H : Entire Display Scroll Mode
  Area Start Line: 00H
  Area End Line: A1H
  Lower Fixed Line Number: 00H
- Scroll Start Line Set
  Scroll Start Line: 00H
- Addressing Mode Set
  GSM=00: 65,536 Color Mode
  DSG = 1: No dummy subgroup
  SGF = 0: SG Frame Inversion OFF
  SGM = 1: SG Reverse Mode ON
  SGP=10: Different phase by 2pixel-unit
- Row Vector Mode Set
  INC =111: Increment every sub-frame
  VEC=0: R1->R2->R3->R4->R1->…

POWER ON/OFF SEQENCE

Power ON Sequence



Power OFF Sequence



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage range	VDD3	-0.3 to +4.0	V
LCD Supply Voltage range	|VCC – VEE|	22	V
Input Voltage range	Vin	- 0.3 to VDD +0.3	V
Operating Temperature range	TOPR	-30 to +70	°C
Storage Temperature range	TSTR	-55 to +150	°C

OPERATING VOLTAGE

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD3	1.8	-	3.3	V
Supply Voltage (2)	2Vr	4.0	-	20	V
Supply Voltage (3)	VIN	2.4	3.0	3.6	V

DC CHARACTERISTICS (1)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Operating voltage		VDD3		1.8		3.3	V	VDD3
Operating voltage		VIN1		2.4	-	3.6	V	VIN1,VIN1A
Operating voltage		VIN2		2.4	-	7.2	V	
Operating voltage		VIN45		2.4	-	7.2	V	VOUT45
Operating voltage		DC2IN	1/4 Bias	1.5	-	3.0	V	DC2OUT
			1/5 Bias	1.33	-	2.67		
			1/6 Bias	1.67	-	3.33		
			1/7 Bias	1.5	-	3.0		
Operating voltage		2Vr	2Vr = |(+VR)- (-VR)|	4.0	-	20	V	+VR, -VR
Driving voltage input range		VM	External power supply mode	1.0		2.0	V	VMOUT
		VCC		5.0		12.0	V	VRP
		VEE		-3.0		-8.0	V	VRN
Input voltage	High	V_{IH}		0.8VDD	-	VDD	V	
	Low	V_{IL}		VSS	-	0.2VDD		
Output voltage	High	V_{OH}	I_{OH} = 0.5mA	0.8VDD	-	VDD	V	
	Low	V_{OL}	I_{OL} = 0.5mA	VSS	-	0.2VDD		
Input leakage current		I_{IL}	VIN = VDD or VSS	-1.0	-	+1.0	μA	
Output leakage current		I_{OZ}	VIN = VDD or VSS	-3.0	-	+3.0	μA	
Oscillator Frequency Tolerance	Normal or Partial 0	F_{OSC1}	R1=90kOhm (fFR=100Hz target), DSG=1, 162 display lines	155.5	172.8	190.1	kHz	OSC1 - OSC2
	Partial 1	F_{OSC2}	R1=300kOhm (fFR=70Hz target), 66 display lines	44.35	49.28	54.21	kHz	OSC3 - OSC4
Oscillator Frequency Range	Normal or Partial 0	F_{OSC1}	(*1)	61.44		259.2	kHz	OSC1 - OSC2
	Partial 1	F_{OSC2}	(*2)	29.44		88.32	kHz	OSC3 - OSC4
Driving voltage input range		V1 VM		2.0 1.0	-	4.0 2.0	V	
Regulator output range		REG_OUT	REG_ENB = “L”	1.8	-	2.2	V	

(*1) Minimum oscillator frequency range is defined at fFR=60Hz and display line number=96
Maximum oscillator frequency range is defined at fFR=150Hz and display line number=162
(*2) Minimum oscillator frequency range is defined at fFR=40Hz and display line number=69
Maximum oscillator frequency range is defined at fFR=120Hz and display line number=69

DC CHARACTERISTICS (2)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Driver output resistance	SEG	$R_{ON\text{-}Seg}$	V1=3.0 V, V0=0V, Ta = 25°C, Iload=50uA	-	1.5	3.0	kΩ	SEGn
	COM	$R_{ON\text{-}Com}$	VCC=10.5 V, VM=1.5V, VEE=-7.5V, Ta = 25°C, Iload=100uA	-	1.0	1.5	kΩ	COMn
Current consumption	Normal Mode	IDD	VDD3=VIN1=3.0V, V1=3.0V, Bias(1)=1/6, DC(1)=x1.5, Ta=25°C, Display line=162 DSG=1 (No dummy) fOSC1=172.8kHz (fFR=100Hz) Low current mode, No load, No access, All white pattern	-	750	950	μA	VDD3 + VIN1
	Partial1 Mode		VDD3=VIN1=3.0V, V1=3.0V, Bias(2)=1/5, DC(2)=x1.5, Ta=25°C, 1/66 duty fOSC2=49.28kHz (fFR=70Hz) Low current mode, No load, No access, All white pattern	-	300	500	μA	

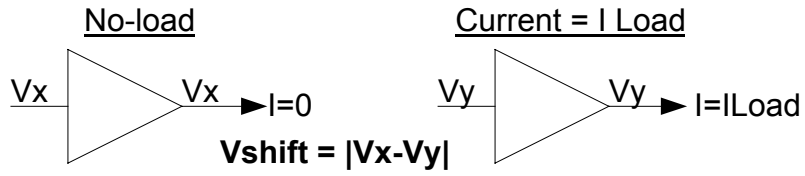
* : “TBD” is determined from lowest power consumption for dc-dc converter.

DC CHARACTERISTICS (3)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage shift range(*1)	Δ (+VR)	Isource = 80uA	-	-	150	mV	+VR
	Δ (V1)	Isource = 250uA	-	-	20	mV	V1
	Δ (VM)	Isource,sink = 250uA	-	-	20	mV	VM
	Δ (-VR)	Isink = 80uA	-	-	150	mV	-VR

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.
Refer to the following figure. (in case of source current mode)



Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias ratio	Δ (+VR)_0 Δ (-VR)_0(*1)	No load	-100	-	+100	mV	+VR -VR

(*1) Tolerance of bias ratio definition
Δ (+VR)_0 = ((+VR) - VM) – VM / Bias
Δ (-VR)_0 = (VM - (-VR)) – VM / Bias

DC CHARACTERISTICS (4)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item	Symbol	Condition		Min	Typ	Max	Unit	Remarks
Temperature compensation	ΔVt	VDD3=VIN1=V1=3.0V, -20 to 70 °C		-0.02	-	+0.02	%/°C	V1
Tolerance of Contrast step of V1	ΔVstep			3.13	6.27	9.41	mV	V1
Voltage range	ΔV1 ΔVM	Contrast set = FFh	V1	3.95	4.00	4.05	V	V1
			VM	1.95	2.00	2.05	V	VM
		Contrast set = 00h	V1	1.95	2.00	2.05	V	V1
			VM	0.95	1.00	1.05	V	VM

Item			Condition		Max	Unit	Ref
			Load current	Voltage range			
Offset Voltage	‖+VR-VM‖ -‖VM -(-VR)‖		I Load = +100uA (+VR) I Load = -100uA (-VR)	+VR=5.0~12.0 V V1=2.0~4.0V VM=1.0~2.0V -VR=-3.0~-8.0 V	150	mV	Fig.1
	‖V1-VM‖ -‖VM-V0‖	A	I Load = +100uA (V1, VM)		50	mV	Fig.2
		B	I Load = +100uA (+VR) I Load = -100uA (-VR)				

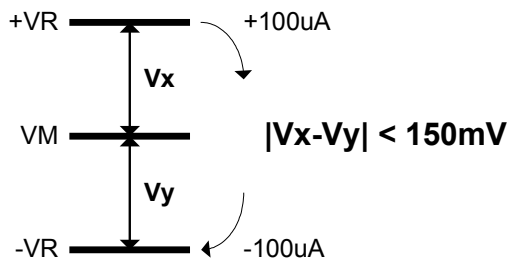


Fig. 1: Offset voltage definition (+VR,VM,-VR)

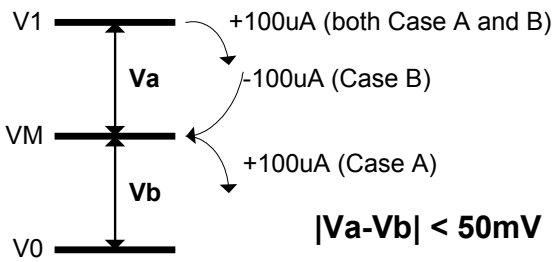


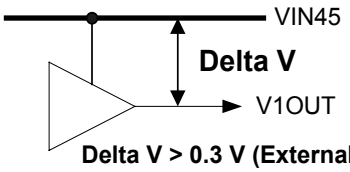
Fig. 2: Offset voltage definition (V1,VM,V0)

DC CHARACTERISTICS (5)

(Vss = 0V, V_{DD3} = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

Item		Range	
		Min	Max
Voltage Level	V1OUT	2.0 V	4.0 V (DC(1) and DC(2) = X2) (*1)
	VMOUT	1.0 V	2.0 V (DC(1) and DC(2) = X2) (*2)
	DC2OUT	1.33V (1/5 Bias, V1OUT = 2V)	3.33V (DC(1) and DC(2) = X2) (*3) (1/6 Bias, V1OUT = 4V)

(*1) This definition is shown as below



Delta V > 0.3 V (External VIN45)

Delta V > 0.5 V (VIN45 = VOUT45)

If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45. In this case, V1OUT output level must not be unstable. Refer to Fig.1

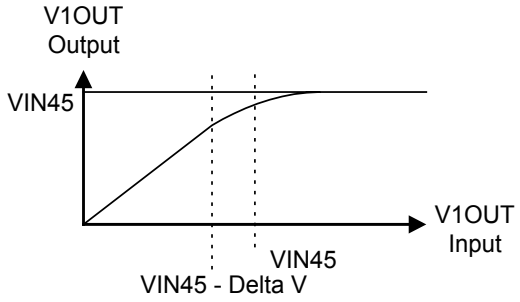
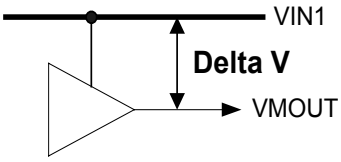


Fig. 1

(*2) This definition is shown as below



Delta V > 0.3 V

If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped near VIN1.
In this case, VMOUT output level must not be unstable. Refer to Fig.2

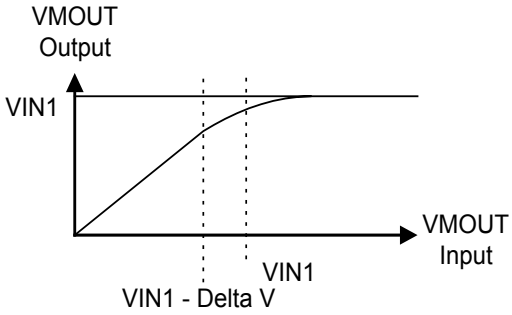
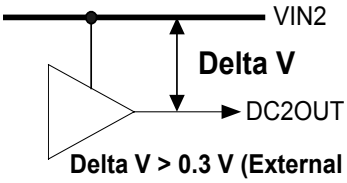


Fig. 2

(*3) This definition is shown as below



Delta V > 0.3 V (External VIN2)

Delta V > 0.5 V (VIN2 = VOUT45)

If DC2OUT input voltage is set over VIN2, DC2OUT output voltage must be clipped near VIN2. In this case, DC2OUT output level must not be unstable. Refer to Fig.3

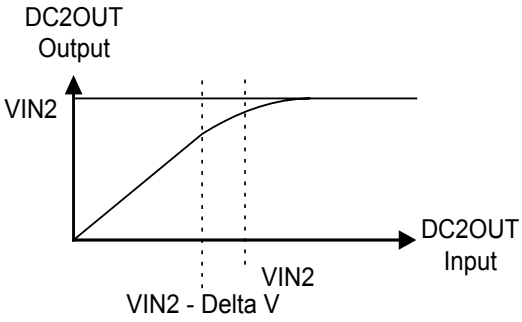
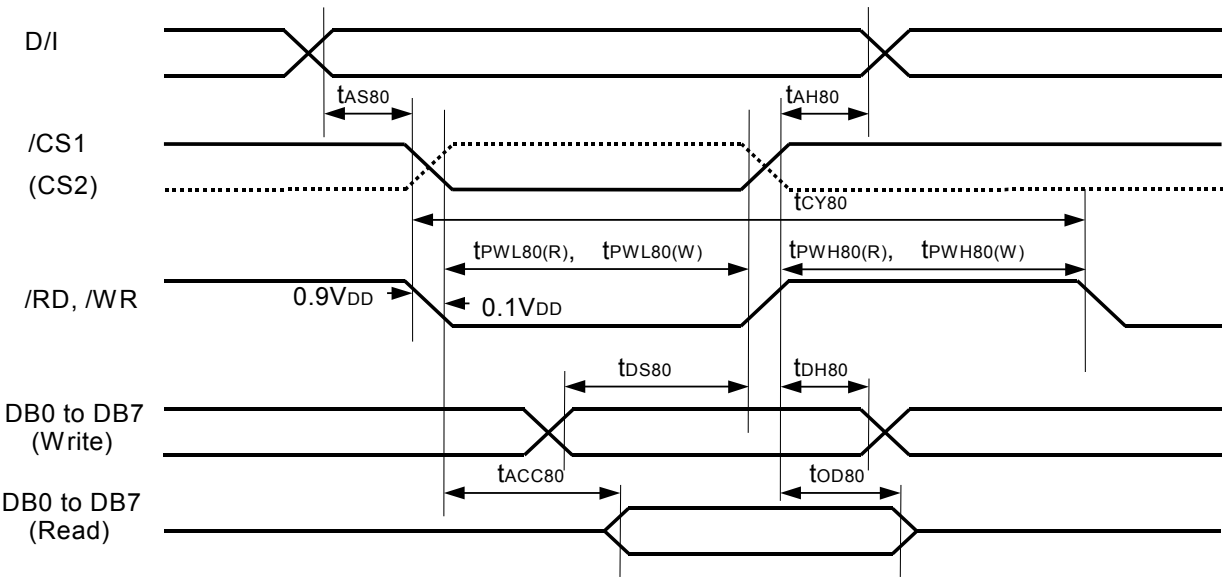


Fig. 3

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)



** $t_{PWL80(W)}$ and $t_{PWL80(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and /WR(/RD) is low.

Figure 25. Parallel Interface (8080-series MPU) Timing Diagram

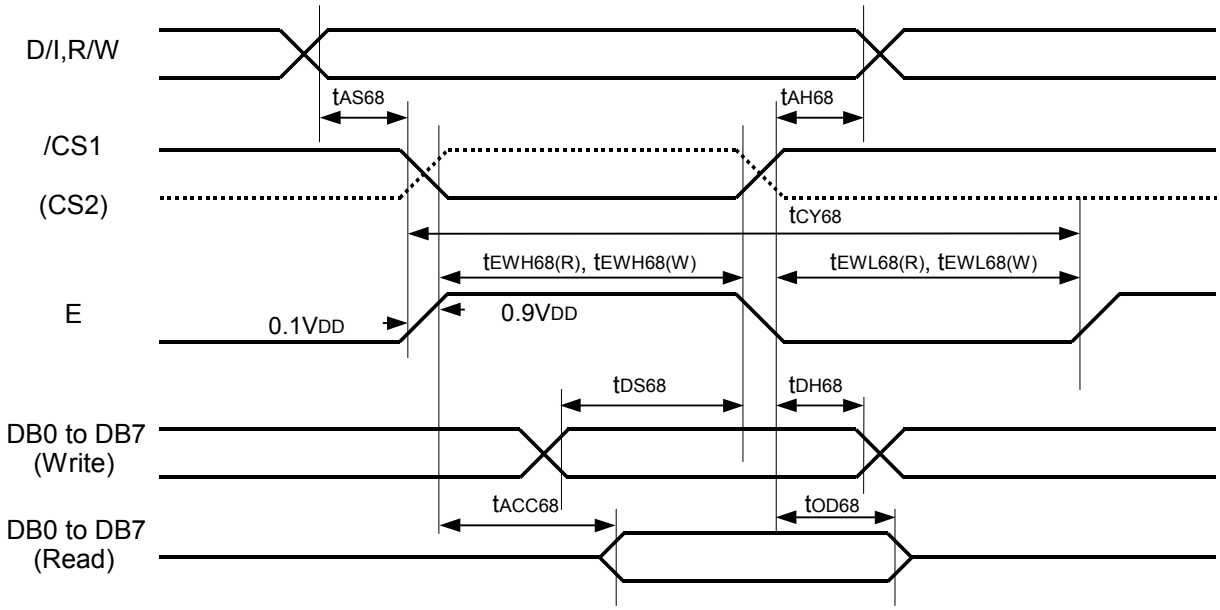
Table 17. AC Characteristics (8080-series Parallel Mode)

(VDD3 = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.		Max. (3.3V/1.8V)	Unit
				3.3V	1.8V		
Address setup time Address hold time	D/I	t_{AS80} t_{AH80}		0 0	0 0	- -	ns
System cycle time		t_{CY80}		150	360	-	ns
Pulse width low for write Pulse width High for write	WRB (WRB)	t_{PWLW} t_{PWHW}		50 30	100 75	- -	ns
Pulse width low for read Pulse width high for read	RDB (RDB)	t_{PWLR} t_{PWHR}		50 30	100 75	- -	ns
Data setup time Data hold time	DB0 to DB15	t_{DS80} t_{DH80}		5 28	10 54	- -	ns
Read access time		t_{ACC80}	CL = 100 pF	-		60 / 120	
Output disable time		t_{OD80}		-		50 / 100	

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
(tr + tf) < (t_{CY80} - t_{PWLW} - t_{PWHW}) for write, (tr + tf) < (t_{CY80} - t_{PWLR} - t_{PWHR}) for read

Read / Write Characteristics (6800-series Microprocessor)



** $t_{EWH68(W)}$ and $t_{EWH68(R)}$ is specified in the overlapped period when /CS1 is low (CS2 is high) and E is high.

Figure 26. Parallel Interface (6800-series MPU) Timing Diagram

Table 18. AC Characteristics (6800-series Parallel Mode)

(V_{DD3} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.		Max. (3.3V/1.8V)	Unit
				3.3V	1.8V		
Address setup time Address hold time	D/I R/W	t_{AS68} t_{AH68}		0 0	0 0	- -	ns
System cycle time		t_{CY68}		150	360	-	ns
Enable width high for write Enable width low for write	RDB (E)	t_{EWHW} t_{EWLW}		50 30	100 75	- -	ns
Enable width high for read Enable width low for read	RDB (E)	t_{EWHR} t_{EWLR}		50 30	100 75	- -	ns
Data setup time Data hold time	DB0 to DB15	t_{DS68} t_{DH68}		5 28	10 54	- -	ns
Read access time		T_{ACC68}	C_L = 100 pF	-		60 / 120	
Output disable time		t_{OD68}		-		50 / 100	

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
(tr + tf) < (t_{CY68} - t_{EWHW} - t_{EWLW}) for write, (tr + tf) < (t_{CY68} - t_{EWHR} - t_{EWLR}) for read

Serial Data Interface Timing

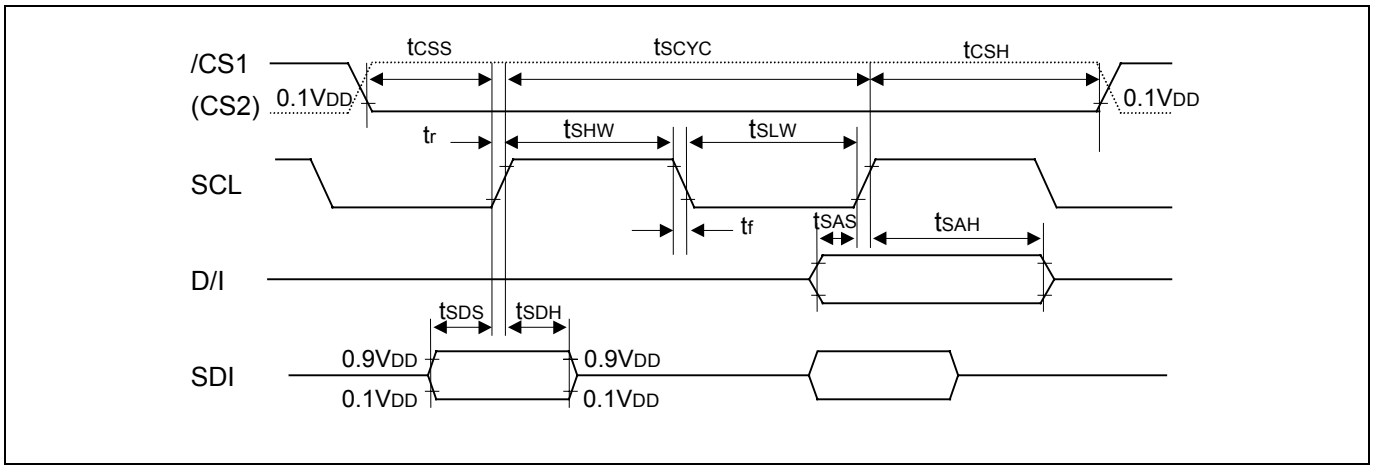


Table 19. Serial Data Interface Timing

(V_{DD3} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
SCL Cycle Time	SCL	t_{SCYC}		120	-	ns
SCL High Pulse Width	SCL	t_{SHW}		60	-	ns
SCL Low Pulse Width	SCL	t_{SLW}		60	-	ns
SDI Setup time	SDI	t_{SDS}		60	-	ns
SDI Hold time	SDI	t_{SDH}		60	-	ns
D/I Setup time	D/I	t_{SAS}		60	-	ns
D/I Hold time	D/I	t_{SAH}		60	-	ns
Chip Select Setup time	CS1B (CS2)	t_{CSS}		60	-	ns
Chip Select Hold time	CS1B (CS2)	t_{CHS}		60	-	ns

Reset Input Timing

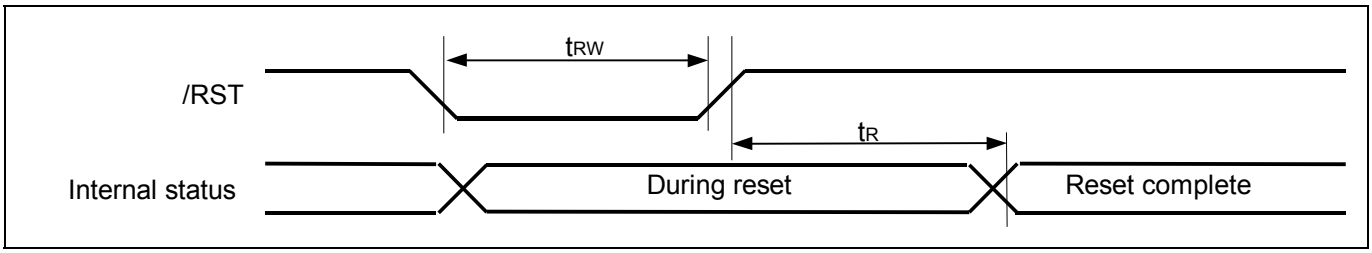


Figure 27. Reset Input Timing Diagram

Table 20. AC Characteristics (Reset mode)

(V_{DD3} = 1.8 to 3.3V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RSTB	t_{RW}		1000	-	ns
Reset time	-	t_R		-	1000	ns

SERIES SPECIFICATIONS

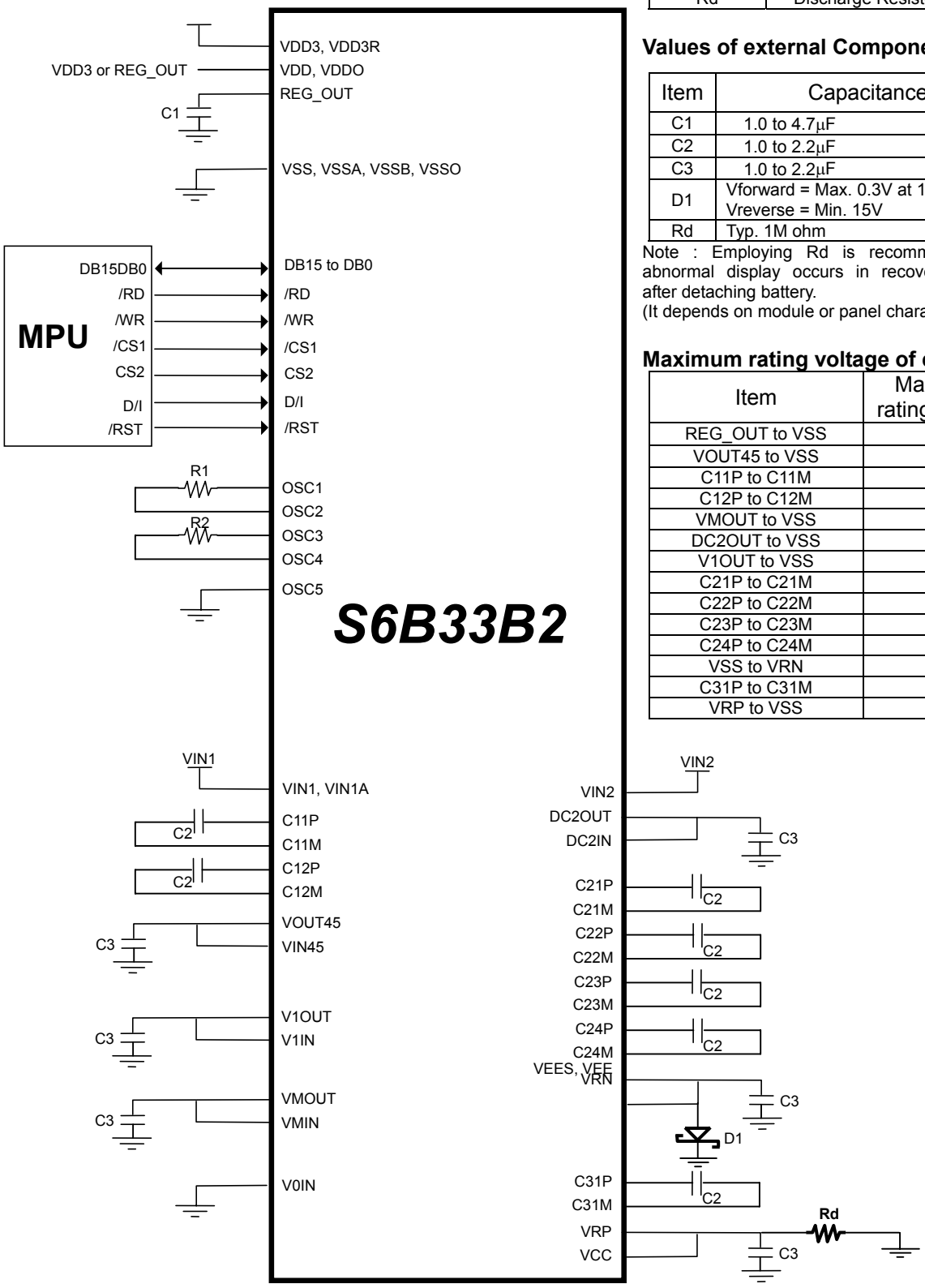
Product code	Temp. Coefficient	TCS Register Set *
S6B33B2X01-B0CY	0.00%/°C	00
S6B33B2X02-B0CY	-0.05%/°C	01
S6B33B2X03-B0CY	-0.10%/°C	10
S6B33B2X04-B0CY	-0.15%/°C	11

* Note :

In case of S6B33B2X01-B0CY, SEC guarantees only 0.00%/°C, not –0.05 and –0.10, -0.15%/°C.
In case of S6B33B2X02-B0CY, SEC guarantees only -0.05%/°C, not –0.00 and –0.1, -0.15%/°C.
In case of S6B33B2X03-B0CY, SEC guarantees only -0.10%/°C, not –0.00 and –0.05, -0.15%/°C.
In case of S6B33B2X04-B0CY, SEC guarantees only -0.15%/°C, not –0.00 and –0.05, -0.10%/°C.

SYSTEM APPLICATION DIAGRAM

Internal Power Mode



External Components

Name	Device
R1,R2	Resistors
C1,C2,C3	Capacitors
D1	Schottky barrier diode
Rd	Discharge Resistor

Values of external Components

Item	Capacitance
C1	1.0 to 4.7μF
C2	1.0 to 2.2μF
C3	1.0 to 2.2μF
D1	Vforward = Max. 0.3V at 1mA Vreverse = Min. 15V
Rd	Typ. 1M ohm

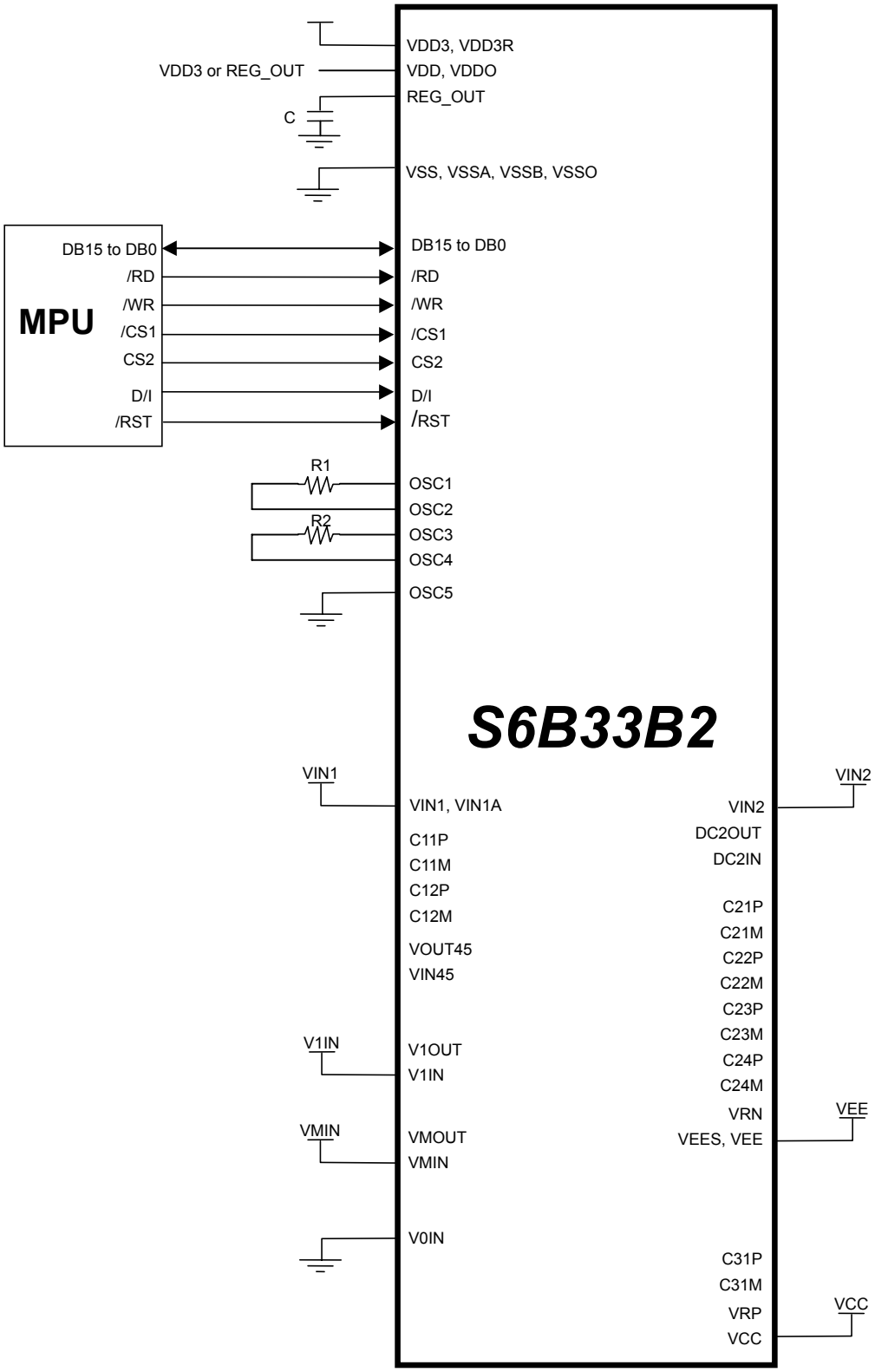
Note : Employing Rd is recommended when abnormal display occurs in recovery sequence after detaching battery.
(It depends on module or panel characteristics.)

Maximum rating voltage of capacitors

Item	Maximum rating voltage
REG_OUT to VSS	3V
VOUT45 to VSS	11V
C11P to C11M	6V
C12P to C12M	6V
VMOUT to VSS	3V
DC2OUT to VSS	5V
V1OUT to VSS	6V
C21P to C21M	5V
C22P to C22M	10V
C23P to C23M	13V
C24P to C24M	13V
VSS to VRN	13V
C31P to C31M	17V
VRP to VSS	18V

SAMSUNG ELECTRONICS

External Power Mode



OTP CALIBRATION MODE

SEQUENCE FOR SETTING THE MODIFIED ELECTRONIC VOLUME

- Next figure is a Block Diagram of Sequence for Setting the Modified Electronic Volume.

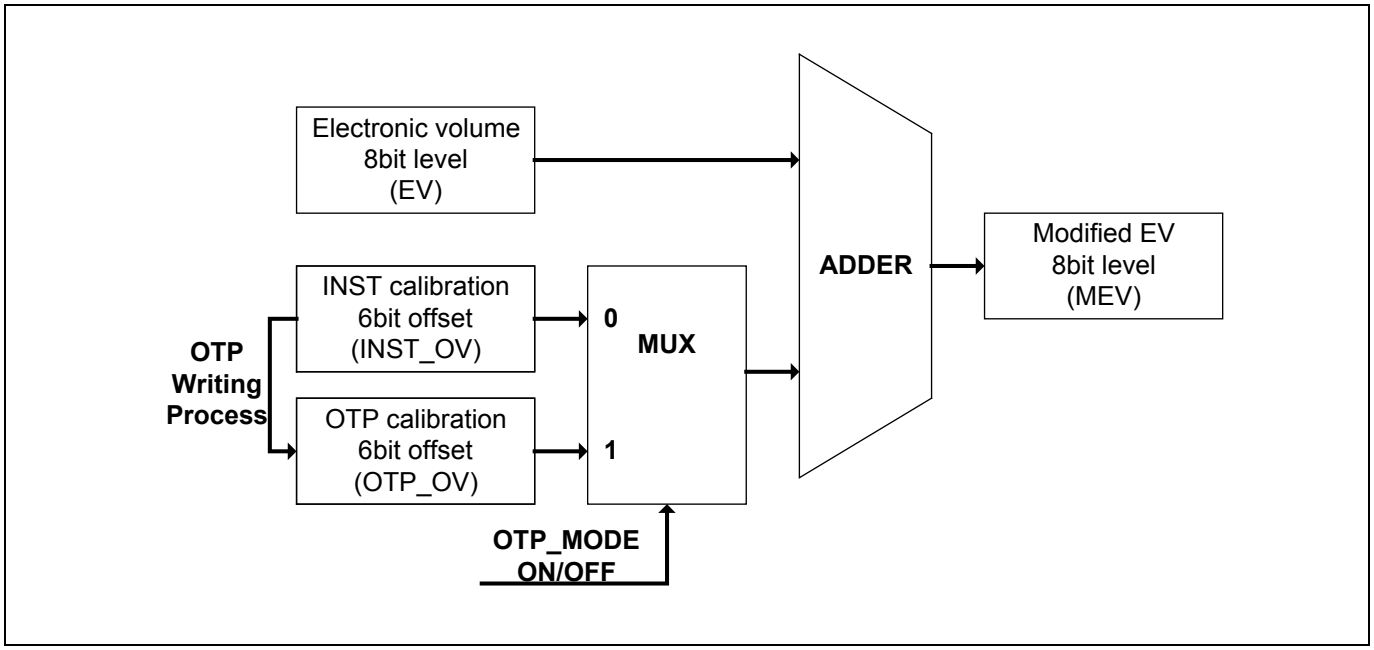


Figure 28. Sequence for Setting the Modified Electronic Volume

Initially, OTP cell is not programmed and has 6'b00000 value. When the external reset is applied, OTP mode is On. MEV is EV + OTP_OV. Since OTP_OV is 6'b00000, MEV is EV. For V1OUT calibration The instruction "OTP mode off" is executed, and then MEV is EV + OV and user can adjust MEV value using the instruction "Set offset volume register". When MEV overflows or underflows, MEV will be saturated. Repeat this step until end of the calibration. If V1OUT calibration is suitable, OTP writing process is executed, and then OTP cell is programmed and OTP_OV is programmed with OV. Finally, V1OUT calibration process is finished. Again, when the external reset is applied, OTP mode is ON. MEV is EV + OTP_OV. Accordingly MEV is the EV that has always the offset with OTP_OV value. However, if programmed OTP_OV is unlike, the instruction "OTP mode off" can be executed and then MEV will be EV + OV. Accordingly OV can be adjusted with instructions although OTP cell is programmed.

EPROM CELL STRUCTURE

OTP (One Time Programmable) has been implemented on the S6B33B2. The EPROM stores the offset volume for V1OUT calibration after the device has been assembled and calibrated on a LCD module. For OTP programming, OTPD pin and OTPG pin are used. These pins should be available to on the module glass by ITO.
The OTP block of the S6B33B2 consists of 7 bits. 1 bit is used for OTP mode protection bit (OPRT), and 6 bits are used for V1OUT calibration (OV5~OV0). OPRT can be read or written automatically in this LSI.

EPROM block

MSB LSB

OPRT	**OV5**	**OV4**	**OV3**	**OV2**	**OV1**	**OV0**

Description

OPRT : The Offset Volume(OV) can be written to EPROM cells only when OPRT bit = '0'
OV5~OV0 : The OV is used for calibrating the V1OUT voltage as an offset to the EV register value.

V1OUT CALIBRATION FLOW

V1OUT may be calibrated with OTP in the following order.(ex : EV = 32, OV=-3)

STEP	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1.											Apply external reset (OTP data read)
2.	0	0	0	0	1	0	1	0	1	0 or 1	Set contrast control 1 or 2 by using instruction (EV = 32)
	0	0	0	0	1	0	0	0	0	0	
3.	0	0	1	1	1	0	1	0	1	0	OTP mode off by using the instruction
4.	0	0	1	1	1	0	1	1	0	1	Set offset volume by using the instruction (OV = -3)
	0	0	0	0	1	1	1	1	0	1	
5											Repeat STEP 4. Until the end of the calibration
6.											Apply programming voltages for OTP programming (OTPG=12.5V,OTPD=10)
7.	0	0	0	0	1	0	1	1	0	1	Standby on by using the instruction.
8	0	0	1	1	1	0	1	1	1	1	OTP write Enable **(Only available when OPRT= 0)**
9											Apply external reset
10.											Cut off programming voltages for OTP programming (OTPG,OTPD)

After the external reset, the calibrated data are automatically transferred to the 6-bit reference voltage control register.
*Step 6, 7, 8, 9 are OTP_WRITING PROCESS.
*OTP_WRITING PROCESS is available when OPRT is zero (if OPRT = 1, OTP cell could not be programmed).

VOLTAGES AND WAVEFORMS FOR OTP PROGRAMMING

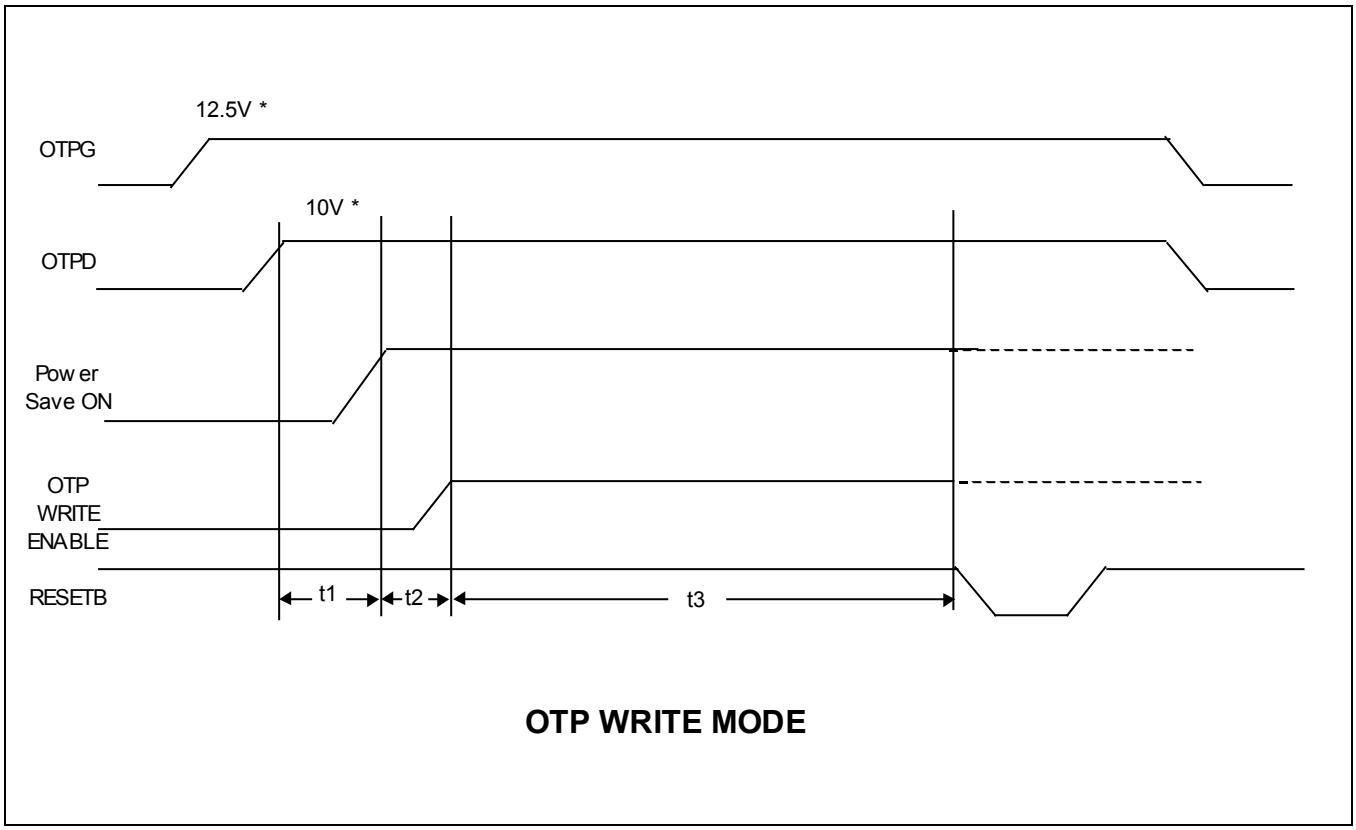


Figure 29. Voltages and waveforms for OTP programming (OTP Writing Process)

* Note : Voltages for OTPG and OTPD may be changed.

Specific timings (t1~t3)

Timing	Min	Max
t1,t2	100uS	-
t3	100mS	2S