SECTION 2

HIGH SPEED OP AMPS

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SECTION 2

HIGH SPEED OP AMPS

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Modern system design increasingly makes use of high speed ICs as circuit building blocks. With bandwidths going up and up, demands are placed on the designer for faster and more power efficient circuits. The default high speed amplifier has changed over the years, with high speed complementary bipolar (CB) process ICs such as the AD846 and AD847 in use just about ten years at this writing. During this time, the general utility/availability of these and other ICs have raised the “high speed” common performance denominator to 50MHz. The most recent extended frequency complementary bipolar (XFCB) process high speed devices such as the AD8001/AD8002, the AD9631/9632 and the AD8036/AD8037 now extend the operating range into the UHF region.

Of course, a traditional performance barrier has been speed, or perhaps more accurately, *painless* speed. While fast IC amplifiers have been around for some time, until more recently they simply haven't been the easiest to use. As an example, devices with substantial speed increases over 741/301A era types, namely the 318-family, did so at the expense of relatively poor settling and capacitive loading characteristics. Modern CB process parts like the AD84X series provide far greater speed, faster settling, and do so at low user cost. Still, the application of high performance fast amplifiers is never entirely a cookbook process, so designers still need to be wary of many inter-related key issues. This includes not just the amplifier selection, but also control of parasitics and other potentially performance-limiting details in the surrounding circuit.

It is worth underscoring that reasons for the "speed revolution" lie not just in affordability of the new high speed ICs, but is also rooted in their *ease of use*. Compared to earlier high speed ICs, CB process devices are generally more stable with capacitive loads (with higher phase margins in general), have lower DC errors, consume less power for a given speed, and are all around more "user friendly". Taking this a step further, XFCB family devices, which extend the utility of the op amp to literally hundreds of MHz, are understandably less straightforward in terms of their application (as is any amplifier operating over such a range). Thus, getting the most from these modern devices definitely stresses the “total environment” aspects of design.

Another major ease of use feature found in today's linear ICs is a much wider range of supply voltage characterization. While the older ±15V standard is still much in use, there is a trend towards including more performance data at popular lower voltages, such as ±5V, or +5V only, single supply operation. The most recent devices using the lower voltage XFCB process use supply voltages of either ±5V, or simply +5V only. The trend towards lower supply voltages is unmistakable, with a goal of squeezing the highest performance from a given voltage/power circuit environment. These "ease of use" design aspects with current ICs are illustrated in this chapter,

along with parasitic issues, optimizing performance over supply ranges, and low distortion stages in a variety of applications.

DRIVING CAPACITIVE LOADS

From system and signal fidelity points of view, transmission line coupling between stages is best, and is described in some detail in the next section. However, complete transmission line system design may not always be possible or practical. In addition, various other parasitic issues need careful consideration in high performance designs. One such problem parasitic is amplifier load capacitance, which potentially comes into play for all wide bandwidth situations which do not use transmission line signal coupling.

A general design rule for wideband linear drivers is that capacitive loading (cap loading) effects should *always* be considered. This is because PC board capacitance can build up quickly, especially for wide and long signal runs over ground planes insulated by thin, higher K dielectric. For example, a 0.025" PC trace using a G-10 dielectric of 0.03" over a ground plane will run about 22pF/foot (Reference 1). Even relatively small load capacitance (i.e., <100 pF) can be troublesome, since while not causing outright oscillation, it can still stretch amplifier settling time to greater than desirable levels for a given accuracy.

The effects of cap loading on high speed amplifier outputs are not simply detrimental, they are actually an anathema to high quality signals. However, before-the-fact designer knowledge still allows high circuit performance, by employing various tricks of the trade to combat the capacitive loading. If it is not driven via a transmission line, remote signal circuitry should be checked for capacitive loading very carefully, and characterized as best possible. Drivers which face poorly defined load capacitance should be bullet-proofed accordingly with an appropriate design technique from the options list below.

Short of a true matched transmission line system, a number of ways exist to drive a load which is capacitive in nature while maintaining amplifier stability.

Custom capacitive load (cap load) compensation, includes two possible options, namely a); overcompensation, and b); an intentionally forced-high loop noise gain allowing crossover in a stable region. Both of these steps can be effective in special situations, as they reduce the amplifier's effective closed loop bandwidth, so as to restore stability in the presence of cap loading.

Overcompensation of the amplifier, when possible, reduces amplifier bandwidth so that the additional load capacitance no longer represents a danger to phase margin. As a practical matter however, amplifier compensation nodes to allow this are available on few high speed amplifiers. One such useful example is the AD829, compensated by a single capacitor at pin 5. In general, almost any amplifier using external compensation can always be over compensated to reduce bandwidth. This will restore stability against cap loads, by lowering the amplifier's unity gain frequency.

CAPACITIVE LOADING ON OP AMP GENERALLY REDUCES PHASE MARGIN AND MAY CAUSE INSTABILITY, BUT INCREASING THE NOISE GAIN OF THE CIRCUIT IMPROVES STABILITY

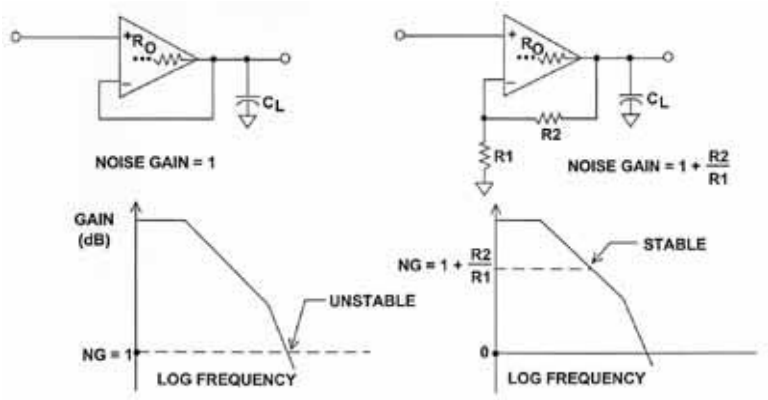

Figure 2.1

Forcing a high noise gain, is shown in Figure 2.1, where the capacitively loaded amplifier with a noise gain of unity at the left is seen to be unstable, due to a 1/ß - open loop rolloff intersection on the Bode diagram in an unstable –12dB/octave region. For such a case, quite often stability can be restored by introducing a higher noise gain to the stage, so that the intersection then occurs in a stable –6dB/octave region, as depicted at the diagram right Bode plot.

RAISING NOISE GAIN (DC OR AC) FOR FOLLOWER OR INVERTER STABILITY

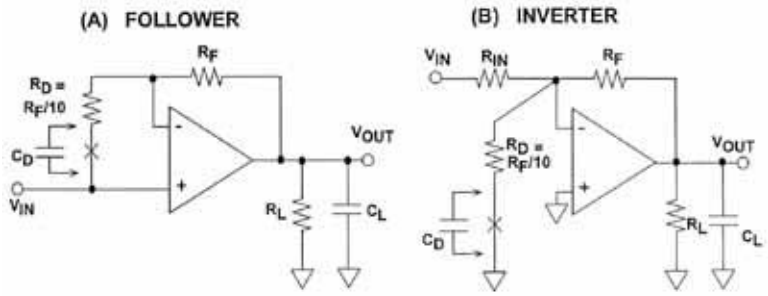

Figure 2.2

To enable a higher noise gain (which does not necessarily need to be the same as the stage's *signal gain*), use is made of resistive or RC pads at the amplifier input, as in Figure 2.2. This trick is more broad in scope than overcompensation, and has the advantage of not requiring access to any internal amplifier nodes. This generally allows use with any amplifier setup, even voltage followers. The technique adds an extra resistor R_D, which works against R_F to force the noise gain of the stage to a level appreciably higher than the signal gain (which is unity in both cases here). Assuming that C_L is a value which produces a parasitic pole near the amplifier's natural crossover, this loading combination would likely lead to oscillation due to the

excessive phase lag. However with R_D connected, the higher amplifier noise gain produces a new 1/ß - open loop rolloff intersection, about a decade lower in frequency. This is set low enough that the extra phase lag from C_L is no longer a problem, and amplifier stability is restored.

A drawback to this trick is that the DC offset and input noise of the amplifier are raised by the value of the noise gain, when the optional C_D is *not* present. But, when C_D is used in series with R_D, the offset voltage of the amplifier is not raised, and the gained-up AC noise components are confined to a frequency region above $1/(2pi \cdot R_D \cdot C_D)$. A further caution is that the technique can be somewhat tricky when separating these operating DC and AC regions, and should be applied carefully with regard to settling time (Reference 2). Note that these simplified examples are generic, and in practice the absolute component values should be matched to a specific amplifier.

"Passive" cap load compensation, shown in Figure 2.3, is the most simple (and most popular) isolation technique available. It uses a simple "out-of-the-loop" series resistor R_X to isolate the cap load, and can be used with any amplifier, current or voltage feedback, FET or bipolar input.

OPEN-LOOP SERIES RESISTANCE ISOLATES CAPACITIVE LOAD FOR AD811 CURRENT FEEDBACK OP AMP (CIRCUIT BANDWIDTH = 13.5 MHz)

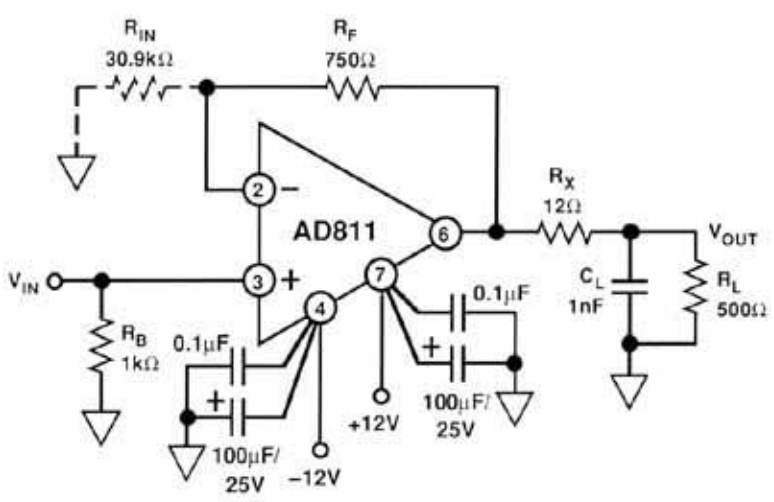

Figure 2.3

As noted, this technique can be applied to virtually any amplifier, which is a major reason why it is so useful. It is shown here with a current feedback amplifier suitable for high current line driving, the AD811, and it consists of just the simple (passive) series isolation resistor, R_X. This resistor's minimum value for stability will vary from device to device, so the amplifier data sheet should be consulted for other ICs. Generally, information will be provided as to the amount of load capacitance tolerated, and a suggested minimum resistor value for stability purposes.

Drawbacks of this approach are the loss of bandwidth as R_X works against C_L, the loss of voltage swing, a possible lower slew rate limit due to I_{MAX} and C_L, and a gain error due to the R_X-R_L division. The gain error can be optionally compensated with R_{IN}, which is ratioed to R_F as R_L is to R_X. In this example, a ±100mA output from the op amp into C_L can slew V_{OUT} at a rate of 100V/µs, far below the intrinsic AD811 slew rate of 2500V/µs. Although the drawbacks are serious, this form of cap load compensation is nevertheless useful because of its simplicity. If the amplifier is not otherwise protected, then an R_X resistor of 50-100ohms should be used with virtually any amplifier facing capacitive loading. Although a non-inverting amplifier is shown, the technique is equally applicable to inverter stages.

With very speed high amplifiers, or in applications where lowest settling time is critical, even small values of load capacitance can be disruptive to frequency response, but are nevertheless sometimes inescapable. One case in point is an amplifier used for driving ADC inputs. Since high speed ADC inputs quite often look capacitive in nature, this presents an oil/water type problem. In such cases the amplifier *must* be stable driving the capacitance, but it must also preserve its best bandwidth and settling time characteristics. To address this type of cap load case performance, R_S and C_L data for a specified settling time is most appropriate.

Some applications, in particular those that require driving the relatively high impedance of an ADC, do not have a convenient back termination resistor to dampen the effects of capacitive loading. At high frequencies, an amplifier's output impedance is rising with frequency and acts like an inductance, which in combination with C_L causes peaking or even worse, oscillation. When the bandwidth of an amplifier is an appreciable percentage of device f_t,the situation is complicated by the fact that the loading effects are reflected back into its internal stages. In spite of this, the basic behavior of most very wide bandwidth amplifiers such as the AD8001 is very similar.

In general, a small damping resistor (R_S) placed in series with C_L will help restore the desired response (see Figure 2.4). The best choice for this resistor's value will depend upon the criterion used in determining the desired response. Traditionally, simply stability or an acceptable amount of peaking has been used, but a more strict measure such as 0.1% (or even 0.01%) settling will yield different values. For a given amplifier, a family of R_S - C_L curves exists, such as those of Figure 2.4. These data will aid in selecting R_S for a given application.

AD8001 R_S REQIRED FOR VARIOUS CL VALUES

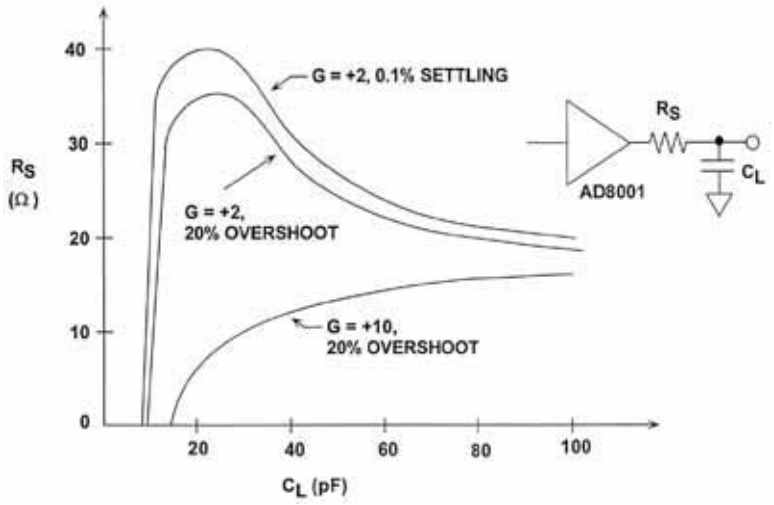

Figure 2.4

The basic shape of this curve can be easily explained. When C_L is very small, no resistor is necessary. When C_L increases to some threshold value an R_S becomes necessary. Since the frequency at which the damping is required is related to the $R_S \cdot C_L$ time constant, the R_S needed will initially increase rapidly from zero, and then will decrease as C_L is increased further. A relatively strict requirement, such as for 0.1%, settling will generally require a larger R_S for a given C_L, giving a curve falling higher (in terms of R_S) than that for a less stringent requirement, such as 20% overshoot. For the common gain condition of +2, these two curves are plotted in the figure for 0.1% settling (upper-most curve) and 20% overshoot (middle curve). It is also worth mentioning that higher closed loop gains lessen the problem dramatically, and will require less R_S for the same performance. The third (lower-most) curve illustrates this, demonstrating a closed loop gain of 10 R_S requirement for 20% overshoot for the AD8001 amplifier. This can be related to the earlier discussion associated with Figure 2.2.

The recommended values for R_S will optimize response, but it is important to note that generally C_L will degrade the maximum bandwidth and settling time performance which is achievable. In the limit, a large $R_S \cdot C_L$ time constant will dominate the response. In any given application, the value for R_S should be taken as a starting point in an optimization process which accounts for board parasitics and other secondary effects.

Active or "in-the-loop" cap load compensation can also be used as shown in Figure 2.5, and this scheme modifies the passive configuration to provide feedback correction for the DC & low frequency gain error associated with R_X. In contrast to the passive form, active compensation can only be used with voltage feedback amplifiers, because current feedback amplifiers don't allow the integrating connection of C_F.

ACTIVE "IN-LOOP" CAPACITIVE LOAD COMPENSATION CORRECTS FOR DC AND LF GAIN ERRORS

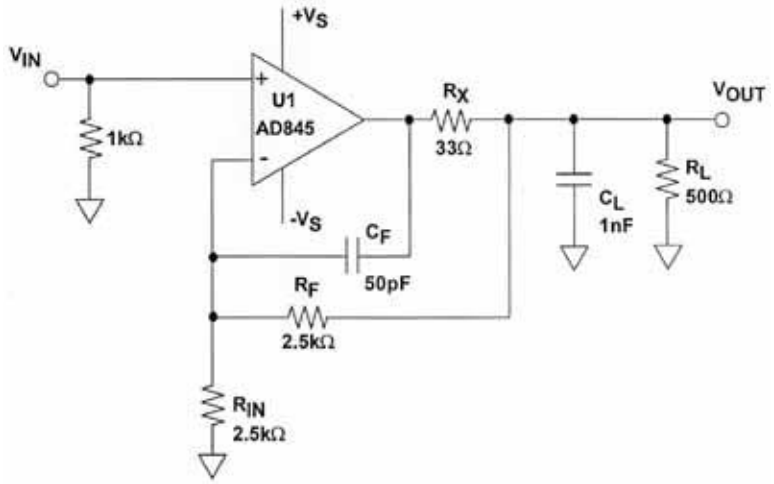

Figure 2.5

This circuit returns the DC feedback from the output side of isolation resistor R_X, thus correcting for errors. AC feedback is returned via C_F, which bypasses R_X/R_F at high frequencies. With an appropriate value of C_F (which varies with C_L, for fixed resistances) this stage can be adjusted for a well damped transient response (Reference 2,3). There is still a bandwidth reduction, a headroom loss, and also (usually) a slew rate reduction, but the DC errors can be very low. A drawback is the need to tune C_F to C_L, as even if this is done well initially, any change to C_L will alter the response away from flat. The circuit as shown is useful for voltage feedback amplifiers only, because capacitor C_F provides integration around U1. It also can be implemented in inverting fashion, by driving the bottom end of R_{IN}.

Internal cap load compensation involves the use of an amplifier which internally has topological provisions for the effects of external cap loading. To the user, this is the most transparent of the various techniques, as it works for any feedback situation, for any value of load capacitance. Drawbacks are that it produces higher distortion than does an otherwise similar amplifier without the network, and the compensation against cap loading is somewhat signal level dependent.

AD817 SIMPLIFIED SCHEMATIC ILLUSTRATES INTERNAL COMPENSATION FOR DRIVING CAPACITIVE LOADS

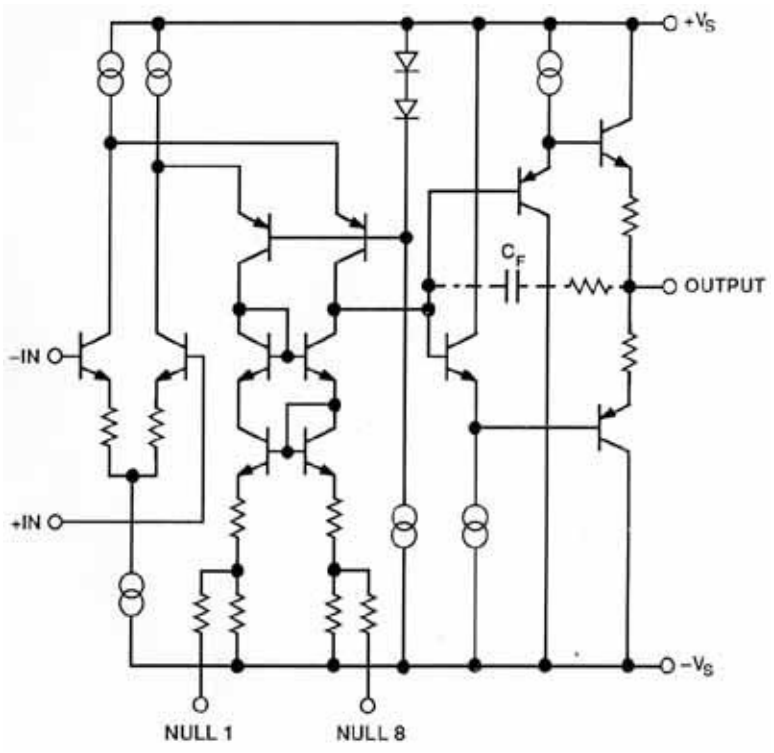

Figure 2.6

The internal cap load compensated amplifier sounds at first like the best of all possible worlds, since the user need do nothing at all to set it up. Figure 2.6, a simplified diagram of an amplifier with internal cap load compensation, shows how it works. The cap load compensation is the C_F -resistor network shown around the unity gain output stage of the amplifier - note that the dotted connection of this network underscores the fact that it only makes its presence felt for certain load conditions.

Under normal (non-capacitive or light resistive) loading, there is limited input/output voltage error across the output stage, so the C_F network then sees a relatively small voltage drop, and has little or no effect on the amplifier's high impedance compensation node. However when a capacitor (or other heavy) load is present, the high currents in the output stage produce a voltage difference across the C_F network, which effectively adds capacitance to the compensation node. With this relatively heavy loading, a net larger compensation capacitance results, and reduces the amplifier speed in a manner which is adaptive to the external capacitance, C_L. *As a point of reference, note that it requires 6.3mA peak to support a 2Vp-p swing across a 100pF load at 10MHz.*

Since this mechanism is resident in the amplifier output stage and it affects the overall compensation characteristics dynamically, it acts independent of the specific

feedback hookup, as well as size of the external cap loading. In other words, it can be transparent to the user in the sense that no specific design conditions need be set to make it work (other than selecting an IC which employs it). Some amplifiers using internal cap load compensation are the AD847 and the AD817, and their dual equivalents, AD827 and AD826.

There are, however, some caveats also associated with this internal compensation scheme. As with the passive compensation techniques, bandwidth decreases as the device slows down to prevent oscillation with higher load currents. Also, this adaptive compensation network has its greatest effect when enough output current flows to produce significant voltage drop across the C_F network. Conversely, at small signal levels, the effect of the network on speed is less, so greater ringing may actually be possible for some circuits for lower-level outputs.

RESPONSE OF INTERNAL CAP LOAD COMPENSATED AMPLIFIER VARIES WITH SIGNAL LEVEL

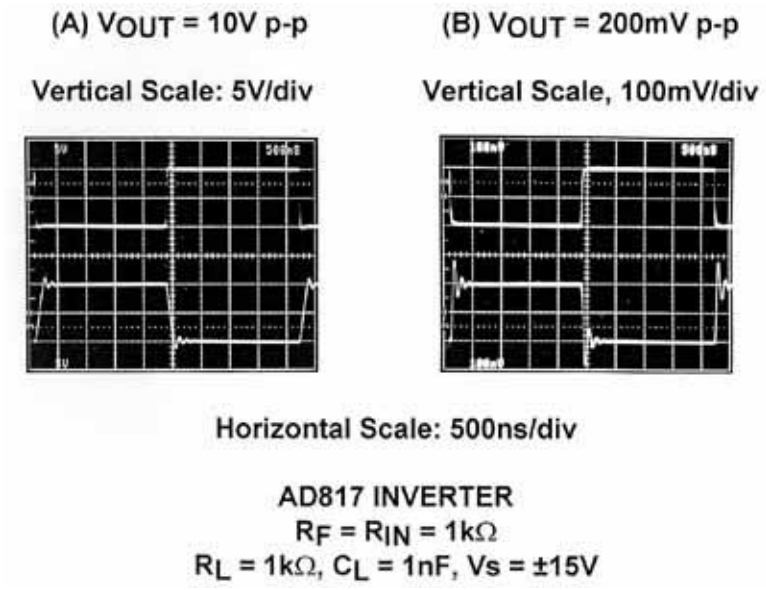

Figure 2.7

The dynamic nature of this internal cap load compensation is illustrated in Figure 2.7, which shows an AD817 unity gain inverter being exercised at both high and low output levels, with common conditions of V_S = ±15V, R_L = 1kohm, C_L = 1nF, and using 1kohm input/feedback resistors. In both photos the input signal is on the top trace and the output signal is on the bottom trace, and the time scale is fixed. In the 10Vp-p output (A) photo at the left, the output has slowed down appreciably to accommodate the capacitive load, but settling is still relatively clean, with a small percentage of overshoot. This indicates that for this high level case, the bandwidth reduction due to C_L is most effective. However, in the (B) photo at the right, the 200mVp-p output shows greater overshoot and ringing, for the lower level signal. The point is made that, to some degree at least, the relative cap load immunity of this type of internally cap load compensated amplifier is signal dependent.

Finally, because the circuit is based on a nonlinear principle, the internal network affects distortion and load drive ability, and these factors influence amplifier performance in video applications. Though the network's presence does not by any means make devices like the AD847 or AD817 unusable for video, it does not permit the very lowest levels of distortion and differential gain and phase which are achievable with otherwise comparable amplifiers (for example, the AD818).

While the individual techniques for countering cap loading outlined above have various specific tradeoffs as noted, all of the techniques have a serious common drawback of reducing speed (both bandwidth and slew rate). If these parameters cannot be sacrificed, then a matched transmission line system is the solution, and is discussed in more detail later in the chapter. As for choosing among the cap load compensation schemes, it would seem on the surface that amplifiers using the internal form offer the best possible solution to the problem- just pick the right amplifier and forget about it. And indeed, that would seem the "panacea" solution for all cap load situations - if you use the "right" amplifier you never need to think about cap loading again. Could there be more to it?

Yes! The "gotcha" of internal cap load compensation is subtle, and lies in the fact that the dynamic adaptive nature of the compensation mechanism actually can produce higher levels of distortion, vis-à-vis an otherwise similar amplifier, *without* the C_F-resistor network. Like the old saying about no free lunches, if you care about attaining top-notch levels of high frequency AC performance, you should give the issue of whether to use an internally compensated cap load amplifier more serious thought than simply picking a trendy device.

On the other hand, if you have no requirements for the lowest levels of distortion, then such an amplifier could be a good choice. Such amplifiers are certainly easier to use, and relatively forgiving about loading issues. Some applications of this chapter illustrate the distortion point specifically, quoting performance in a driver circuit with/without the use of an internal cap load compensated amplifiers.

With increased gain bandwidths of greater than or equal to 100MHz available in today's ICs, layout, grounding and the control of parasitics become much, much more important. In fact, with the fastest available ICs such as the XFCB types, these issues simply cannot be ignored, they are critical and *must* be addressed for stable performance. All high frequency designs can profit from the use of low parasitic construction techniques, such as described in Chapter 9. In the circuit discussions which follow, similar methods should be used for best results, and in the very high frequency circuits (greater than 100MHz) it is mandatory. Some common pitfalls are covered before getting into specific circuit examples.

As with all wide bandwidth components, good PC board layout is critical to obtain the best dynamic performance with these high speed amplifiers. The ground plane in the area of the op amp and its associated components should cover as much of the component side of the board as possible (or first interior ground layer of a multilayer board).

The ground plane should be removed in the area of the amplifier inputs and the feedback and gain set resistors to minimize stray capacitance at the input. Each power supply trace should be decoupled close to the package with a minimum of 0.1µF ceramic (preferably surface mount), plus a 6.8µF or larger tantalum capacitor within 0.5", as a charge storage reservoir when delivering high peak currents (line drivers, for example). Optionally, larger value conventional electrolytic can be used in place of the tantalum types, if they have a low ESR.

All lead lengths for input, output, and feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors (buffed metal film rather than laser-trimmed spiral-wound) and/or carbon resistors.

Microstrip techniques should be used for all input and output lead lengths in excess of one inch (Reference 1). Sockets should be avoided if at all possible because of their parasitic capacitance and inductance. If sockets are necessary, individual *pin sockets* such as AMP p/n 6-330808-3 should be used. These contribute far less stray capacitance and inductance than molded socket assemblies.

The effects of inadequate decoupling on harmonic distortion performance are dramatically illustrated in Figure 2.8. The left photo shows the spectral output of the AD9631 op amp driving a 100ohm load with proper decoupling (output signal is 20MHz, 2V p-p). Notice that the second harmonic distortion at 40MHz is approximately –70dBc. If the decoupling is removed, the distortion is increased, as shown in the right photo of the same figure. Figure 2.8 (right-hand photo) also shows stray RF pickup in the wiring connecting the power supply to the op amp test fixture. Unlike lower frequency amplifiers, the power supply rejection ratio of many high frequency amplifiers is generally fairly poor at high frequencies. For example, at 20MHz, the power supply rejection ratio of the AD9631 is less than 25dB. This is the primary reason for the degradation in performance with inadequate decoupling. The change in output signal produces a corresponding signal-dependent load current change. The corresponding change in power supply voltage due to inadequate decoupling produces a signal-dependent error in the output which manifests itself as an increase in distortion.

EFFECTS OF INADEQUATE DECOUPLING ON HARMONIC DISTORTION PERFORMANCE OF AD9631 OP AMP

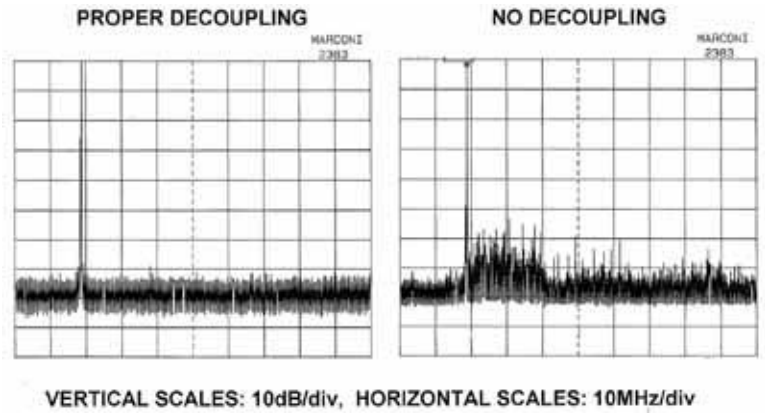

Figure 2.8

Inadequate decoupling can also severely affect the pulse response of high speed amplifiers such as the AD9631. Figure 2.9 shows normal operation and the effects of removing all decoupling capacitors on the AD9631 in its evaluation board. Notice the severe ringing on the pulse response for the poorly decoupled condition, in the right photo. A Tektronix 644A, 500MHz digitizing oscilloscope was used to make the measurement (as well as the pulse responses in Figure 2.10, 2.14, 2.15, 2.16, and 2.17).

EFFECT OF INADEQUATE DECOUPLING ON PULSE RESPONSE OF AD9631 OP AMP

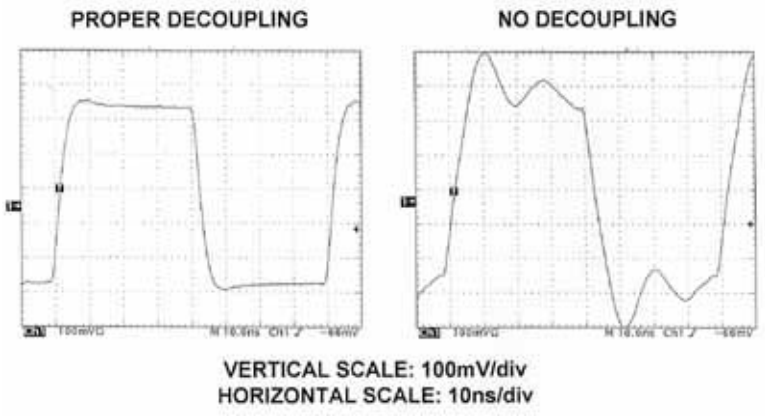

Figure 2.9

The effects of stray parasitic capacitance on the inverting input of such high speed op amps as the AD8001 is shown in Figure 2.10. In this example, 10pF was connected to the inverting input, and the overshoot and ringing increased significantly. (The AD8001 was configured in the inverting mode with a gain of –1, and the feedback and feedforward resistors were equal to 649ohms). In some cases,

low-amplitude oscillation may occur at frequencies of several hundred megahertz when there is significant stray capacitance on the inverting input. Unfortunately, you may never actually observe it unless you have a scope or spectrum analyzer which has sufficient bandwidth. Unwanted oscillations at RF frequencies will probably be rectified and averaged by devices to which the oscillating signal is applied. This is referred to as *RF rectification* and will create small unexplained dc offsets which may even be a function of moving your hand over the PC board. It is absolutely essential when building circuits using high frequency components to have high bandwidth test equipment and use it to check for oscillation at frequencies well beyond the signals of interest.

EFFECT OF 10pF STRAY INVERTING INPUT CAPACITANCE ON PULSE RESPONSE OF AD8001 OP AMP

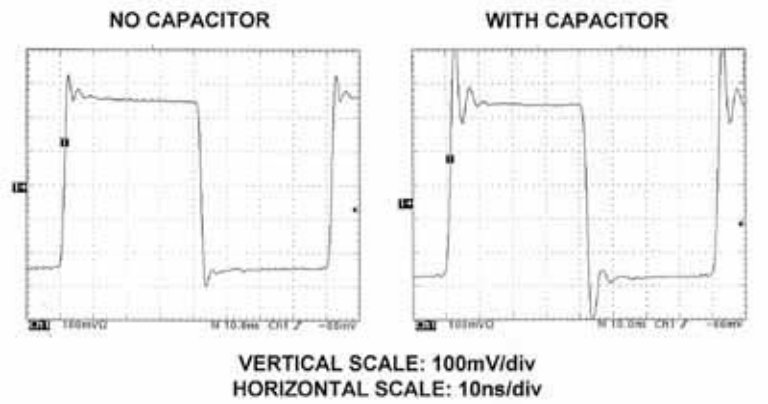

Figure 2.10

Many of these problems occur in the prototype phase due to a disregard for high frequency layout and decoupling techniques. The solutions to them lie in rigorous attention to such details as above, and those described in Chapter 9.

CABLE DRIVING

For a number of good reasons, wide bandwidth amplifier systems traditionally use transmission line interconnections, such as that shown in the basic diagram of Figure 2.11. This system uses a drive amplifier A, matched in terms of output impedance by the 75ohm source termination R_T to the transmission line connecting stages A and B. In this particular case the line is a 75ohm coax, but in general it is a wideband line matched at both ends, and can alternately be of twisted pair or stripline construction. It is followed immediately by the differential receiver circuit, B, which terminates the line with a load R_{TERM}, equal to its 75ohm impedance. The receiver stage recovers a noise-free 1V signal which is referenced to system ground B.

SINGLE-ENDED DRIVER AND DIFFERENTIAL RECEIVER

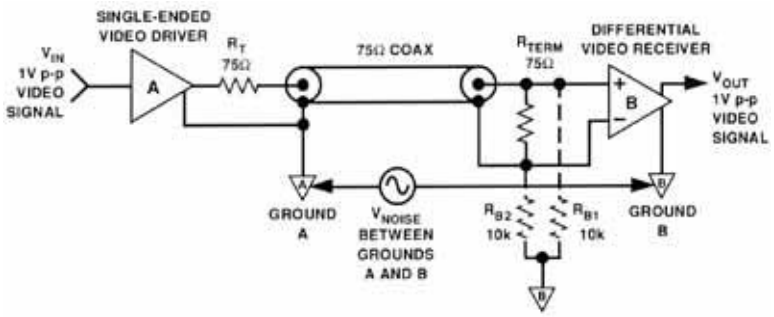

Figure 2.11

When properly implemented (i.e., the line is source and load terminated in its characteristic impedance), this system presents resistive-only loading to drive amplifier A. This factor makes it near ideal from the mutual viewpoints of amplifier stability, distortion and frequency response, as well as minimizing line reflections and associated time domain aberrations. There is an intrinsic 2/1 (6dB) signal loss associated with the line's source and load terminations, but this is easily made up by a 2x driver stage gain.

It is very important to understand that the capacitive-load compensation techniques described above are hardly the perfect solution to the line-driving problem. The most foolproof way to drive a long line (which could otherwise present a substantial capacitive load) is to use a transmission line, a standard for signal distribution in video and RF systems for years. Figure 2.12 summarizes several important cable characteristics.

CABLE CAPACITANCE

- **All Interconnections are Really Transmission Lines Which Have a Characteristic Impedance (Even if Not controlled)**
- **The Characteristic Impedance is Equal to √(L/C), where L and C are the Distributed Inductance and Capacitance**
- **Correctly Terminated Transmission Lines Have Impedances Equal to Their Characteristic Impedance**
- **Unterminated Transmission Lines Behave Approximately as Lumped Capacitance at Frequencies << $1/t_p$, where t_p = Propagation Delay of Cable**

Figure 2.12

A transmission line correctly terminated with pure resistance (no reactive component) does *not* look capacitive. It has a controlled distributed capacitance per foot (C) and a controlled distributed inductance per foot (L). The characteristic impedance of the line is given by the equation Z_O = sqrt(L/C). Coaxial cable is the

most popular form of single-ended transmission line and comes in characteristic impedances of 50ohms, 75ohms, and 93ohms.

Because of skin effect, it exhibits a loss which is a function of frequency as shown in Figure 2.13 for several popular coaxial cables (Reference 5). Skin effect also affects the pulse response of long coaxial cables. The response to a fast pulse will rise sharply for the first 50% of the output swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform risetime is 30 times greater than the 0 to 50% risetime when the cable is skin effect limited (Reference 5).

COAXIAL CABLE ATTENUATION VERSUS FREQUENCY

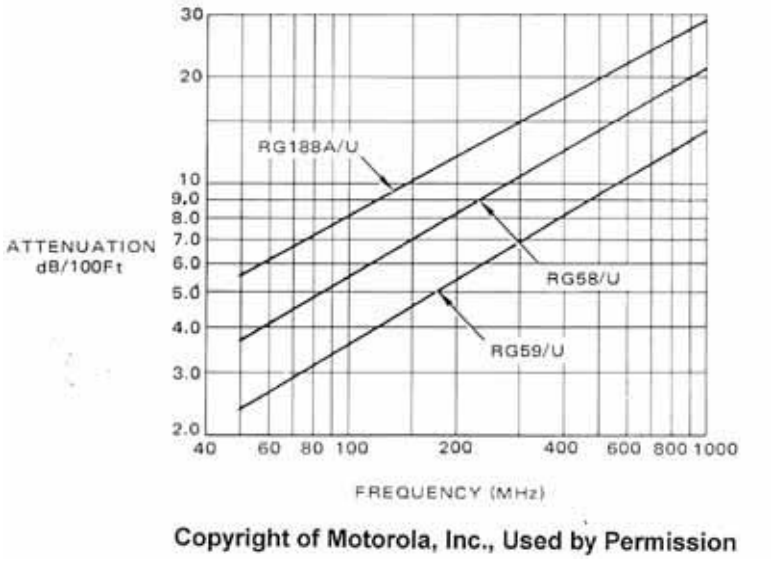

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Figure 2.13

It is useful to examine what happens for conditions of proper and improper cable source/load terminations. To illustrate the behavior of a high speed op amp driving a coaxial cable, consider the circuit of Figure 2.14. The AD8001 drives 5 feet of 50ohm coaxial cable which is load-end terminated in the characteristic impedance of 50ohms. No termination is used at the amplifier (driving) end. The pulse response is also shown in the figure.

The output of the cable was measured by connecting it directly to the 50ohm input of a 500MHz Tektronix 644A digitizing oscilloscope. The 50ohm resistor termination is actually the input of the scope. The 50ohm load is not a perfect termination (the scope input capacitance is about 10pF), so some of the pulse is reflected out of phase back to the source. When the reflection reaches the op amp output, it sees the closed-loop output impedance of the op amp which, at 100MHz, is approximately 100ohms. Thus, it is reflected back to the load with no phase reversal, accounting for the negative-going "blip" which occurs approximately 16ns after the leading edge. This is equal to the round-trip delay of the cable (2•5ft•1.6 ns/ft=16ns). In the frequency domain (not shown), the cable mismatch will cause a loss of bandwidth flatness at the load.

PULSE RESPONSE OF AD8001 DRIVING
5 FEET OF LOAD-TERMINATED 50Ω COAXIAL CABLE

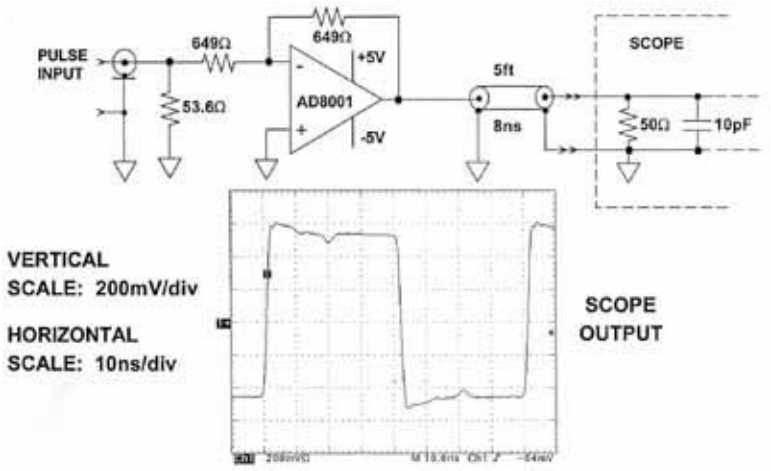


Figure 2.14

Figure 2.15 shows a second case, the results of driving the same coaxial cable, but now used with both a 50ohm source-end as well as a 50ohm load-end termination. This case is the preferred way to drive a transmission line, because a portion of the reflection from the load impedance mismatch is absorbed by the amplifier's source termination resistor. The disadvantage is that there is a 2x gain reduction, because of the voltage division between the equal value source/load terminations. However, a major positive attribute of this configuration, with matched source and load terminations in conjunction with a low-loss cable, is that the best bandwidth flatness is ensured, especially at lower operating frequencies. In addition, the amplifier is operated under near optimum loading conditions, i.e., a resistive load.

PULSE RESPONSE OF AD8001 DRIVING 5 FEET
OF SOURCE AND LOAD-TERMINATED 50Ω COAXIAL CABLE

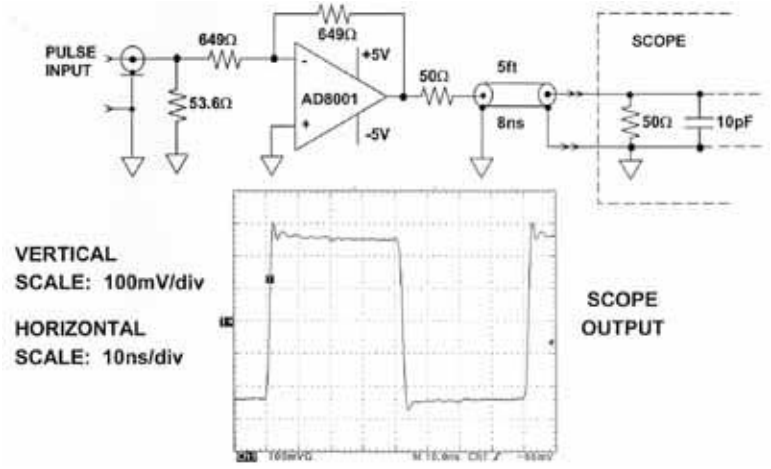


Figure 2.15

Source-end (only) terminations can also be used as shown in Figure 2.16, where the op amp is source terminated by the 50ohm resistor which drives the cable. The scope is set for 1Mohm input impedance, representing an approximate open circuit. The initial leading edge of the pulse at the op amp output sees a 100ohm load (the 50ohm source resistor in series with the 50ohm coax impedance. When the pulse reaches the load, a large portion is reflected in phase because of the high load impedance, resulting in a full-amplitude pulse at the load. When the reflection reaches the source-end of the cable, it sees the 50ohm source resistance in series with the op amp closed loop output impedance (approximately 100ohms at the frequency represented by the 2ns risetime pulse edge). The reflected portion remains in phase, and appears at the scope input as the positive-going "blip" approximately 16ns after the leading edge.

PULSE RESPONSE OF AD8001 DRIVING 5 FEET OF SOURCE-TERMINATED 50Ω COAXIAL CABLE

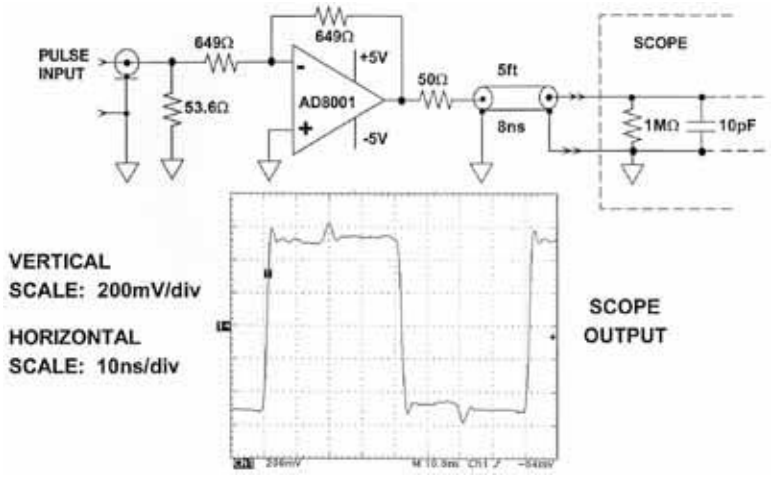


Figure 2.16

From these experiments, one can easily see that the preferred method for minimum reflections (and therefore maximum bandwidth flatness) is to use both source and load terminations and try to minimize any reactance associated with the load. The experiments represent a worst-case condition, where the frequencies contained in the fast edges are greater than 100MHz. (Using the rule-of-thumb that bandwidth = 0.35/risetime). At video frequencies, either load-only, or source-only terminations may give acceptable results, but the data sheet should always be consulted to determine the op amp's closed-loop output impedance at the maximum frequency of interest. A major disadvantage of the source-only termination is that it requires a truly high impedance load (high resistance and minimal parasitic capacitance) for minimum absorption of energy.

Now, for a truly worst case, let us replace the 5 feet of coaxial cable with an uncontrolled-impedance cable (one that is largely capacitive with little inductance). Let us use a capacitance of 150pF to simulate the cable (corresponding to the total capacitance of 5 feet of coaxial cable whose distributed capacitance is about 30pF/foot). Figure 2.17 shows the output of the AD8001 driving a lumped 160pF

capacitance (including the scope input capacitance of 10pF). Notice the overshoot and ringing on the pulse waveform due to the capacitive loading. This example illustrates the need to use good quality controlled-impedance coaxial cable in the transmission of high frequency signals.

PULSE RESPONSE OF AD8001 DRIVING 160Pf || 50Ω LOAD

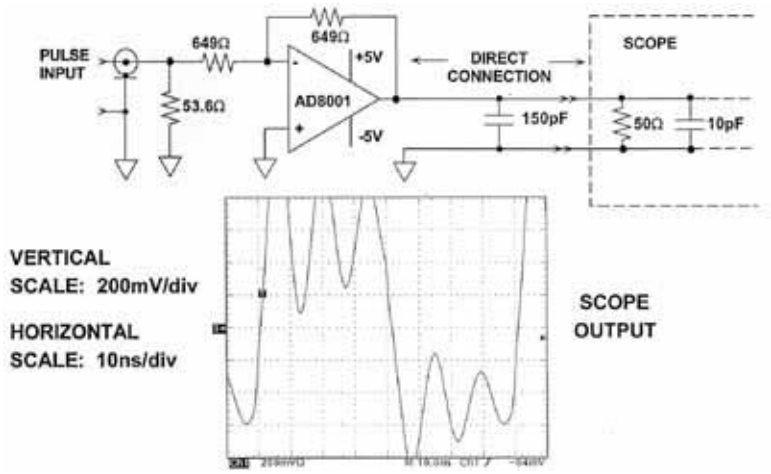


Figure 2.17

Line Drivers

The single-ended line driver function complements the receiver at the transmission end (below). This type driver is usually non-inverting, and accepts a signal from a high impedance board level source, scales it, and buffers it to drive a source matched coaxial transmission line of 50-100ohms. Typically, the driver has a gain of 2 times, which complements the 2/1 attenuation of system source/load terminations. A gain-of-two stage seems simple on the surface, but actually many factors become involved in optimizing device and power supply selection to meet overall system performance criteria. Among these are bandwidth/distortion levels versus load impedance, supply voltage/power consumption, and device type.

Fortunately, modern ICs have become more complete in their specifications, as well as more flexible in terms of supply voltage, so there is much from which to choose. For high performance in such demanding applications as wideband video, designers need a fully specified circuit environment, so that the best choice can be easy. For NTSC video systems, distortion is usually rated in terms of differential gain and differential phase, expressed as change in percentage for gain and change in degrees for phase, driving a rated load at the 3.58MHz subcarrier frequency. While traditional 3dB bandwidth is important, a more stringent specification of 0.1dB bandwidth is also often used.

VIDEO LINE DRIVER USING THE AD818 VOLTAGE FEEDBACK OP AMP HAS 50MHz BANDWIDTH (-0.1 dB)

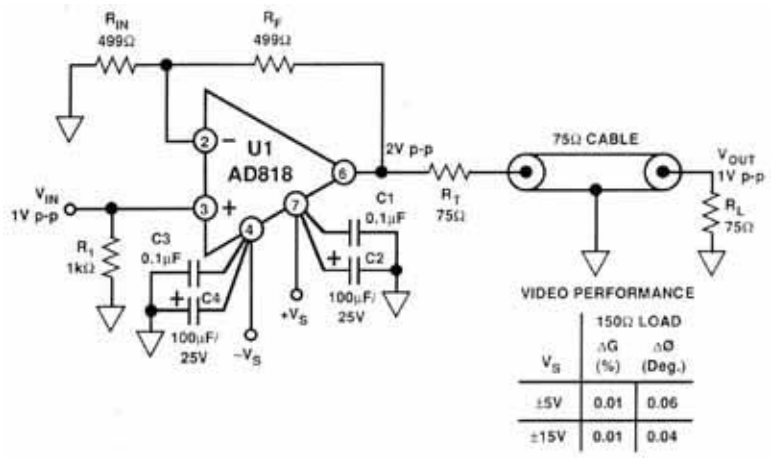


Figure 2.18

An excellent single-ended, high performance line driver meeting these guidelines is shown in Figure 2.18. Although this circuit uses inexpensive amplifiers, an AD818 (or 1/2 an AD828), it is still has excellent performance. Stage gain is set at 2 times by the equal R_1- R_2 values, which are also relatively low (500-1kohms), to minimize the feedback time constant. This voltage feedback op amp has maximum effective bandwidth when operated at G=2, and has been optimized for this specific application, thus it is able to achieve a 50MHz 0.1dB bandwidth. For highest linearity, it does not use internal capacitive load compensation. This factor, plus a high current (50mA) output stage provides the gain linearity required for high performance video, and line driving applications.

The NTSC video differential gain/phase performance of this circuit is quite good with the 150ohm loading presented by the 75ohm source termination R_T plus the 75ohm load, R_L, and is typically on the order of 0.01%/0.05° for a 2Vp-p V_{OUT} video swing while operating at ±15V. These figures do degrade for operation at V_S= ±5V, but can be maintained for supplies of ±10V or more. Thus to minimize distortion, supplies of ±10V to ±15V should be used. Other video grade op amps can also be used for U1, but illustrate the potential for distortion tradeoffs. For example, the AD817 (a similar op amp with internal cap load compensation, see above) achieves NTSC video distortion figures of 0.04%/0.08° at V_S=±15V for the same 150ohm loading.

Supply bypassing for line drivers such as this should include both local low inductance caps C1- C3, as well as larger value electrolytics, for a charge reservoir to buffer heavy load currents. Tantalum types can be used for C2 - C4, and tend to have both lower ESR and small physical size (both desirable), but the 100µF aluminum types shown can also be used. Quiescent current of this circuit is 7mA, which equates to power dissipations of 210 and 70mW for V_S=±15V and ±5V, respectively.

VIDEO LINE DRIVER USING THE AD810 CURRENT FEEDBACK OP AMP HAS DISABLE MODE, 65MHz BANDWIDTH (-3 dB) AND 20MHz BANDWIDTH (-0.1 dB)

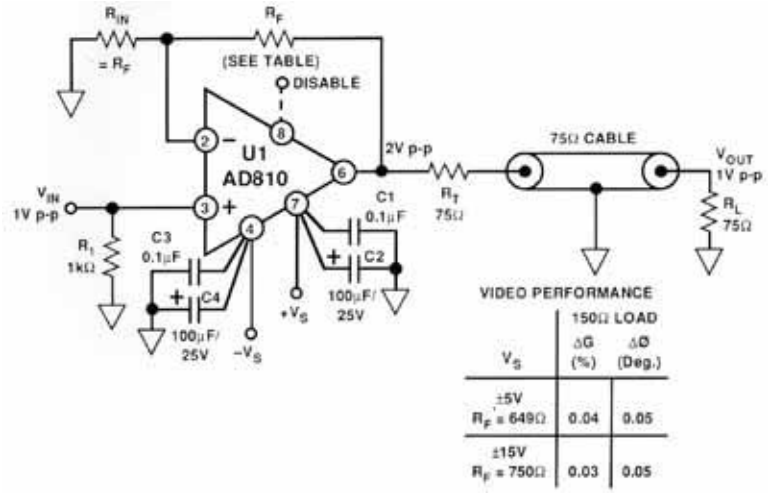


Figure 2.19

Figure 2.19 shows another high-performance video line driver using the AD810 current feedback amplifier. This circuit is also inexpensive and has higher slew rate and higher output current. The AD810 has a 3dB bandwidth of 65MHz, and a 0.1dB bandwidth of 20MHz, while the quiescent current is only 8mA.

A unique feature of the AD810 is its power-down mode. The DISABLE pin is active-low to shut the device down to a standby current drain of 2mA, with 60dB input isolation at 10MHz. This permits on/off control of a single amplifier, or "wire or-ing" the outputs of a number of devices to achieve a multiplexing function. *Note: If the AD810's disabling function is not required, then the DISABLE pin can float, and it operates conventionally.*

Note that when the AD810 is used on different power supplies, the optimum R_F will change (see table... this also will be true for other current feedback amplifiers). Other current feedback amplifiers suitable for this driver function are the single AD811, the dual AD812, and the triple AD813 (with the AD813 also featuring a DISABLE function).

VERY HIGH PERFORMANCE ±5V VIDEO LINE DRIVER/ DISTRIBUTION AMPLIFIER HAS 440MHz BANDWIDTH (-3Db) AND 110MHz BANDWIDTH (-0.1Db)

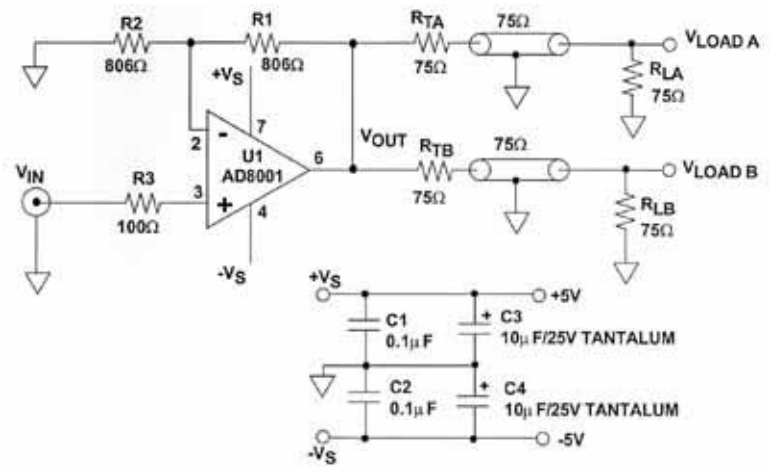


Figure 2.20

Figure 2.20 illustrates a very high performance video line driver, which has optional distribution amplifier features. This circuit uses the AD8001 current feedback amplifier as a gain-of-2 dual 75ohm line driver, generally similar to the above. Some key performance differences which set this circuit apart lie in the fact that the op amp employs a complementary UHF process. It is capable of extremely wideband response, due to the NPN/PNP f_ts of 3-5GHz. This allows higher frequency response at a lower power dissipation than the 500-600MHz f_t complementary process parts, such as the AD818 or AD810 above. The extended frequency response and lower power helps achieve low distortion at higher frequencies, while operating at a much lower quiescent power on supply voltages up to 12V.

Because the higher frequency response per mW of power, a higher output drive is possible. Here, this leads to a performance difference in that this circuit also doubles as a distribution amplifier, that is it can drive two 75ohm output lines if desired. Operated from ±5V supplies as shown, the circuit has 3dB bandwidth of 440MHz. Video distortion for differential gain/phase is 0.01%/0.025° with one line driven (R_L = 150ohms). Driving two lines (R_L = 75ohms), the differential gain errors are essentially the same, while the differential phase errors rise to about 0.07°. The 0.1dB bandwidth of this circuit is 110MHz, and the quiescent power is 50mW with the ±5V supplies. Supply bypassing should follow the same guidelines as the previous drivers, and the general physical layout should follow the RF construction techniques described above and in Chapter 9.

SINGLE-SUPPLY CONSIDERATIONS

The term *single-supply* has various implications, some of which are often further confused by marketing hype, etc. As mentioned above, there is a distinct trend toward systems which run on lower supply voltages. For high speed designs where 2Vp-p swings are often the norm, ±5V power supplies have become standard. There

are many obvious reasons for lower power dissipation, such as the ability to run without fans, reliability issues, etc. There are, therefore, many applications for single-supply ADCs other than in systems which have only one supply voltage. In many instances, the lower power drain of a single-supply ADC can be the reason for its selection, rather than the fact that it requires just one supply.

Then, there are also systems which truly operate on a single power supply. In such cases, it can often be difficult to maintain DC coupling from a source all the way to the ADC. In fact, AC coupling is quite often used in single-supply systems, with a DC restoration circuit preceding the ADC. This is necessary to prevent the loss of dynamic range which could otherwise occur, because of a need to provide maximum headroom to an AC coupled signal of arbitrary duty cycle. In the AC-coupled portions of such systems, a “false ground” is often created, usually centered between the rails.

This introduces the question of an optimum input voltage range for a single-supply ADC. At first it would seem that a zero-volt referenced input might be desirable. But in fact, this places severe constraints on the ADC driving amplifier in DC coupled systems, as it must maintain full linearity at or near 0V out. In actuality, there is no such thing as a true rail-rail output amplifier, since all output stage types will have finite saturation voltage(s) to the $+V_S$ rail or ground. Bipolar stages come the closest, and can go as low as an NPN V_{CESAT} of ground (or, a complementary PNP can go within a V_{CESAT} of the + rail). The exact saturation voltage is current dependent, and while it may be only a few mV at light currents, it can be several hundred mV for higher load currents. The traditional CMOS rail-rail output stage looks like a resistor to ground for zero-volt outputs (or to the + rail, for + outputs), so substantial load currents create proportionally higher voltage drops across these resistors, thereby limiting the output swing.

A more optimum ADC input range is thus one which includes neither ground nor the positive supply, and a range centered around $V_S/2$ is usually optimum. For example, an input range of 2Vp-p around +2.5V is bounded by +1.5V and +3.5V. A complementary common-emitter type single-supply output stage is quite capable of handling this range.

For design and process reasons however, the ADC input common-mode range may be offset from the ideal $V_S/2$ voltage midpoint. Single-supply op amps dynamic specifications such as distortion, settling time, slew rate, bandwidth, etc. are typically stated for a $V_S/2$ output bias condition. Distortion and other dynamics can degrade if the signal is offset substantially in either direction from this nominal range.

The output voltage range of an op amp is most often given for DC or low frequency output signals. Distortion may increase as the signal approaches either high or low saturation voltage limits. For instance, a +5V op amp can have a distortion specification of –60dBc for a 3Vp-p output signal. If not stated otherwise, the implication is that the signal is centered around +2.5V (or $V_S/2$), i.e., the sinewave is bounded by +1V and +4V. If the signal is offset from +2.5, distortion may very well increase.

Low distortion op amp designs typically use a complementary emitter follower output stage. This limits their output swing to slightly greater than 1 diode drop of the rails, in general more like 1V of the rails. In order to maintain low distortion at high frequencies, even more headroom may be required, reducing the available peak-to-peak swing.

The complementary common-emitter output stage allows the output to approach within V_{CESAT} of the rails. However, it does have a higher open-loop output impedance than that of the follower type of stage, and is more likely to distort when driving such non-linear loads as flash converters. When driving constant impedance loads, distortion performance can be equal to or better that the follower type of stage, but such a generalization obviously has its limitations.

The input voltage range of a single-supply op amp may also be restricted. The ability to handle zero-volt input signals can be realized by either a PNP bipolar transistor or N-channel JFET differential input stage. Including both supply rails is rarely required for high frequency signal processing. Of course, the positive rail can be included, if the op amp design uses NPN bipolars, or P-channel JFETs. For true rail-rail input capability, two amplifier input stages must operate in parallel, and the necessary bias crossover point between these stages can result in distortion and reduced CMRR. This type of input stage serves DC and lower frequency amplifiers best.

In many cases, an amplifier may be AC-specified for low voltage single-supply operation, but neither its input nor its output can actually swing very close to the rails. Such devices must use applications designed so that both the input and output common-mode restrictions are not violated. This generally involves offsetting the inputs using some sort of a false ground reference scheme.

To summarize, there are many tradeoffs involved in single-supply high speed designs. In many cases using devices specified for operation on +5V, but without true rail inclusive input/output operation, can give best available performance. As more high speed devices which are truly single-supply become available, they can be added to the designer's bag of tricks.

Direct Coupling Requires Careful Design and Controlled Levels

A design which operates on a single +5V supply with DC coupling is illustrated in Figure 2.21. This type of circuit is useful when the input signal maximum amplitude is known, and a specified output bias level is required to interface to the next stage (such as the ADC input range mentioned).

CAREFUL BIASING AND CONTROLLED LEVELS ALLOW DC COUPLING WITHIN SINGLE-SUPPLY SYSTEMS

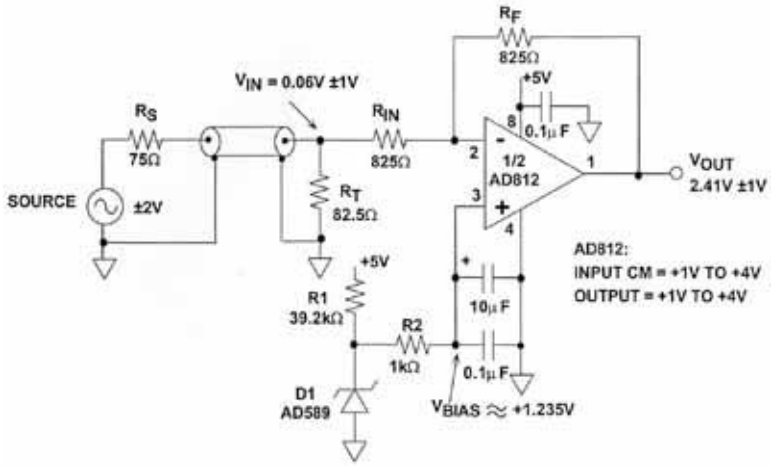


Figure 2.21

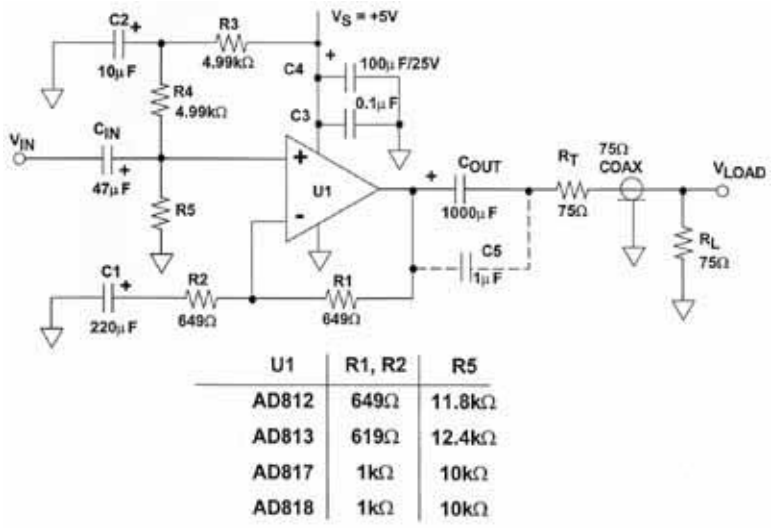
Here the source voltage is a ±2V 75ohm source, which is DC coupled and terminated by R_T. An AD812 amplifier is used, which has an input CM range of +1V to +4V (when operating on +5V), and a minimum output swing of 3Vp-p into 1kohm on 5V. It can easily swing the required 2Vp-p at the output, so there is some latitude for biasing it around an output level of $V_S/2$. For unity signal gain, equal value feedback and input resistors are used. The R_F and R_{IN} values chosen are a slight compromise to maximum bandwidth (the optimum value is 715ohms), but the input line is terminated properly at 75ohms (the parallel equivalent value of R_T and R_{IN}).

The resulting resistor values provide a gain of about 1.95 to the DC voltage applied to pin 3, V_{BIAS}. A voltage of 1.235V from a stable reference source such the AD589 will fix the static output DC level at 1.95•1.235V, or 2.41V. Because of the inverting mode signal operation, pin 2 of the op amp does not change appreciably with signal, therefore this node effectively operates at a fixed DC level, equal to V_{BIAS}. As long as this bias voltage is well above the amplifier's minimum CM range of +1V, there should be no problem. The RC network at pin 3 provides a noise filter for the diode. If a more precise output DC level is required from this stage, then V_{BIAS} can be adjusted to provide it without change to the stage's signal gain.

Single-Supply Line Drivers

By choosing a high frequency op amp which is specified for operation on low voltage supplies, single-ended line drivers can also be adapted for single 5V supply operation. An example is the 5V supply line driver circuit of Figure 2.22, which also illustrates AC coupling in single-supply design.

AC COUPLED SINGLE-SUPPLY LINE DRIVER



U1	R1, R2	R5
AD812	649Ω	11.8kΩ
AD813	619Ω	12.4kΩ
AD817	1kΩ	10kΩ
AD818	1kΩ	10kΩ

Figure 2.22

Speaking generally, this circuit can use a number of op amps, both voltage and current feedback types. The output of the AD812 and AD813 devices can swing to within about 1V of either rail, allowing 3Vp-p outputs to be delivered into 150ohm loads on 5V. While bandwidth of these current feedback amplifiers does reduces with low voltage operation, they are still capable of a small signal 0.1dB bandwidth on the order of 10MHz, and good differential gain/phase performance, about 0.07%/0.06°, quite good for a simple circuit. The AD817 and AD818 are not as clean in performance, and not necessarily recommended for 5V line drivers, but are included as examples of more general purpose voltage feedback types operable on 5V. For optimizing the bias and bandwidth of any of these amplifiers, use the resistor values from the table.

As would be expected, headroom is critical on such low supplies, so if nothing else, biasing should be optimized for the voltage in use, via the R5 value as noted. R3 and R4 are equal values, AC bypassed for minimum noise coupling from the supply line. All input and output coupling capacitors are large in value, and are so chosen for a minimum of low frequency phase shift, for composite video uses. They can be reduced for applications with higher low frequency cutoffs. C_{OUT} is potentially a problem in the large value shown, as large electrolytics can be inductive. C5, a non-critical optional low inductance shunt, can minimize this problem.

Obviously, the stage cannot be driven beyond 3Vp-p at V_{OUT} without distortion, so operating levels need to maintained conservatively below this. The next section discusses AC coupling issues and headroom in more detail.

The AC coupling of arbitrary waveforms can actually introduce problems which don't exist at all in DC coupled or DC restored systems. These problems have to do with

the waveform duty cycle, and are particularly acute with signals which approach the rails, as they can in low supply voltage systems which are AC coupled.

In an amplifier circuit such as that of Figure 2.22, the output bias point will be equal to the DC bias as applied to the op amp's (+) input. For a symmetric (50% duty cycle) waveform of a 2Vp-p output level , the output signal will swing symmetrically about the bias point, or nominally 2.5V ±1V. If however the pulsed waveform is of a very high (or low) duty cycle, the AC averaging effect of C_{IN} and R4||R5 will shift the effective peak level either high or low, dependent upon the duty cycle. This phenomenon has the net effect of reducing the working headroom of the amplifier, and is illustrated in Figure 2.23.

WAVEFORM DUTY CYCLE TAXES
HEADROOM IN AC COUPLED AMPLIFIERS

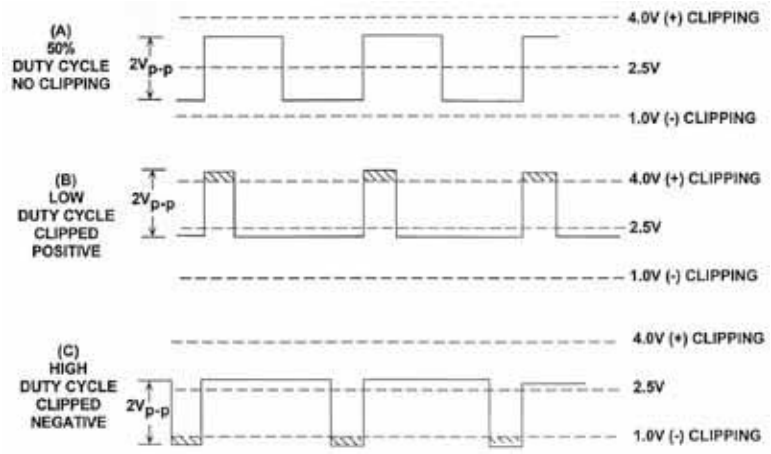


Figure 2.23

In Figure 2.23 (A), an example of a 50% duty cycle square wave of about 2Vp-p level is shown, with the signal swing biased symmetrically between the upper and lower clip points of a 5V supply amplifier. This amplifier, for example, (an AD817 biased similarly to Figure 2.22) can only swing to the limited DC levels as marked, about 1V from either rail. In cases (B) and (C), the duty cycle of the input waveform is adjusted to both low and high duty cycle extremes *while maintaining the same peak-to-peak input level*. At the amplifier output, the waveform is seen to clip either negative or positive, in (B) and (C), respectively.

Since standard video waveforms *do* vary in duty cycle as the scene changes, the point is made that low distortion operation on AC coupled single supply stages must take the duty cycle headroom degradation effect into account. If a stage has a 3Vp-p output swing available before clipping, and it must cleanly reproduce an arbitrary waveform, then the maximum allowable amplitude is less than 1/2 of this 3Vp-p swing, that is <1.5Vp-p. An example of violating this criteria is contained the 2Vp-p waveform of Figure 2.23, which is clipping for both the high and low duty cycles. Note that the criteria set down above is based on avoiding hard clipping, while subtle distortion increases may in fact take place at lower levels. This suggests an

even more conservative criteria for lowest distortion operation such as composite NTSC video amplifiers.

Of course, amplifiers designed with rail-rail outputs and low distortion in mind address these problems most directly. One such device is the AD8041, an XFCB single-supply op amp designed for video applications, and summarized briefly by Figure 2.24. As these data show, this part is designed to provide low NTSC video distortion while driving a single 75ohm source terminated load (in a circuit such as Figure 2.22).

RAIL-RAIL OUTPUT VIDEO OP AMPS ALLOW LOW DISTORTION OUTPUT AND GREATEST FLEXIBILITY

Typical specifications for AD8041 op amp @ V_s = +5V, T_A = 25°C

- **Common Mode Range: -0.2V to +4V**
- **Offset Voltage: 2mV**
- **Bias Current: 1.2μA**
- **Bandwidth: 80MHz**
- **Slew Rate: 160V/μs**
- **Differential Gain/Phase: 0.03%/ 0.03°**
- **(V_{out} = 2Vp-p, R_L=150Ω)**
- **Output Current: 50mA (0.5V from rails)**
- **Quiescent Current: 5mA**
- **Disable Feature Allows Multiplexing**

Figure 2.24

APPLICATION CIRCUITS

A common video circuit requirement is the multiplexer, a stage which selects one of "N" video inputs, and transmits a buffered version of the selected signal to an output transmission line. Video amplifiers which can operate internally in a switched mode, such as the AD810 and AD813, allow this operation to be performed directly in the video signal path with no additional hardware. This feature is activated with the use of the device's *disable* pin, which when pulled low, disables the amplifier and drops power to a low state. The AD810 is a single channel current feedback amplifier with this disable feature, while the AD813 offers similar functionality, in a 14 pin, three channel format. The high performance of the AD813 on low voltages allows it to achieve high performance on ±5V supplies, and to be directly interfaced with standard 5V logic drivers.

2:1 Video Multiplexer

The outputs of two AD810s can be wired together to form a 2:1 multiplexer without degrading the flatness of the gain response. Figure 2.25 shows a recommended configuration, which results in a 0.1dB bandwidth of 20MHz and OFF channel isolation of 77dB at 10MHz on ±5V supplies. The time to switch between channels is about 750ns when the disable pins are driven by open drain output logic. With the use of the recommended 74HC04 as shown, the switching time is about 180ns. The switching time is only slightly affected by the signal level.

A 2:1 VIDEO MULTIPLEXER USING AD810s HAS -0.1dB BANDWIDTH OF 20MHz AND SWITCHES IN 180ns

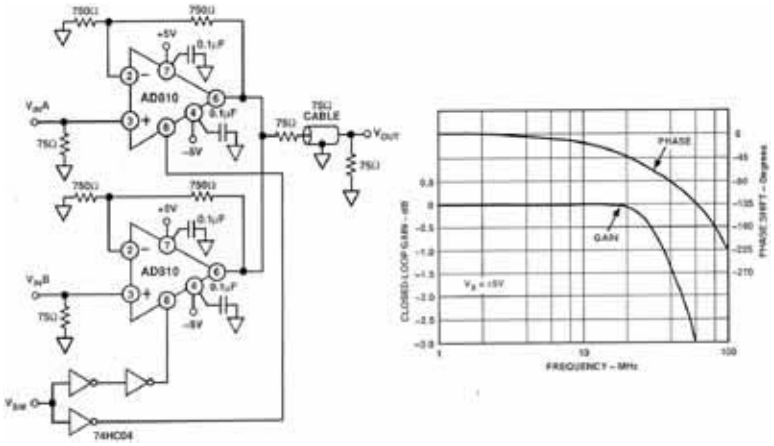


Figure 2.25

3:1 Video Multiplexer

A 3:1 video multiplexer circuit using the triple AD813 is shown in Figure 2.26, and features relative simplicity and high performance while operating from ±5V power supplies. The 3 standard 1Vp-p video input signals V_{IN1} - V_{IN3} drive the 3 channels of the AD813, one of which is ON at a given moment. If say channel 1 is selected, amplifier section 1 is enabled, by virtue of a logic HIGH signal on the SELECT1 line driving the ENABLE input of the first amplifier. The remaining two amplifier channels appear as open circuits looking back into them, but their feedback networks do appear as a load to the active channel. Control logic decoding is provided by U2, a 74HC238 1 of 8 logic decoder. The control lines A0 and A1 are decoded as per the truth table, which provides selection between the 3 input signals and OFF, as noted.

3:1 VIDEO MULTIPLEXER USING AD813 TRIPLE OP AMP

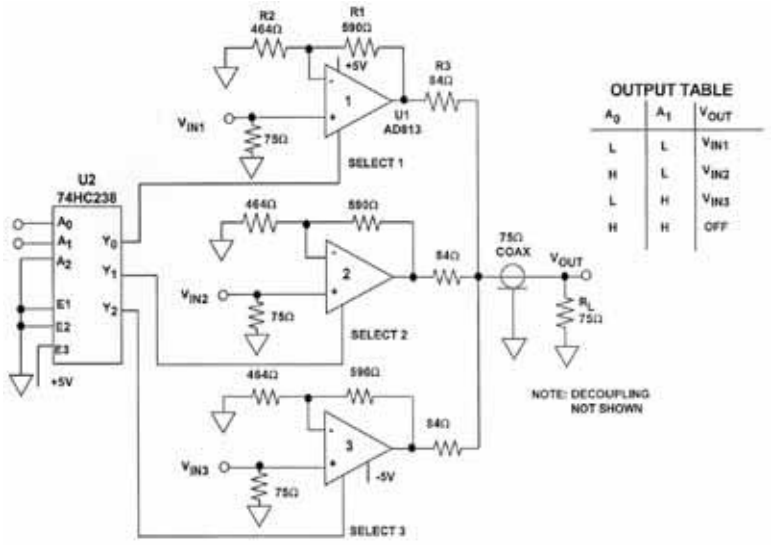
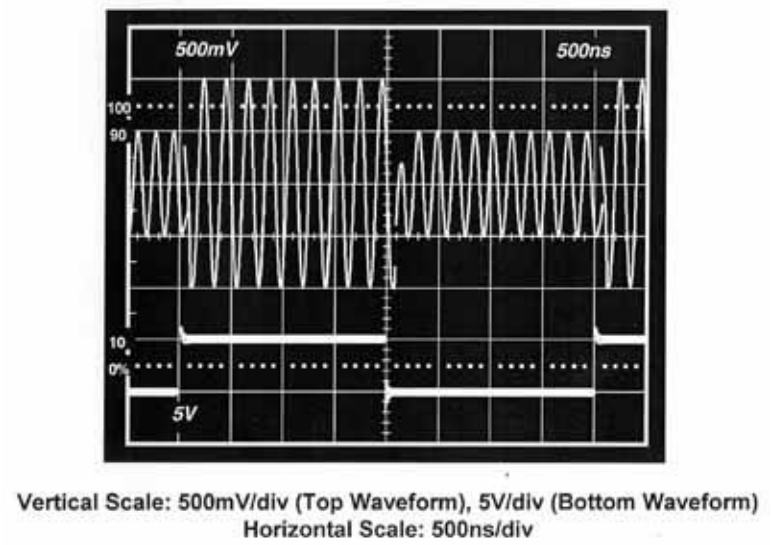


Figure 2.26

Some design subtleties of the circuit come about because of necessity to account for several design criteria. One is the 590ohm value of feedback resistor R1, to provide optimum response to the AD813 current feedback amplifier; another is the parasitic loading of the two unused gain resistor networks; a third is the source termination of the line, 75ohms in this case. While any given channel is ON, it drives not only load resistor R_L, but also the net dummy resistance $R_X/2$, where R_X is an equivalent series resistance equal to R1 + R2 + R3. To provide a net overall gain of unity plus and effective 75ohm source impedance, this sets the resistance values of R1 + R2 + R3 as shown.

SWITCHING CHARACTERISTICS OF 3:1 VIDEO MULTIPLEXER



Vertical Scale: 500mV/div (Top Waveform), 5V/div (Bottom Waveform)
Horizontal Scale: 500ns/div

Figure 2.27

Performance of the circuit is excellent, with 0.1dB bandwidth of 20MHz, and an OFF state isolation of 60dB at 10MHz. Switching time is about 180ns, and is shown in Figure 2.27 switching between two different inputs (top trace) with the control input also shown (bottom trace).

Video Programmable Gain Amplifier

Closely related to the 3:1 multiplexer of Figure 2.26 is a programmable gain video amplifier, or PGA, as shown in Figure 2.28. With a similarly configured 2 line digital control input, this circuit can be set up to provide 3 different gain settings. This makes it a useful tool in various systems which can employ signal normalization or gain ranging prior to A/D conversion, such as CCD systems, ultrasound, etc. The gains can be binary related as here, or they can be arbitrary. An extremely useful feature of the AD813 current feedback amplifier to this application is the fact that the bandwidth does not reduce in inverse proportion, as gain is increased. Instead, it stays relatively constant as gain is raised. Thus more useful bandwidth is available at the higher programmed gains than would be true for a fixed gain-bandwidth product amplifier type.

GAIN OF 1, 2, 4 PROGRAMMABLE GAIN VIDEO AMPLIFIER

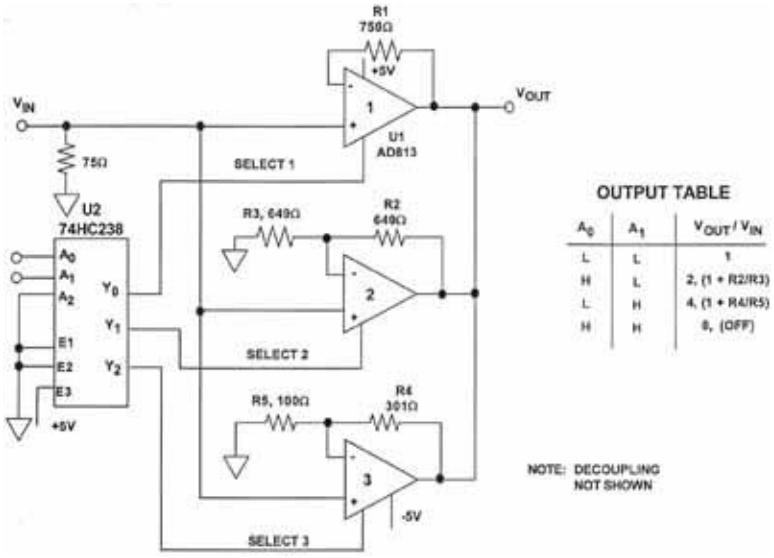


Figure 2.28

In the circuit, channel 1 of the AD813 is a unity gain channel, channel 2 has a gain of 2, and channel 3 a gain of 4, while the fourth control state is OFF. As is indicated by the table, these gains can varied by adjustment of the R2/R3 or R4/R5 ratios. For the gain range and values shown, the PGA will be able to maintain a 3dB bandwidth of about 50MHz or more for loading as shown (a high impedance load of 1kohm or more is assumed). Fine tuning of the bandwidth for a given gain setting can be accomplished by tweaking the absolute values of the feedback resistors (most applicable at higher gains).

Differential Drivers

Many applications require gain/phase matched complementary or differential signals. Among these are analog-digital-converter (ADC) input buffers, where differential operation can provide lower levels of 2nd harmonic distortion for certain converters. Other uses include high frequency bridge excitation, and drivers for balanced transmission twisted pair lines such as UTP-5. While various topologies can be employed to derive differential drive signals, many circuit details as well as the topologies themselves are important as to how accurate two outputs can be maintained.

Inverter-Follower Differential Driver

The circuit of Figure 2.29 is useful as a high speed differential driver for driving high speed 10-12 bit ADCs, differential video lines, and other balanced loads at levels of 1-4Vrms. As shown it operates from ±5V supplies, but it can also be adapted to supplies in the range of ±5 to ±15V. When operated directly from ±5V as here, it

minimizes potential for destructive ADC overdrive when higher supply voltage buffers drive a ±5V powered ADC, in addition to minimizing driver power.

DIFFERENTIAL DRIVER USING INVERTER/FOLLOWER

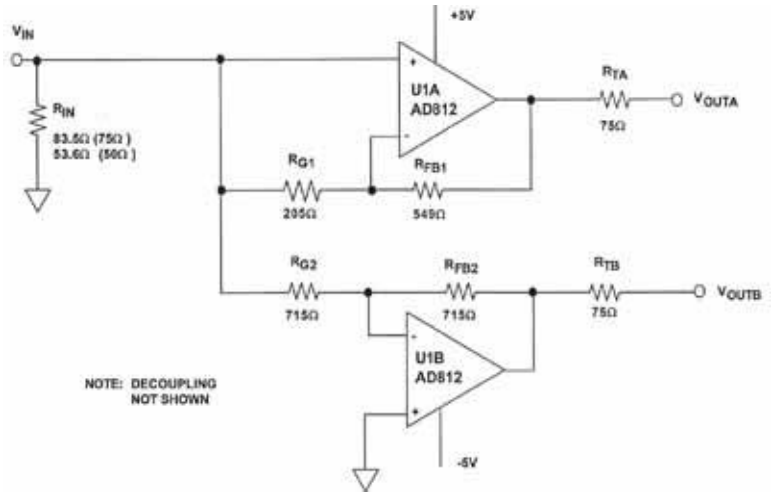


Figure 2.29

In many of these differential drivers the performance criteria is high. In addition to low output distortion, the two signals should maintain gain/phase flatness. In this driver, two sections of an AD812 dual current feedback amplifier are used for the channel A & B buffers, U1A & U1B. This measure can provide inherently better open-loop bandwidth matching than will the use of two individual same part number singles (where bandwidth varies between devices from different manufacturing lots).

The two buffers here operate with precise gains of ±1, as defined by their respective feedback and input resistances. Channel B buffer U1B is conventional, and uses a matched pair of 715ohm resistors- the value for using the AD812 on ±5V supplies.

In channel A, non-inverting buffer U1A has an inherent signal gain of 1, by virtue of the bootstrapped feedback network R_{FB1} and R_{G1}(Reference 5). It also has a higher noise gain, for phase matching. Normally a current feedback amplifier operating as a simple unity gain follower would use one (optimum) resistor R_{FB1}, and no gain resistor at all. Here, with input resistor R_{G1} added, a U1A noise gain like that of U1B results. Due to the bootstrap connection of R_{FB1}-R_{G1}, the signal gain is maintained at unity. Given the matched open loop bandwidths of U1A and U1B, similar noise gains in the A-B channels provide closely matched output bandwidths between the driver sides, a distinction which greatly impacts overall matching performance.

In setting up a design for the driver, the effects of resistor gain errors should be considered for R_{G2}-R_{FB2}. Here a worst case 2% mis-match will result in less than 0.2dB gain error between channels A and B. This error can be improved simply by specifying tighter resistor ratio matching, avoiding trimming.

If desired, phase matching is trimmed via R_{G1}, so that the phase of channel A closely matches that of B. This can be done for new circuit conditions, by using a pair of closely matched (0.1% or better) resistors to sum the A and B channels, as R_{G1} is adjusted for the best null conditions at the sum node. The A-B gain/phase matching is quite effective in this driver, with test results of the circuit as shown 0.04dB and 0.1° between the A and B output signals at 10MHz, when operated into dual 150ohm loads. The 3dB bandwidth of the driver is about 60MHz.

Net input impedance of the circuit is set to a standard line termination value such as 75ohms (or 50ohms), by choosing R_{IN} so that the desired value results with R_{IN} in parallel with R_{G2}. In this example, an R_{IN} value of 83.5ohms provides a standard input impedance of 75ohms when paralleled with 715ohms. For the circuit just as shown, dual voltage feedback amplifier types with sufficiently high speed and low distortion can also be used. This allows greater freedom with regard to resistor values using such devices as the AD826 and AD828.

Gain of the circuit can be changed if desired, but this is not totally straightforward. An easy step to satisfy diverse gain requirements is to simply use a triple amplifier such as the AD813, with the third channel as a variable gain input buffer.

CROSS-COUPLED DIFFERENTIAL DRIVER
PROVIDES BALANCED OUTPUTS AND 250MHz BANDWIDTH

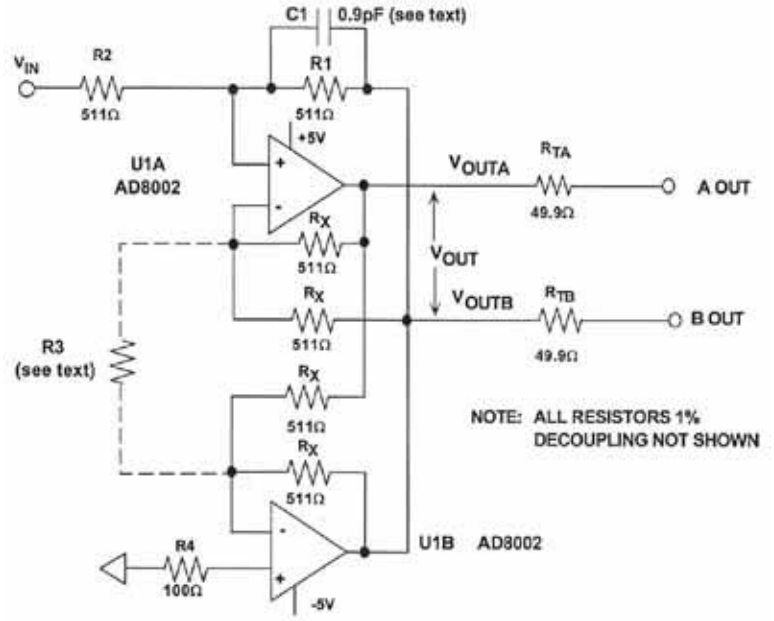


Figure 2.30

Cross-Coupled Differential Driver

Another differential driver approach uses cross-coupled feedback to get very high CMR and complementary outputs at the same time. In Figure 2.30, by connecting AD8002 dual current feedback amplifier sections as cross-coupled inverters, their outputs are forced equal and opposite, assuring zero output common mode voltage.

The gain cell which results, U1A and U1B plus cross-coupling resistances R_X, is fundamentally a differential input and output topology, but it behaves as a voltage feedback amplifier with regard to the feedback port at the U1A (+) node. The gain of the stage from V_{IN} to V_{OUT} is:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2R1}{R2}$$

where V_{OUT} is the differential output, equal to $V_{OUTA} - V_{OUTB}$.

This circuit has some unique benefits. First, differential gain is set by a single resistor ratio, so there is no necessity for side-side resistor matching with gain changes, as is the case for conventional differential amplifiers (see line receivers, below). Second, because the (overall) circuit emulates a voltage feedback amplifier, these gain resistances are not as restrictive as is true in the case of a conventional current feedback amplifier. Thus they are not highly critical as to absolute value. This is unlike standard applications using current feedback amplifiers, and will be true as long as the equivalent resistance seen by U1A is reasonably low (less than 1kohm in this case). Third, the cell bandwidth can be optimized to the desired gain by a single optional resistor, R3, as follows. If for instance, a net gain of 20 is desired (R1/R2=10), the bandwidth would otherwise be reduced by roughly this amount, since without R3 the cell operates with a constant gain-bandwidth product. With R3 present however, advantage can be taken of the AD8002 current feedback amplifier characteristics. Additional internal gain is added by the connection of R3, which, given an appropriate value, effectively raises gain-bandwidth to a level so as to restore the bandwidth which would otherwise be lost by the higher closed loop gain.

In the circuit as shown, no R3 is necessary at the low working gain of 2 times differential, since the 511ohm R_X resistors are already optimized for maximum bandwidth. Note that these four matched resistances are somewhat critical, and will change in absolute value with the use of another current feedback amplifier. At higher gain closed loop gains as set by R1/R2, R3 can be chosen to optimize the working transconductance in the input stages of U1A and U1B, as follows:

$$R3 \quad \frac{Rx}{(R1 / R2) - 1}$$

As in any high speed inverting feedback amplifier, a small high-Q chip type feedback capacitance, C1, may be needed to optimize flatness of frequency response. In this example, a 0.9pF value was found optimum for minimizing peaking. In general, provision should be made on the PC layout for an NPO chip capacitor in the range of 0.5-2pF. This capacitor is then value selected at board characterization for optimum frequency response.

FREQUENCY RESPONSE OF AD8002 CROSS-COUPLED DRIVER IS > 250MHz (C1 = 0.9pF ± 0.1pF)

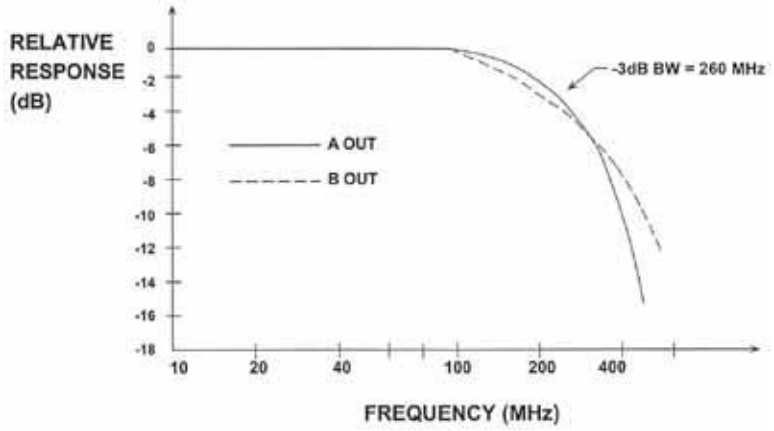


Figure 2.31

For the dual trace, 1-500MHz swept frequency response plot of Figure 2.31, output levels were 0dBm into matched 50ohm loads, through back termination resistances R_{TA} and R_{TB}, at V_{OUTA} and V_{OUTB}. In this plot the vertical scale is 2dB/div, and it shows the 3dB bandwidth of the driver measuring about 250MHz, with peaking about 0.1dB. The four R_X resistors along with R_{TA} and R_{TB} control low frequency amplitude matching, which was within 0.1dB in the lab tests, using 511ohm 1% resistor types. For tightest amplitude matching, these resistor ratios can be more closely controlled.

Due to the high gain-bandwidths involved with the AD8002, the construction of this circuit should follow RF rules, with the use of a ground plane, chip bypass capacitors of zero lead length at the ±5V supply pins, and surface mount resistors for lowest inductance.

Differential Receivers

Another standard system application is the line receiver function, a stage which accepts signals from a single-ended (or differential) transmission line, and converts them into a buffered version for local processing (referring back to the system diagram of Figure 2.11). In a typical system, there is a single ended driving signal V_{IN} at the origination point, a coaxial transmission line with the signal terminated in the characteristic line impedance at the local end, and finally, a differential input receiver. The system operates the same in principle for standard impedances of 50-100ohms, as long as the source and load impedances match that of the line, under which conditions bandwidth is maximized. In the receiver, input impedance is assumed high in relation to line impedance, and high common-mode rejection (CMR) allows rejection of spurious noise appearing between driver/receiver grounds. Noise is rejected in proportion to the CMR of the receiver amplifier, and typical CMR performance goal for such a stage is 60-70dB or better for frequencies up to 10MHz.

Functionally, this system delivers at the output of the receiver stage a signal V_{OUT}, a replica of the original driving signal V_{IN}. The receiver may also scale the received signal, and may also be called on to drive another transmission line. Critical performance parameters for the receiver are signal bandwidth and distortion specifications. For line receivers, video distortion is rated in terms of differential gain and differential phase at the 3.58 MHz subcarrier frequency.

4 Resistor Differential Line Receiver

Figure 2.32 shows a low cost, medium performance line receiver using a high speed op amp rated for video use. It is actually a standard 4 resistor instrumentation amplifier optimized for high speed, with a differential to single-ended gain of R2/R1. Using low value, DC accurate/AC trimmed resistances for R1-R4 and a high speed, high CMR op amp provides the good performance. Practically speaking however, at low frequencies resistor matching can be more critical to overall CMR than the rated CMR of the op amp. For example, the worst case CMR (in dB) of this circuit due to resistor effects is:

$$CMR = 20\log_{10}\left(\frac{1 + \frac{R2}{R1}}{4Kr}\right)$$

In this expression the term “Kr” is a single resistor tolerance in fractional form (1%=0.01, etc.), and it is assumed the amplifier has significantly higher CMR (greater than 100dB). Using discrete 1% metal films for R1/R2 and R3/R4 yields a worst case CMR of 34dB, 0.1% types 54dB, etc. Of course 4 random 1% resistors will on the average yield a CMR better than 34dB, but not dramatically so. A single substrate dual matched pair thin film network is preferred, for reasons of best noise rejection and simplicity. One type suitable is the Ohmtek 1005, (Reference 6) which has a ratio match of 0.1%, which will provide a worst case low frequency CMR of 66dB.

SIMPLE VIDEO LINE RECEIVER USING THE AD818 OP AMP

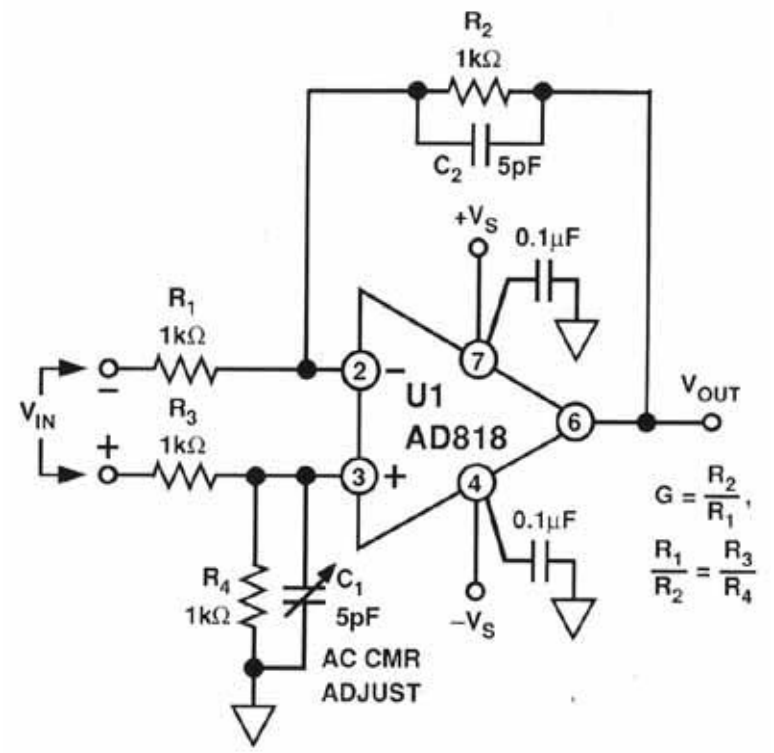


Figure 2.32

This circuit has an interesting and desirable side property. Because of the resistors it divides down the input voltage, and the amplifier is protected against overvoltage. This allows CM voltages to exceed ±5V supply rails in some cases without hazard. Operation at ±15V should constrain the inputs within the rails.

At frequencies above 1MHz, the bridge balance is dominated by AC effects, and a C1-C2 capacitive balance trim should be used for best performance. The C1 adjustment is intended to allow this, providing for the cancellation of stray layout capacitance(s) by electrically matching the net C1-C2 values. In a given PC layout with low and stable parasitic capacitance, C1 is best adjusted once in 0.5pF increments, for best high frequency CMR. Using designated PC pads, production values then would use the trimmed value. Good AC matching is essential to achieving good CMR at high frequencies. C1-C2 should be types similar physically, such as NPO (or other stable) ceramic chip style capacitors.

While the circuit as shown has unity gain, it can be gain-scaled in discrete steps, as long as the noted resistor ratios are maintained. In practice, this means using taps on a multi-ratio network for gain change, so as to raise both R2 and R4, in identical proportions. There is no other simple way to change gain in this receiver circuit. Alternately, a scheme for continuous gain control without interaction with CMR is to follow this receiver with a scaling amplifier/driver with adjustable gain. The similar AD828 dual amplifier allows this with the addition of only two resistors.

Video gain/phase performance of this stage is dependent upon the device is used for U1 and the operating supply voltages. Suitable voltage feedback amplifiers work best at supplies of ±10 - ±15V, which maximizes op amp bandwidth. And, while many high speed amplifiers function in this circuit, those expressly designed with low distortion video operation perform best. The circuit as shown can be used with supplies of ±5 to ±15V, but lowest NTSC video distortion occurs for supplies of ±10V or more, where differential gain/differential phase errors are less than 0.01%/0.05°. Operating at ±5V the distortion rises somewhat, but the lowest power drain of 70mW occurs.

One drawback to this circuit is that it does load a 75ohm video line to some extent, and so should be used with this loading taken into account. On the plus side, it has wide dynamic range for both signal and CM voltages, plus the inherent overvoltage protection.

Active Feedback Differential Line Receiver

Fully integrating the line receiver function eliminates the resistor-related drawbacks of the 4 resistor line receiver, improving CMR performance, ease of use, and overall circuit flexibility. An IC designed for this function is the AD830 active feedback amplifier (Reference 7,8). Its use as a differential line receiver with gain is illustrated in Figure 2.33.

VIDEO LOOP-THROUGH CONNECTION USING THE AD830

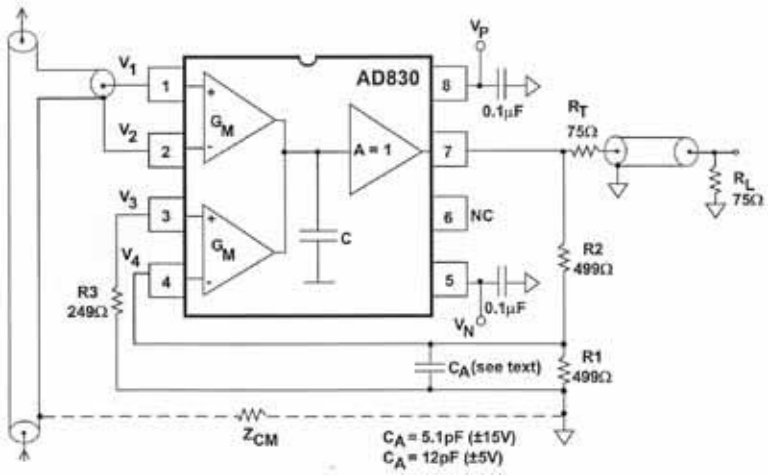


Figure 2.33

The AD830 operates as a feedback amplifier with two sets of fully differential inputs, available at pins 1-2 and 3-4, respectively. Internally, the outputs of the two stages are summed and drive a buffer output stage. Both input stages have high CMR, and can handle differential signals up to ±2V, and CM voltages can range up to $-V_S+3V$ or $+V_S-2.1V$, with a ±1V differential input applied. While the AD830 does not normally need protection against CM voltages, if sustained transient voltage beyond the rails is encountered, an optional pair of equal value (approximately 200ohms) resistances can be used in series with pins 1-2.

In this device the overall feedback loop operates so that the differential voltages V_{1-2} and V_{3-4} are forced to be equal. Feedback is taken from the output back to one input differential pair, while the other pair is driven by a differential input signal. An important point of this architecture is that high CM rejection is provided by the two differential input pairs, so CMR isn't dependent on resistor bridges and their associated matching problems. The inherently wideband balanced circuit and the quasi-floating operation of the driven input provide the high CMR, which is typically 100dB at DC.

The general expression for the U1 stage's gain "G" is like a non-inverting op amp, or:

$$G = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R2}{R1}$$

For lowest DC offset, balancing resistor R3 is used (equal to R1 | | R2).

In this example of a video "loop-through" connection, the input signal tapped from a coax line and applied to one input stage at pins 1-2, with the scaled output signal tied to the second input stage between pins 3-4. With the R1-R4 feedback attenuation of 2/1, the net result is that the output of U1, is then equal to $2 \cdot V_{IN}$, i.e., a gain of 2.

Functionally, the input and local grounds are isolated by the CMR of the AD830, which is typically 75dB at frequencies below 1MHz, 60dB at 4.43MHz, and relatively supply independent.

With the addition of an output source termination resistor R_T, this circuit has an overall loaded gain of unity at the load termination, R_L. It is a ground isolating video repeater, driving the terminated 75ohm output line, delivering a final output equal to the original input, V_{IN}.

NTSC video performance will be dependent upon supplies. Driving a terminated line as shown, the circuit has optimum video distortion levels for V_S ±15V, where differential gain is typically 0.06%, and differential phase 0.08°. Bandwidth can be optimized by the optional 5.1pF (or 12pF) capacitor, C_A, which allows a 0.1dB bandwidth of 10MHz with ±15V operation. The differential gain and phase errors deteriorate about 2 or more times at ±5V.

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