# SECTION 3

# HIGH RESOLUTION SIGNAL CONDITIONING ADCs

- Sigma-Delta ADCs
- High Resolution, Low Frequency Measurement ADCs

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# HIGH RESOLUTION SIGNAL CONDITIONING ADCs

*Walt Kester, James Bryant, Joe Buxton*

The trend in ADCs and DACs is toward higher speeds and higher resolutions at reduced power levels. Modern data converters generally operate on ±5V (dual supply) or +5V (single supply). There are now a few converters which operate on a single +3V supply. This trend has created a number of design and applications problems which were much less important in earlier data converters, where ±15V supplies were the standard.

Lower supply voltages imply smaller input voltage ranges, and hence more susceptibility to noise from all potential sources: power supplies, references, digital signals, EMI/RFI, and probably most important, improper layout, grounding, and decoupling techniques. Single-supply ADCs often have an input range which is not referenced to ground. Finding compatible single-supply drive amplifiers and dealing with level shifting of the input signal in direct-coupled applications also becomes a challenge.

In spite of these issues, components are now available which allow extremely high resolutions at low supply voltages and low power. This section discusses the applications problems associated with such components and shows techniques for successfully designing them into systems.

**LOW POWER, LOW VOLTAGE ADC DESIGN ISSUES**

- **Low Power ADCs typically run on ±5V, +5V, +5/+3V, or +3V**
- **Lower Signal Swings Increase Sensitivity to All Types of Noise (Device, Power Supply, Logic, etc.)**
- **Device Noise Increases at Low Quiescent Currents**
- **Bandwidth Suffers as Supply Current Drops**
- **Input Common-Mode Range May be Limited**
- **Selection of Zero-Volt Input/Output Amplifiers is Limited**
- **Auto-Calibration Modes Highly Desirable at High Resolutions**

**Figure 3.1**

# SIGMA-DELTA ADCS (COURTESY OF JAMES M. BRYANT)

Because Sigma-Delta is such an important and popular architecture for high resolution (16 to 24 bits) ADCs, the section begins with a basic description of this type of converter.

Sigma-Delta Analog-Digital Converters have been known for nearly thirty years, but only recently has the technology (high-density digital VLSI) existed to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low-cost, low-bandwidth, low-power, high-resolution ADC is required.

There have been innumerable descriptions of the architecture and theory of Sigma-Delta ADCs, but most commence with a maze of integrals and deteriorate from there. In the Applications Department at Analog Devices, we frequently encounter engineers who do not understand the theory of operation of Sigma-Delta ADCs and are convinced, from study of a typical published article, that it is too complex to comprehend easily.

There is nothing particularly difficult to understand about Sigma-Delta ADCs, as long as you avoid the detailed mathematics, and this section has been written in an attempt to clarify the subject. A Sigma-Delta ADC contains very simple analog electronics (a comparator, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low pass filter). It is not necessary to know precisely how the filter works to appreciate what it does. To understand how a Sigma-Delta ADC works one should be familiar with the concepts of *over-sampling, noise shaping, digital filtering.* and *decimation*.

**SIGMA-DELTA (Σ-Δ) ADCs**

- **Sigma-Delta ADCs are low-cost and have high resolution, excellent DNL, low-power, although limited input bandwidth**
- **A Σ-Δ ADC is Simple**
- **The Mathematics, however is Complex**
- **This section Concentrates on What Actually Happens!**

**Figure 3.2**

## SIGMA-DELTA ADC KEY CONCEPTS

- **Oversampling**
- **Noise Shaping**
- **Digital Filtering**
- **Decimation**

**Figure 3.3**

An ADC is a circuit whose digital output is proportional to the ratio of its analog input to its analog reference. Often, but by no means always, the scaling factor between the analog reference and the analog signal is unity, so the digital signal represents the normalized ratio of the two.

Figure 3.4 shows the transfer characteristic of an ideal 3-bit unipolar ADC. The input to an ADC is analog and is not quantized, but its output is quantized. The transfer characteristic therefore consists of eight horizontal steps (when considering the offset, gain and linearity of an ADC we consider the line joining the midpoints of these steps).

**TRANSFER CHARACTERISTIC OF AN IDEAL 3-BIT UNIPOLAR ADC**

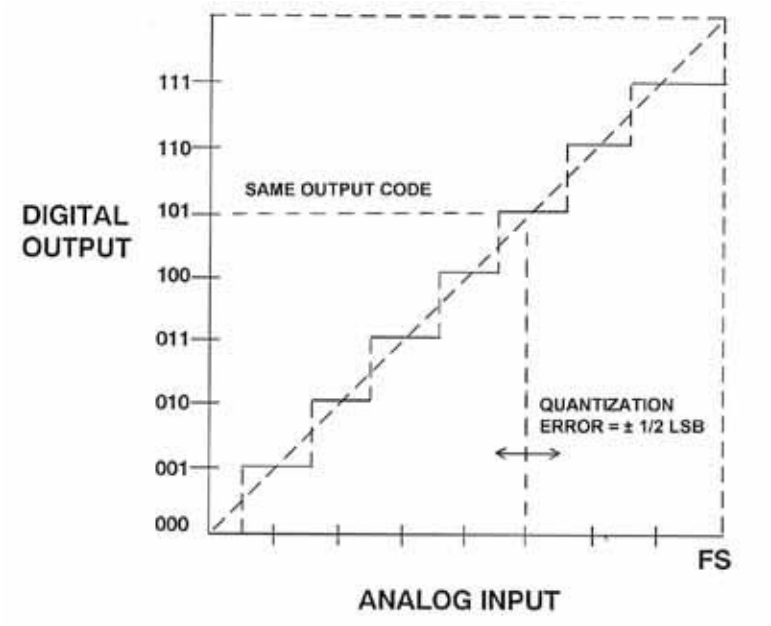



**Figure 3.4**

Digital full scale (all "1"s) corresponds to 1 LSB below the analog full scale (the reference or some multiple thereof). This is because, as mentioned above, the digital code represents the *normalized* ratio of the analog signal to the reference, and if this were unity, the digital code would be all "0"s and "1" in the bit *above* the MSB.

The (ideal) ADC transitions take place at _ LSB above zero and thereafter every LSB, until 1_ LSB below analog full scale. Since the analog input to an ADC can take any value, but the digital output is quantized, there may be a difference of up to _ LSB between the actual analog input and the exact value of the digital output. This is known as the *quantization error* or *quantization uncertainty*. In AC (sampling) applications, this quantization error gives rise to *quantization noise.* If we apply a fixed input to an ideal ADC, we will always obtain the same output, and the resolution will be limited by the quantization error.

Suppose, however, that we add some AC (dither) to the fixed signal, take a large number of samples, and prepare a histogram of the results. We will obtain something like the result in Figure 3.5. If we calculate the mean value of a large number of samples, we will find that we can measure the fixed signal with greater resolution than that of the ADC we are using. This procedure is known as *over-sampling.*

**OVERSAMPLING WITH DITHER ADDED TO INPUT**

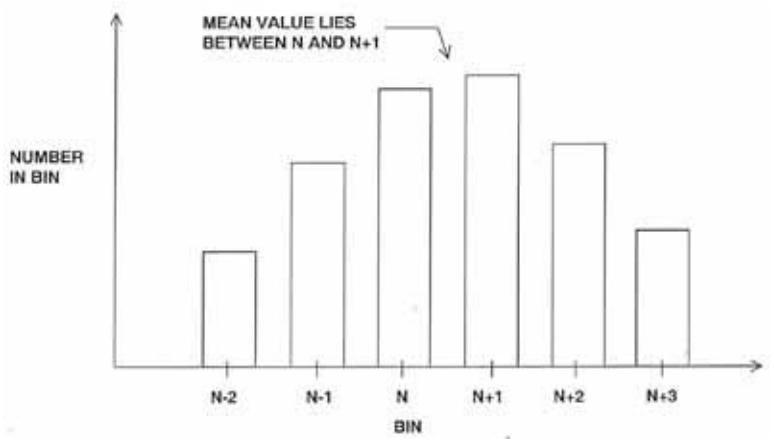



**Figure 3.5**

The AC (dither) that we add may be a sine-wave, a tri-wave, or Gaussian noise (but *not* a square wave) and, with some types of sampling ADCs (including Sigma-Delta ADCs), an external dither signal is unnecessary, since the ADC generates its own. Analysis of the effects of differing dither waveforms and amplitudes is complex and, for the purposes of this section, unnecessary. What we do need to know is that with the simple over-sampling described here, the number of samples must be doubled for each _bit of increase in effective resolution.

If, instead of a fixed DC signal, the signal that we are over-sampling is an AC signal, then it is not necessary to add a dither signal to it in order to over-sample, since the signal is moving anyway. (If the AC signal is a single tone harmonically related to the sampling frequency, dither may be necessary, but this is a special case.)

Let us consider the technique of over-sampling with an analysis in the frequency domain. Where a DC conversion has a *quantization error* of up to _ LSB, a sampled data system has *quantization noise.* As we have already seen, a perfect classical

N-bit sampling ADC has an rms quantization noise of q/(sqrt 12) uniformly distributed within the Nyquist band of DC to $f_S/2$ (where q is the value of an LSB and $f_S$ is the sampling rate). Therefore, its SNR with a full-scale sinewave input will be (6.02N + 1.76) dB. If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise, then its *effective* resolution will be less than N-bits. Its actual resolution (often known as its Effective Number of Bits or ENOB) will be defined by

$$\text{ENOB} = \frac{\text{SNR} - 1.76\text{dB}}{6.02\text{dB}} .$$

**SAMPLING ADC QUANTIZATION NOISE**

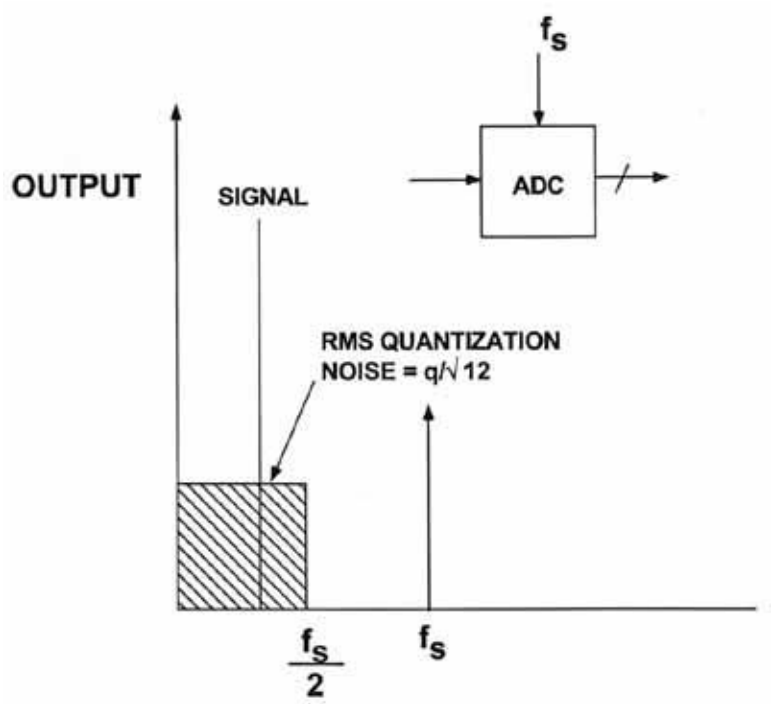



**Figure 3.6**

If we choose a much higher sampling rate, the quantization noise is distributed over a wider bandwidth as shown in Figure 3.7. If we then apply a digital low pass filter (LPF) to the output, we remove much of the quantization noise, but do not affect the wanted signal - so the ENOB is improved. We have accomplished a high resolution A/D conversion with a low resolution ADC.

**OVERSAMPLING FOLLOWED BY DIGITAL FILTERING AND DECIMATION IMPROVES SNR AND ENOB**

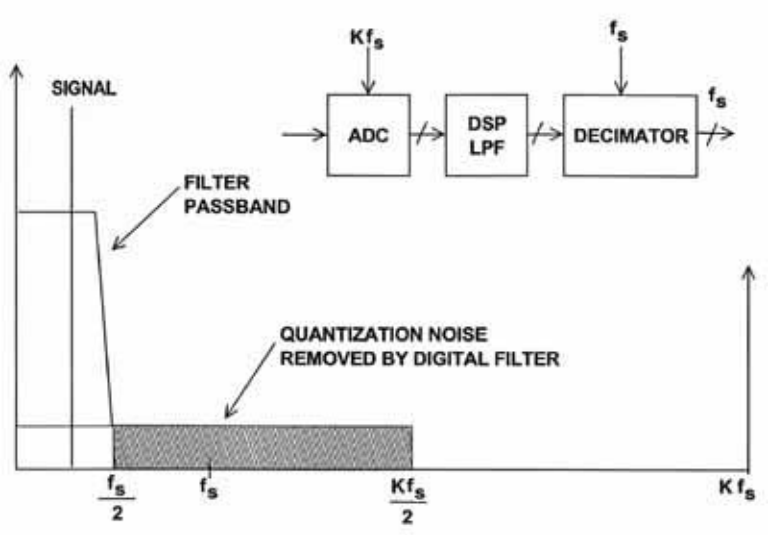



**Figure 3.7**

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate and still satisfy the Nyquist criterion. This may be achieved by passing every Mth result to the output and discarding the remainder. The process is known as "decimation" by a factor of M. Despite the origins of the term (*decem* is Latin for ten), M can have any integer value, provided that the output data rate is more than twice the signal bandwidth. Decimation does not cause any loss of information (see Figure 3.8).

**DECIMATION**

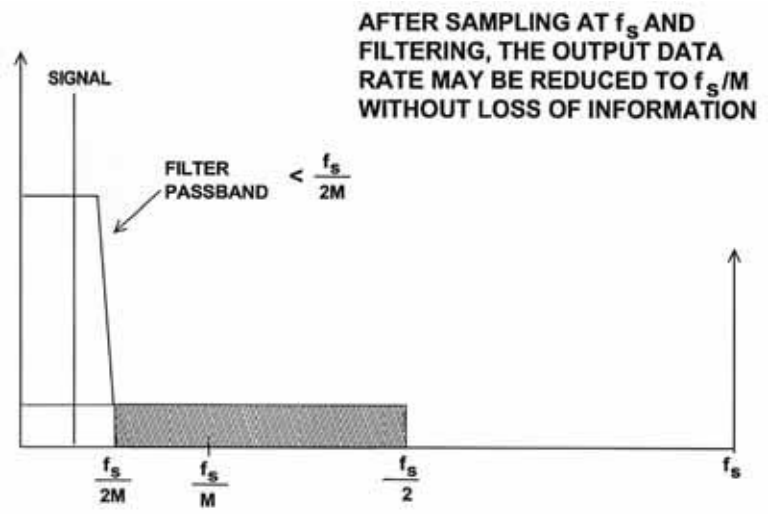



**Figure 3.8**

If we simply use over-sampling to improve resolution, we must over-sample by a factor of 2^2N to obtain an N-bit increase in resolution. The Sigma-Delta converter does not need such a high over-sampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband.

If we take a 1-bit ADC (generally known as a comparator), drive it with the output of an integrator, and feed the integrator with an input signal summed with the output of a 1-bit DAC fed from the ADC output, we have a first-order Sigma-Delta modulator as shown in Figure 3.9. Add a digital low pass filter (LPF) and decimator at the digital output, and we have a Sigma-Delta ADC: the Sigma-Delta modulator shapes the quantization noise so that it lies above the passband of the digital output filter, and the ENOB is therefore much larger than would otherwise be expected from the over-sampling ratio.

**FIRST ORDER SIGMA-DELTA ADC**

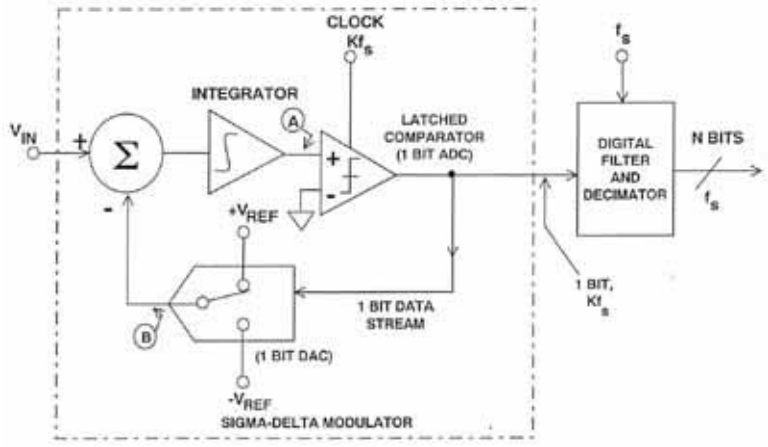



**Figure 3.9**

By using more than one integration and summing stage in the Sigma-Delta modulator, we can achieve higher orders of quantization noise shaping and even better ENOB for a given over-sampling ratio as is shown in Figure 3.10 for both a first and second-order Sigma-Delta modulator. The block diagram for the second-order Sigma-Delta modulator is shown in Figure 3.11. Third, and higher, order Sigma-Delta ADCs were once thought to be potentially unstable at some values of input - recent analyses using *finite* rather than infinite gains in the comparator have shown that this is not necessarily so, but even if instability does start to occur, it is not important, since the DSP in the digital filter and decimator can be made to recognize incipient instability and react to prevent it.

**SIGMA-DELTA MODULATORS**
**SHAPE QUANTIZATION NOISE**

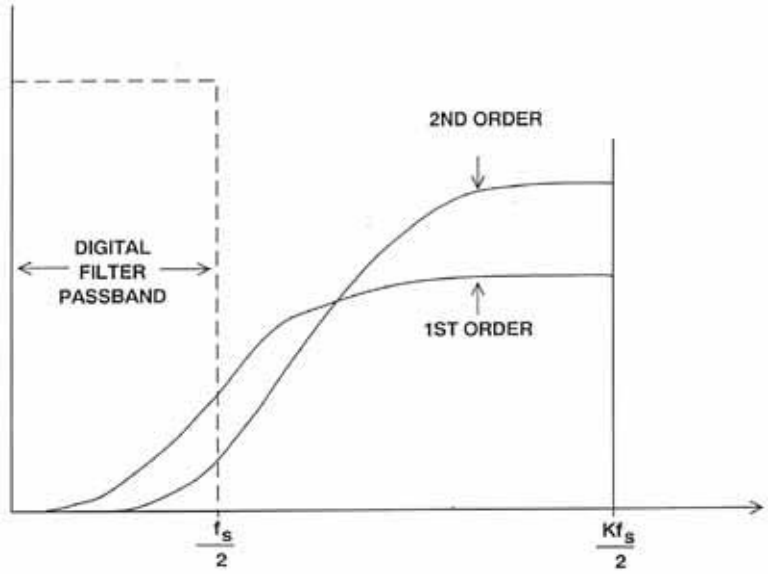



**Figure 3.10**

**SECOND-ORDER SIGMA-DELTA ADC**

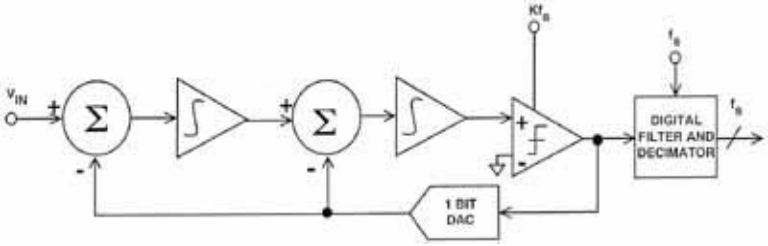



**Figure 3.11**

Figure 3.12 shows the relationship between the order of the Sigma-Delta modulator and the amount of over-sampling necessary to achieve a particular SNR.

**SNR VERSUS OVERSAMPLING RATIO FOR FIRST, SECOND, AND THIRD-ORDER LOOPS**

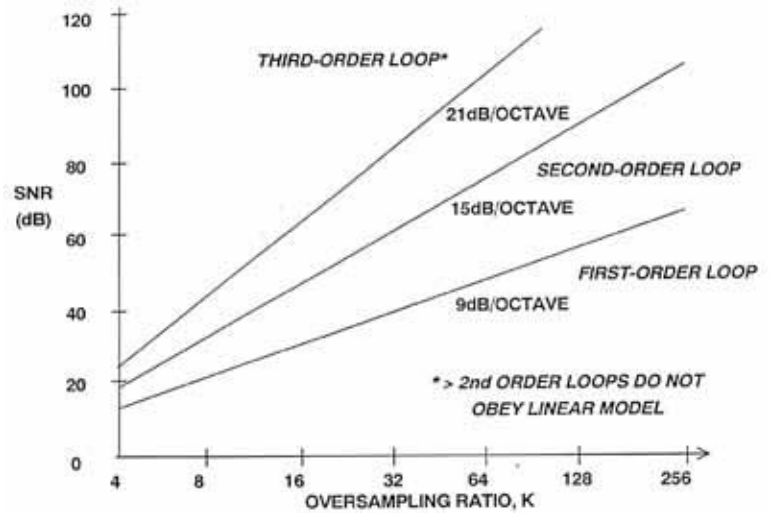



**Figure 3.12**

The Sigma-Delta ADCs that we have described so far contain integrators, which are low pass filters, whose passband extends from DC. Thus, their quantization noise is pushed up in frequency. At present, all commercially available Sigma-Delta ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain bandpass rather than lowpass digital filters to eliminate any system DC offsets). Sigma-Delta ADCs are available with resolutions up to 24-bits for DC measurement applications (AD7710, AD7711, AD7712, AD7713, AD7714), and with resolutions of 18-bits for high quality digital audio applications (AD1879).

But there is no particular reason why the filters of the Sigma-Delta modulator should be LPFs, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a Sigma-Delta ADC with bandpass filters (BPFs), the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the pass-band (see Reference 1). If the digital filter is then programmed to have its pass-band in this region, we have a Sigma-Delta ADC with a bandpass, rather than a low pass characteristic (see Figure 3.13). Although studies of this architecture are in their infancy, such ADCs would seem to be ideally suited for use in digital radio receivers, medical ultrasound, and a number of other applications.

## REPLACING INTEGRATORS WITH RESONATORS GIVES A BANDPASS SIGMA-DELTA ADC

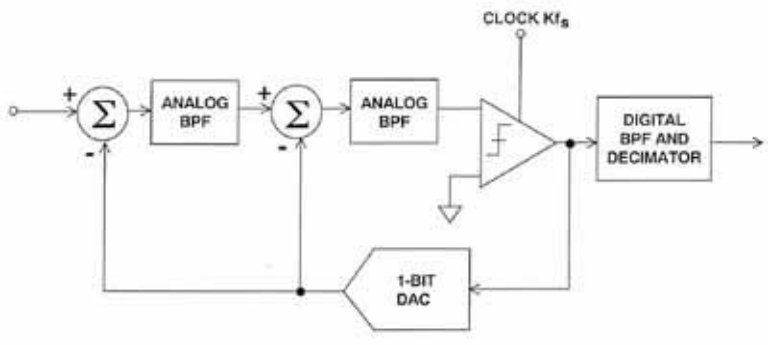



**Figure 3.13**

A Sigma-Delta ADC works by over-sampling, where simple analog filters in the Sigma-Delta modulator shape the quantization noise so that the SNR *in the bandwidth of interest* is much lower than would otherwise be the case, and by using high performance digital filters and decimation to eliminate noise outside the required passband. Because the analog circuitry is so simple and undemanding, it may be built with the same digital VLSI process that is used to fabricate the DSP circuitry of the digital filter. Because the basic ADC is 1-bit (a comparator), the technique is inherently linear.

Although the detailed analysis of Sigma-Delta ADCs involves quite complex mathematics, their basic design can be understood without the necessity of any mathematics at all. For further discussion on Sigma-Delta ADCs, refer to References 2 and 3.

### SIGMA-DELTA SUMMARY

- **Linearity is Inherently Excellent**
- **High Resolutions (16 - 24 Bits)**
- **Ideal for Mixed-Signal IC Processes, no Trimming**
- **No SHA Required**
- **Charge Injection at Input Presents Drive Problems**
- **Upper Sampling Rate Currently Limits Applications to Measurement, Voiceband, and Audio, but Bandpass Sigma-Delta Techniques Will Change This**
- **Analog Multiplexing Applications are Limited by Internal Filter Settling Time. Consider One Sigma-Delta ADC per Channel.**

**Figure 3.14**

# HIGH RESOLUTION, LOW-FREQUENCY MEASUREMENT ADCS

The AD7710, AD7711, AD7712, AD7713, and AD7714 are members of a family of sigma-delta converters designed for high accuracy, low frequency measurements. They have no missing codes at 24-bits and useful resolution of up to 21.5-bits (AD7710, AD7711, AD7712, and AD7713), and 22.5 bits (AD7714). They all use similar sigma-delta cores, and their main differences are in their analog inputs, which are optimized for different transducers. The AD7714 is the newest member of the family and is fully specified for either +5V (AD7714-5) or +3V (AD7714-3) operation.

The digital filter in the sigma-delta core may be programmed by the user for output update rates between 10Hz and 1kHz (AD7710, AD7711, AD7712), 2Hz and 200Hz (AD7713), and 2Hz and 1kHz (AD7714). The effective resolution of these ADCs is inversely proportional to the bandwidth. For example, for 22.5-bits of effective resolution, the output update rate of the AD7714 cannot exceed 10Hz. The AD771X family is ideal for such sensor applications as those shown in Figure 3.15.

**SIGNAL CONDITIONING, TRANSDUCER INPUT ADCs**
**THE AD7710, AD7711, AD7712, AD7713, AD7714**

- **Ultra-High Resolution Measurement Systems**
- **Implemented Using ΣΔ Conversion**
- **Ideal for Applications Such As:**
  - **Weigh Scales**
  - **RTDs**
  - **Thermocouples**
  - **Strain Gauges**
  - **Process Control**
  - **Smart Transmitters**
  - **Medical**

**Figure 3.15**

The AD771X family has a high level of integration which simplifies the design of data acquisition systems. For example, the AD7710 (Figures 3.16 and 3.17) has two high impedance differential inputs that can be interfaced directly to many different sensors, including resistive bridges. The two inputs are selected by the internal multiplexer, which passes the signal to a programmable gain amplifier (PGA). The PGA has a digitally programmable gain range of 1 to 128 to accommodate a wide range of signal inputs. After the PGA, the signal is digitized by the sigma-delta modulator. The digital filter notch frequency may be adjusted from 10Hz to 1kHz, which allows various input bandwidths.

To achieve this high accuracy, the AD771X family has four different internal calibration modes, including system and background calibration. All of these

functions are controlled via a serial interface. A benefit of this serial interface is that the AD771X-family fits into a 24-pin package, giving a small footprint for the high level of integration. All of the parts except the AD7713 and AD7714 can operate on either a single +5V or dual ±5V supplies. The AD7713 is designed exclusively for single supply (+5V) operation. The AD7714 is the newest member of the family and is designed for either single +3V (AD7714-3) or single +5V (AD7714-5) low power applications. The AD771X family has <0.0015% non-linearity.

**THE AD771X-SERIES PROVIDES**
**A HIGH LEVEL OF INTEGRATION IN A 24-PIN PACKAGE**

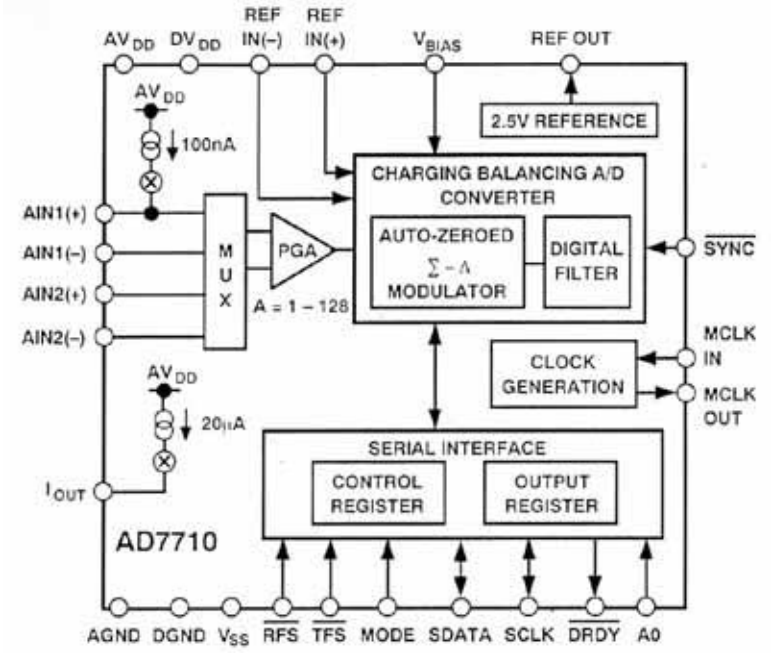



**Figure 3.16**

**KEY FEATURES OF THE AD7710**

- **±0.0015% Nonlinearity**
- **Two Channels with Differential Inputs**
- **Programmable Gain Amplifier (G = 1 to 128)**
- **Programmable Low Pass Filter**
- **System or Self-Calibration Options**
- **Single or Dual 5V Supply Operation**
- **Microcontroller Serial Interface**

**Figure 3.17**

The AD7710, AD7711, AD7712, and AD7713 have identical structures of PGA, sigma-delta modulator, and serial interface. Their main differences are in their input configurations. The AD7710 has two low level differential inputs, the AD7711 two low level differential inputs with excitation current sources which make it ideal for RTD applications, the AD7712 has one low level differential input and a single ended high level input that can accommodate signals of up to four times the reference voltage, and the AD7713 is designed for loop-powered applications where power dissipation is important. The AD7713 consumes only 3.5mW of power from a single +5V supply.

The AD7714 is designed for either +3V (AD7714-3) or +5V (AD7714-5) single-supply, low power applications. It has a buffer between the multiplexer and the PGA which can be enabled or bypassed using a control line. When the buffer is active, it isolates the analog inputs from the transient currents and variable impedance of the switched-capacitor PGA.

**SUMMARY TABLE OF AD771X DIFFERENCES**

- **AD7710:**
  - **2-Channel Low-Level Differential Inputs**
- **AD7711:**
  - **1-Channel Low-Level Differential Input**
  - **1-Channel Low-Level Single-Ended Input**
  - **Excitation Current Sources for 3 or 4-Wire RTDs**
- **AD7712:**
  - **1-Channel Low-Level Differential Input**
  - **1-Channel High-Level Single-Ended Input**
- **AD7713:**
  - **2-Channel Low-Level Differential Inputs**
  - **1-Channel High-Level Single-Ended Input**
  - **Excitation Current Sources for 3 or 4-Wire RTDs**
  - **Single 5V Operation Only**
  - **Low Power (3.5mW)**
  - **No Internal Reference**
- **AD7714:**
  - **3-Channel Low-Level Differential Inputs or 5-Channel Pseudo-Differential Inputs**
  - **Single +3V (AD7714-3) or Single +5V (AD7714-5)**
  - **Low Power (1.5mW: AD7714-3)**
  - **No Internal Reference**

**Figure 3.18**

Because of the differences in analog interfaces, each device is best suited to a particular sensor or system application. In other words, the sensor and the system requirements (i.e. type of sensor, single versus dual supply, power consumption, etc.) determine which converter should be used. Figure 3.19 lists the converters, and the sensors and applications to which they are best suited.

**AD771X APPLICATIONS**

- **AD7710:**
  - **Weigh Scales**
  - **Thermocouples**
  - **Chromatography**
  - **Strain Gauge**
- **AD7711:**
  - **RTD Temperature Measurement**
- **AD7712:**
  - **Smart Transmitters**
  - **Process Control**
- **AD7713:**
  - **Loop-Powered Smart Transmitters**
  - **RTD Temperature Measurement**
  - **Process Control**
  - **Portable Industrial Instruments**
- **AD7714:**
  - **Single +3V Supply Applications**
  - **Portable Industrial Instruments**
  - **Portable Weigh Scales**

**Figure 3.19**

Although the AD7714 is often used as an example, the following discussion applies to all the converters in the family, with some minor exceptions. The basic AD7714 ADC (see Figure 3.20) is a switched capacitor sigma-delta converter which operates as has previously been discussed in this section. The signals on the input channels pass through a switching matrix (multiplexer) and into a bypassable buffer. The buffer (available only in the AD7714) allows the input signals to be isolated from the PGA switching transients and variable impedance (PGA operation will be described shortly). The PGA gain is programmable from 1 to 128, thereby allowing low level signals to be converted without the need for external amplification.

**AD7714 SINGLE-SUPPLY MEASUREMENT ADC**

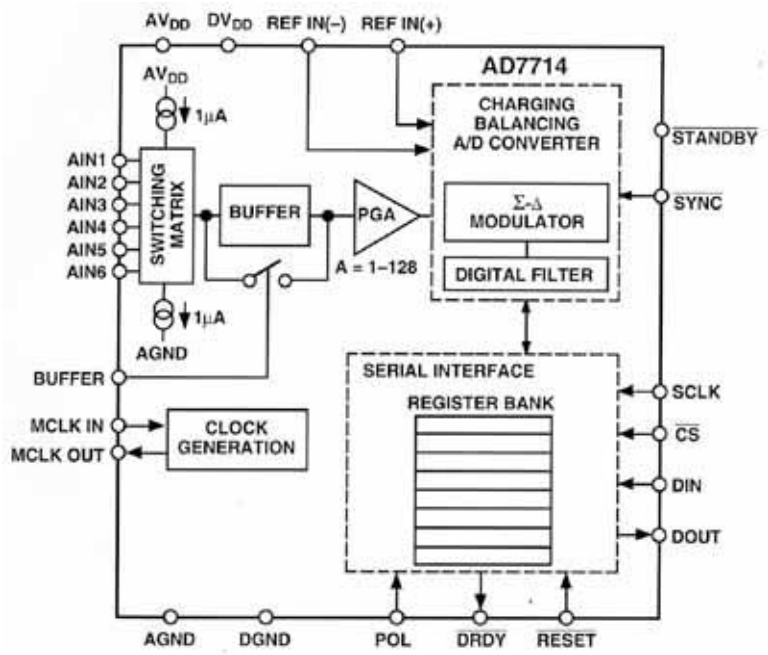



**Figure 3.20**

The functional block diagram of the AD7714 shows the PGA as separate from the sigma-delta modulator. In fact, it is part of the sigma-delta integrator (see Figure 3.21). The differential signal input charges C2, which is then discharged into the integrator summing node. This is done by closing S1 and S2, and then, after opening them, closing S3 and S4. When the PGA has a gain of 1 this happens once per cycle of the basic 19.2kHz clock, but for gains of 2, 4, and 8 respectively it happens 2, 4, or 8 times per cycle. The integrator charge is balanced by switching charge in the same way from the reference into C1, and thence to the integrator summing node. The polarity of reference switched depends on the state of the comparator output.

**THE AD7714 Σ-Δ MODULATOR INCLUDES A PGA FUNCTION**

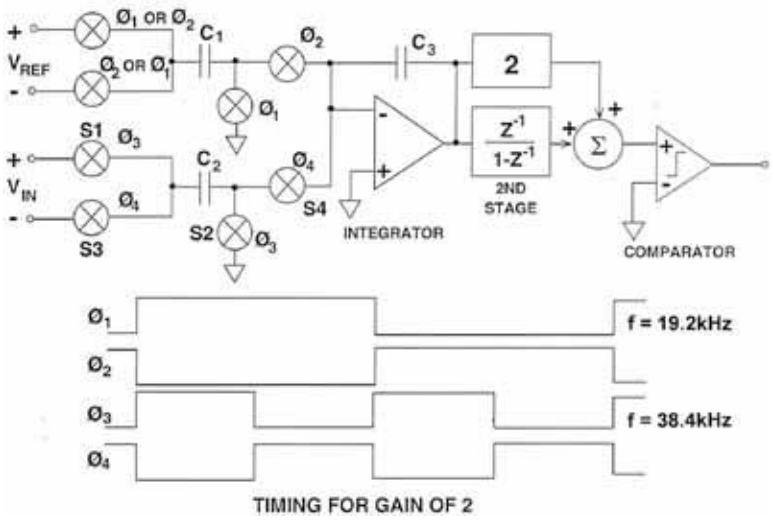



**Figure 3.21**

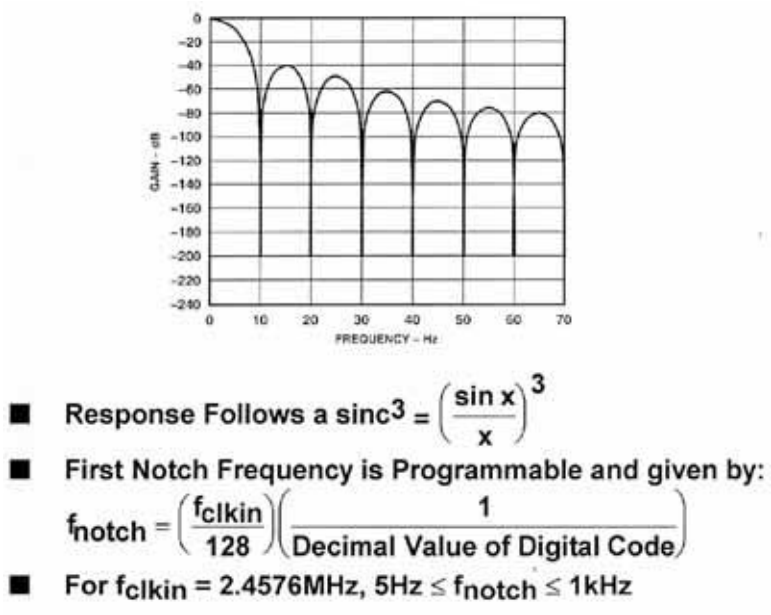
At a gain of 8, the sampling rate is 153.6kHz. Higher switching rates than this would not allow C2 sufficient time to charge, so for PGA gains greater than 8, the value of the reference capacitor, C1, is reduced, rather than the sampling rate being increased. Each time C1 is halved the gain of the system is doubled. The original value of C1 for gains of 1-8 is about 7pF in the AD7714 and 20pF for the other members of the AD771X family.

The internal digital filter has the sinc-cubed response illustrated in Figure 3.22. The first notch in the filter response is programmable according to the formula:

$$f_{notch} = \left(\frac{f_{clkin}}{128}\right)\left(\frac{1}{\text{Decimal Value of Digital Code}}\right),$$

where $f_{clkin}$ is normally either 2.4576MHz or 1MHz for the AD7714. The decimal value of the digital code in the above equation is loaded into the appropriate register in the AD7714. The master clock $f_{clkin}$ frequency of 2.4576MHz is chosen because 50Hz and 60Hz may be obtained by direct division as well as the popular communications frequencies of 19.2kHz and 9.6kHz.

## AD7714 DIGITAL FILTER FREQUENCY RESPONSE




- Response Follows a $\text{sinc}^3 = \left(\frac{\sin x}{x}\right)^3$
- First Notch Frequency is Programmable and given by:

$$f_{notch} = \left(\frac{f_{clkin}}{128}\right)\left(\frac{1}{\text{Decimal Value of Digital Code}}\right)$$

- For $f_{clkin} = 2.4576\text{MHz}$, $5\text{Hz} \le f_{notch} \le 1\text{kHz}$

**Figure 3.22**

The first notch frequency is 3.82 times the -3 dB frequency, so the notch frequency must be chosen so that the maximum signal frequency falls within the filter passband.

The lower the notch frequency, the lower the noise bandwidth, and therefore the higher the effective resolution of the converter. Moreover, the PGA gain will also set limits on the achievable resolution. With a 2.5V span, 1 LSB in a 24-bit system is only 150nV - with a gain of 128 it is 1.2nV!

As is evident from their pipeline architecture, sigma-delta ADCs have a conversion time which is related to the bandwidth of the digital filter:- the narrower the bandwidth, the longer the conversion. For a 10Hz notch frequency, the AD7714 has a 10Hz output data rate.

When the input to a sigma-delta ADC changes by a large step, the entire digital filter must fill with the new data before the output becomes valid, which is a slow process. This is why sigma-delta ADCs are sometimes said to be unsuitable for multi-channel multiplexed systems - they are not, but the time taken to change channels can be inconvenient. In the case of the AD771X-series, four conversions must take place after a channel change before the output data is again valid (Figure 3.23). The SYNC input pin resets the digital filter, and if it used, data is valid on the third output afterwards, saving one conversion cycle (when the internal multiplexer is switched, the SYNC is automatically operated). The SYNC input also allows several AD771X ADCs to be synchronized.

**THE RATE OF CONVERSION AND SETTLING TIME DEPENDS ON THE FILTER SETTING**

| | FILTER NOTCH FREQUENCY (Hz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 10 | 25 | 30 | 50 | 60 | 100 | 250 | 500 | 1k |
| CONVERSION TIME (ms) | 100 | 40 | 33.3 | 20 | 16.7 | 10 | 4 | 2 | 1 |
| MUX SWITCHING OR FULLSCALE WITH $\overline{\text{SYNC}}$, SETTLING TIME (ms) | 300 | 120 | 100 | 60 | 50 | 30 | 12 | 6 | 3 |
| ASYNCHRONOUS FULLSCALE SETTLING TIME (ms) | 400 | 160 | 133.3 | 80 | 66.7 | 40 | 16 | 8 | 4 |

- Conversion Time = $\frac{1}{\text{Filter Notch Frequency}}$
- Digital Filter Requires Settling Time for Input Step Changes
- Use $\overline{\text{SYNC}}$ Input to Decrease Settling Time

**Figure 3.23**

Although the AD771X sigma-delta ADCs are 24-bit devices, it is not possible to obtain 24 bits of useful resolution from a single sample because internal ADC noise limits the accuracy of the conversion. We thus introduce the concept of "Effective Resolution," or "Effective Number of Bits," ENOB. This is a measure of the useful signal-noise ratio of an ADC.

Noise in the ADC is generated by unwanted signal coupling and by components such as resistors and active devices. There is also intrinsic *quantization noise* which is inescapably linked to the analog-digital conversion process. As discussed in the first part of this section, sigma-delta ADCs use special techniques to shape their quantization noise and thus reduce their oversampling ratio for a given ENOB, but they cannot eliminate quantization noise entirely.

In an ideal noise-free ADC, it is possible to position a dc input signal so that the ADC digital output is always the same code from sample to sample. There is no quantization noise present, because only one code is being exercised. In a real-world high resolution ADC, however, there are internal noise sources which can cause the output code to change from sample to sample for a constant-value dc input signal. Figure 3.24 shows the comparison between an ideal ADC and an one which has internal noise. The results are plotted as a histogram, where the vertical axis represents the number of occurrences of each code out of the total number of 5000 samples used in this example. In the ideal ADC, all 5000 samples result in the same output code. In the practical ADC, however, internal noise generally results in a distribution of codes, centered around the primary code. In most cases, the noise is Gaussian, and a normal distribution can be fitted to the points on the histogram. The standard deviation of this distribution, sigma, represents the rms value of the sum of all internal noise sources reflected to the ADC output, measured in LSBs. This of course assumes a noise-free input. The rms value in LSBs can be converted easily to an effective rms voltage noise.

**HISTOGRAM SHOWS THE EFFECT OF INTERNAL ADC NOISE FOR A DC INPUT SIGNAL**

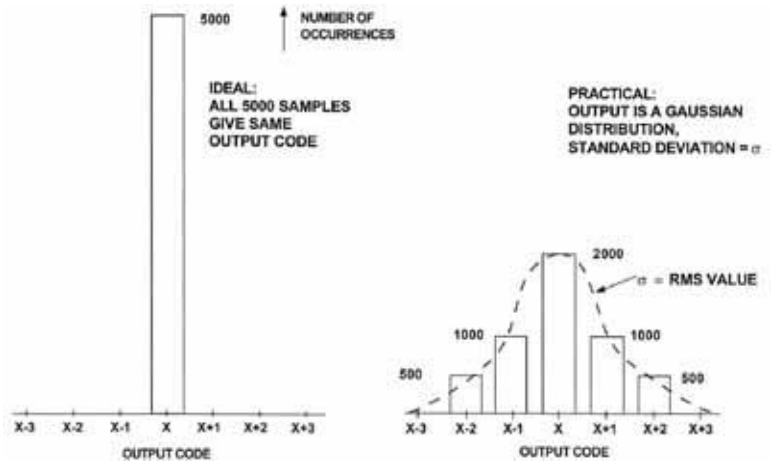



**Figure 3.24**

The signal-to-noise ratio can then be computed by dividing the full scale ADC input range by the rms noise computed from the histogram. The full scale input range for the AD771X-series is equal to twice the reference voltage divided by the gain of the PGA, and the equation for calculating the *effective resolution* in bits is given by:

$$\text{Effective Resolution} = \log_2\left(\frac{2 \times V_{REF}}{\text{GAIN}} \cdot \frac{1}{\text{RMS NOISE}}\right)$$

**DETERMINING EFFECTIVE RESOLUTION**

- Effective Resolution (ENOB) = $\log_2\left(\frac{\text{Full Scale Signal}}{\text{RMS Noise}}\right)$

  = $\log_2\left(\frac{2 \times V_{REF}}{\text{Gain} \times \text{RMS Noise}}\right)$

- Output RMS Noise = Effective Noise in the Digital Output Code
- ENOBs is Greatest at Low Filter Frequency and Low Gain

**Figure 3.25**

Figure 3.26 shows how RMS noise in an AD7714 varies with gain and notch frequency. Figure 3.27 gives the same results in terms of effective resolution, or ENOB using the previous equation. The effective output noise comes from two sources. the first is the electrical noise in the semiconductor devices used in the implementation of the ADC front end and the modulator (device noise). Secondly, when the analog input signal is converted into the digital domain, quantization noise is added.

The device noise is at a low level, and is largely independent of frequency. The quantization noise starts at an even lower level, but rises rapidly with increasing frequency to become the dominant noise source. Consequently, lower filter notch settings (below 100Hz approximately for $f_{clkin}$ = 2.4576MHz tend to be device-noise dominated, while higher notch settings are dominated by quantization noise. Reducing the filter notch and cutoff frequency in the quantization-noise dominated region results in a more dramatic improvement in noise performance than it does in the device-noise dominated region. Furthermore, quantization noise is added after the PGA, so effective resolution is largely independent of gain for the higher filter notch frequencies. Meanwhile, device noise is added in the PGA, and therefore effective resolution suffers a little at high gains for lower notch frequencies.

Additionally, in the device-noise dominated region, the output noise (in μV) is largely independent of reference voltage, while in the quantization-noise dominated region, the noise is proportional to the value of the reference.

**NOISE VARIES AS A FUNCTION OF GAIN AND FILTER CUTOFF FREQUENCY (AD7714-5, UNBUFFERED MODE, CLOCK = 2.4576 MHz)**

| First Notch of Filter and O/P Data Rate | -3dB Frequency | Typical Output RMS Noise (μV) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Gain of 1 | Gain of 2 | Gain of 4 | Gain of 8 | Gain of 16 | Gain of 32 | Gain of 64 | Gain of 128 |
| 5 Hz | 1.31Hz | 0.67 | 0.48 | 0.24 | 0.2 | 0.18 | 0.17 | 0.17 | 0.17 |
| 10 Hz | 2.62 Hz | 1.0 | 0.78 | 0.48 | 0.33 | 0.25 | 0.25 | 0.25 | 0.25 |
| 25 Hz | 6.55 Hz | 1.8 | 1.1 | 0.63 | 0.5 | 0.44 | 0.41 | 0.38 | 0.38 |
| 30 Hz | 7.86 Hz | 2.5 | 1.31 | 0.84 | 0.57 | 0.46 | 0.43 | 0.4 | 0.4 |
| 50 Hz | 13.1 Hz | 4.33 | 2.06 | 1.2 | 0.64 | 0.54 | 0.46 | 0.46 | 0.46 |
| 60 Hz | 15.72 Hz | 5.28 | 2.36 | 1.33 | 0.87 | 0.63 | 0.62 | 0.6 | 0.56 |
| 100 Hz | 26.2 Hz | 12.1 | 5.9 | 2.86 | 1.91 | 1.06 | 0.83 | 0.82 | 0.76 |
| 250 Hz | 65.5 Hz | 127 | 58 | 29 | 15.9 | 6.7 | 3.72 | 1.96 | 1.5 |
| 500 Hz | 131 Hz | 533 | 267 | 137 | 66 | 38 | 20 | 8.6 | 4.4 |
| 1kHz | 262 Hz | 2,850 | 1,258 | 680 | 297 | 131 | 99 | 53 | 28 |

**Figure 3.26**

**EFFECTIVE RESOLUTION VERSUS GAIN AND FIRST NOTCH FREQUENCY (AD7714-5, UNBUFFERED MODE, CLOCK = 2.4576 MHz)**

| First Notch of Filter and O/P Data Rate | -3dB Frequency | Effective Resolution (ENOBs) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Gain of 1 | Gain of 2 | Gain of 4 | Gain of 8 | Gain of 16 | Gain of 32 | Gain of 64 | Gain of 128 |
| 5 Hz | 1.31Hz | 22.5 | 22.5 | 22.5 | 21.5 | 20.5 | 20 | 19 | 18 |
| 10 Hz | 2.62 Hz | 22.5 | 21.5 | 21.5 | 21 | 20.5 | 19.5 | 18.5 | 17.5 |
| 25 Hz | 6.55 Hz | 21.5 | 21 | 21 | 20 | 19.5 | 18.5 | 17.5 | 16.5 |
| 30 Hz | 7.86 Hz | 21 | 21 | 20.5 | 20 | 19.5 | 18.5 | 17.5 | 16.5 |
| 50 Hz | 13.1 Hz | 20 | 20 | 20 | 20 | 19 | 18.5 | 17.5 | 16.5 |
| 60 Hz | 15.72 Hz | 20 | 20 | 20 | 19.5 | 19 | 18 | 17 | 16 |
| 100 Hz | 26.2 Hz | 18.5 | 18.5 | 19 | 18.5 | 18 | 17.5 | 16.5 | 15.5 |
| 250 Hz | 65.5 Hz | 15.5 | 15.5 | 15.5 | 15.5 | 15.5 | 15.5 | 15.5 | 14.5 |
| 500 Hz | 131 Hz | 13 | 13 | 13 | 13 | 13 | 13 | 13 | 13 |
| 1kHz | 262 Hz | 11 | 11 | 11 | 11 | 11 | 10.5 | 10.5 | 10.5 |

- Effective Resolution = $\log_2\left[\frac{2\times V_{REF}}{GAIN}\bullet\frac{1}{RMS\ NOISE}\right]$
- Highest resolution occurs at low gains and low frequency

**Figure 3.27**

It is important to distinguish between RMS and peak-to-peak noise. Noise in a sigma-delta ADC has a Gaussian (or near Gaussian) distribution. This means that if one waits long enough, any value of peak noise will eventually occur, and it is not possible to write a specification *absolutely* prohibiting a specified value of noise peak. For practical purposes, the peak-to-peak noise is defined as 6.6 times the RMS noise, since such peaks occur less than 0.1% of the time. The noise specified in the ENOB table in Figure 3.27 is expressed in RMS terms. If a figure for "noise-free" code resolution is required, it will be approximately 3-bits worse: 20-bits ENOB becomes 17-bits noise-free code, etc. Since most applications are concerned with noise *power*, however, the RMS ENOB figure is the more commonly used.

This does not mean that the original 24-bit resolution has no value, however. Additional external filtering, to narrower bandwidths than the internal filter, can further improve the resolution and ENOB at the expense of longer conversion times. The histogram approach using a large number of samples can also be used to more accurately define the input signal.

**ESTIMATING NOISE-FREE CODE RESOLUTION**

- **Determined Using Peak-to-Peak Noise**
- **Output RMS Noise × 6.6 = Peak-to-Peak Noise**
- **Factor of 6.6 is Approximately Equal to 3 bits:**

  $$\log_2 (6.6) = 2.72$$

- **Therefore, subtract 3 bits from Effective Resolution Given in Figure 3.27 to Determine Noise Free Code Resolution**

**Figure 3.28**

The results in Figures 3.27 and 3.28 assume the use of a low noise, heavily decoupled external reference and a noise-free analog input. Noisy inputs (and the reference is an input) reduce the effective resolution. For this reason, careful attention must be paid to external noise sources. Figure 3.29 lists aspects of board layout which may affect system noise, and hence the ENOB of the AD771X-series.

**OPTIMIZING NOISE PERFORMANCE**

- **Pay Attention to Layout!**
- **Use Ground Planes**
- **Keep Analog PCB Tracks Short**
- **Interface Directly with Transducer**
- **Use Low Noise Amplifiers (AD797, OP-213, OP-177, AD707) (Only if Required)**
- **Connect Analog and Digital Grounds of Converters Together at the Device, and Connect them to Analog Ground Plane**
- **Route Digital PCB Tracks Clear of Analog Tracks**
- **Filter Signal and Reference Inputs**
- **Minimize Reference Noise**
- **The Evaluation Board is an Example of Good Layout**

**Figure 3.29**

The AD771X-series is designed to interface directly with most transducers without the need for external buffering or amplification. If external amplifiers are used, however, low noise devices such as the OP-213 and AD797 should be chosen. To determine if external amplifiers will lower the AD771X system resolution, the total additional noise (in the bandwidth 0.1 Hz to the cutoff frequency set in the AD771X) should be calculated and compared with the RMS noise figures given in Figure 3.26. (Uncorrelated noise adds by root sum of squares, so if the additional noise is <50% of the AD7710 noise, it may be ignored; but if it exceeds this level, its effect on system performance must be studied carefully.)

An external filter on the input of the AD771X-series can improve its noise performance, because the modulator does not reject noise at integer multiples of the sampling frequency. This means that there are frequency bands $\pm f_{3dB}$ wide ($f_{3dB}$ is the cutoff frequency of the internal digital filter) where noise passes unattenuated to the output. However, due to the AD771X high oversampling ratio, these bands occupy only a small fraction of the spectrum, and most broadband noise is filtered. The internal analog front end provides some filtering at these frequencies (the attenuation at 19.2kHz is approximately 70dB), but high level wideband noise can degrade system ENOB. A simple external RC low-pass filter is generally sufficient to minimize the effects of this noise, but the resistor and capacitor must be carefully chosen so that the gain accuracy of the AD771X is not affected. If the AD7714 is used in the buffered mode (i.e. the internal buffer is active), this restriction does not apply.

**INPUT FILTER HELPS REDUCE WIDEBAND NOISE**

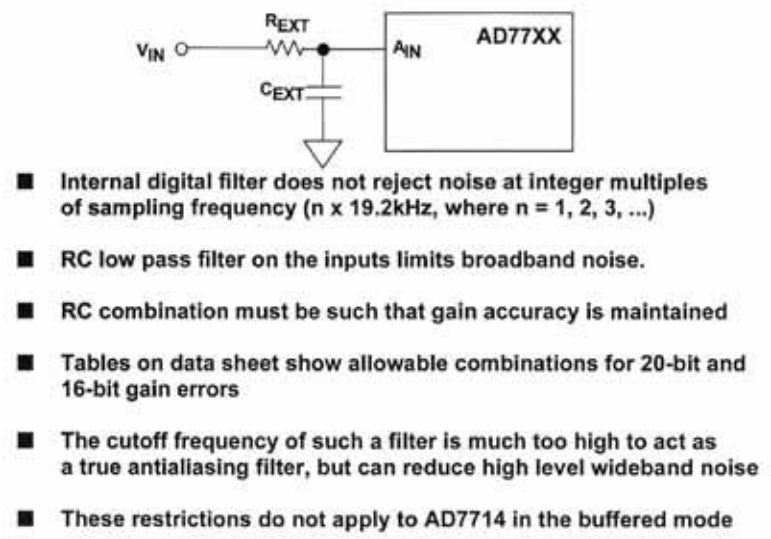



**Figure 3.30**

A simplified model of the analog input of the AD7714 in the unbuffered mode is shown in Figure 3.31 (The AD7710, AD7711, AD7712, and AD7713 have similar structures). It consists of a resistor of approximately 7kohm (input multiplexer on-resistance) connected to the input terminal and to an analog switch which switches a 7pF sampling capacitor between the resistor and ground, with a mark-space ratio of 50%. The switching frequency depends on $f_{clkin}$ and the gain which is being used: with a gain of unity and the standard clock frequency of 2.4576MHz, the switching frequency is 19.2kHz, and at gains of 2, 4, and 8 or more it is 38.4, 76.8, and 153.6kHz respectively.

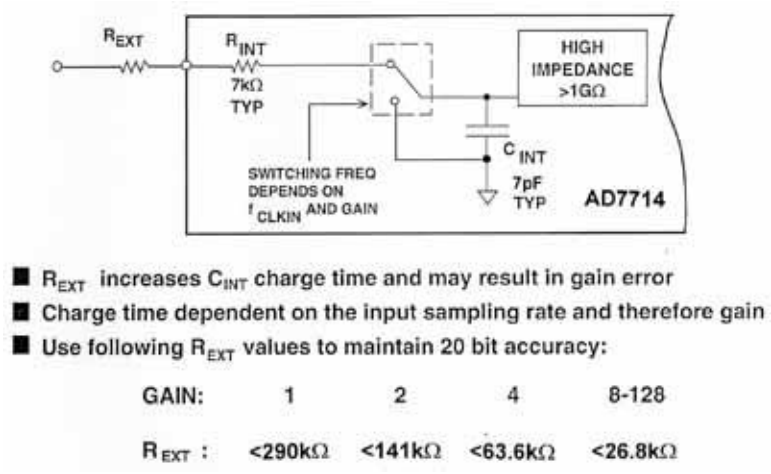
If the converter is working to an accuracy of 20-bits, the capacitor must charge with an accuracy of 20-bits. The input RC time constant due to the switch on-resistance (7kohm) and the sampling capacitor (7pF) is 49ns. If the charge is to achieve 20-bit accuracy, it must charge for at least 14x the time constant, or 686ns. Any external resistor in series with the input will increase the time constant, and the chart in Figure 3.31 shows acceptable values of series resistance necessary to maintain 20-bit performance.

To determine the minimum charge time for 20-bit performance with an external resistance $R_{ext}$ we use the equation:

$$\text{Minimum Charge Time} = 14(R_{ext} + 7\text{kohm}) \times 7\text{pF}$$

The minimum charge time must be less than half the period of the switching signal used (it has a 50% duty cycle). The fastest switching frequency with the standard 2.4576MHz clock is 153.6kHz (for a gain of 8 or greater), and half of that clock period is 3.3µs, which allows a maximum $R_{ext}$ of 26.8kohm. At lower gains $R_{ext}$ may be larger.

**AD7714 ANALOG INPUT STRUCTURE (UNBUFFERED MODE)**




- $R_{EXT}$ increases $C_{INT}$ charge time and may result in gain error
- Charge time dependent on the input sampling rate and therefore gain
- Use following $R_{EXT}$ values to maintain 20 bit accuracy:

| GAIN: | 1 | 2 | 4 | 8-128 |
|---|---|---|---|---|
| $R_{EXT}$ : | <290kΩ | <141kΩ | <63.6kΩ | <26.8kΩ |

**Figure 3.31**

It is not practical to use $R_{ext}$ in conjunction with a capacitor to ground from the input pin of the AD7710, AD7711, AD7712, or AD7713 (or the AD7714 operating in the unbuffered mode) to make an anti-aliasing filter (with a cutoff frequency less than one-half the input sampling frequency), unless the capacitor is dramatically larger than the 7pF $C_{int}$. This is because $C_{int}$ is discharged on every sampling clock cycle and will recharge from the filter capacitor. Therefore, either the filter capacitor must be so large that charging $C_{int}$ from it changes its voltage by less than an LSB at 20-bits (i.e. it is larger than 7µF), or the time constant $R_{ext}C_{ext}$ must be short enough for $C_{ext}$ to recharge before the next clock cycle - in which case the cutoff frequency due to $R_{ext}$ and $C_{ext}$ is not low enough to make an anti-aliasing filter with respect to the sampling frequency. There may, however, be some benefit in such a filter if there is input noise at high frequencies. The data sheets for the AD771X-series contain tables which give the allowable external capacitor and resistor values as a function of PGA gain for 16-bit and 20-bit gain accuracy (see Figure 3.32).

Note that if an external $R_{ext}$ and $C_{ext}$ are used, the capacitor type must have low non-linearities and dielectric absorption. Film types such as polystyrene or polypropylene are recommended.

**AD7714 EXTERNAL FILTER RESTRICTIONS ON R AND C FOR NO 20-BIT GAIN ERROR (UNBUFFERED MODE ONLY)**

| GAIN | EXTERNAL CAPACITOR (pF) | | | | | |
|---|---|---|---|---|---|---|
| | 0 | 50 | 100 | 500 | 1000 | 5000 |
| 1 | 290 kΩ | 69 kΩ | 40.8 kΩ | 10.4 kΩ | 5.6 kΩ | 1.4 kΩ |
| 2 | 141 kΩ | 33.8 kΩ | 20 kΩ | 5 kΩ | 2.8 kΩ | 700 Ω |
| 4 | 63.6 kΩ | 16 kΩ | 9.6 kΩ | 2.4 kΩ | 1.34 kΩ | 340 Ω |
| 8 - 128 | 26.8 kΩ | 7.2 kΩ | 4.4 kΩ | 1.1 kΩ | 600 Ω | 160 Ω |

**Figure 3.32**

The advantage of the AD7714 operating in the buffered mode is that a true input antialiasing filter can be used without affecting the gain accuracy. The penalty is only a slight increase in noise (approximately 10%) and a small reduction in input common-mode voltage range. If the value of the series resistor is large, the effects of the input bias current must be considered, but this error can be removed using the calibration modes.

Some successive approximation and subranging ADCs draw large transient currents at their analog and reference inputs which load their respective drive circuitry and cause errors. Often, special drive amplifiers with low output impedance at frequencies well above the conversion clock frequency are necessary to avoid this problem, but these problems do not occur with the very small transient loads of the AD771X devices. The oscilloscope photograph in Figure 3.33 shows the transient current in an AD7710. It was taken with a 1kohm resistor in series with the input to measure the change in current. This circuit produces a 15mV spike of less than 1µs duration. The corresponding peak pulse current is only 15µA, which permits the use of quite high impedance signal sources with no risk of degrading the ENOB. As discussed earlier, the AD7714 operating in the buffered mode has no significant transients on its analog input.

**INPUT TRANSIENT LOADING IS MINIMAL IN THE AD77XX FAMILY**

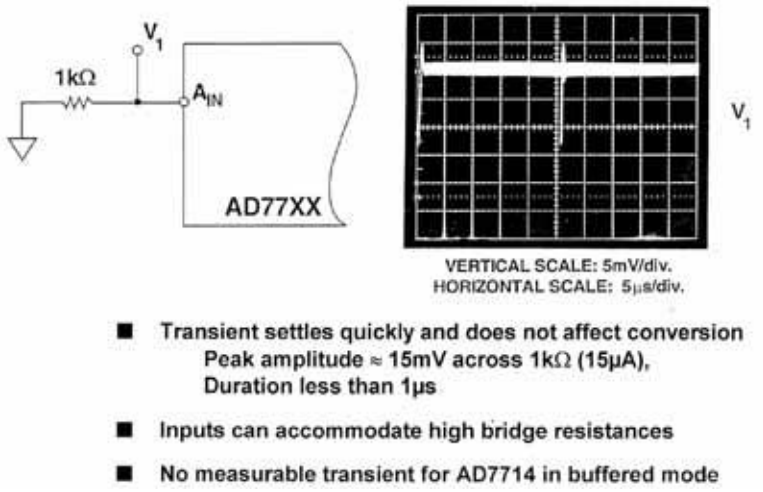



**Figure 3.33**

The AD771X family was designed to simplify transducer interfacing. Many types of transducers can be connected directly to the input of one of the AD771X family without additional circuitry, but some care is necessary to achieve the best possible accuracy:- noise needs to be minimized (a simple capacitor across a resistive sensor may be all the filtering that is needed, but this must be checked - noise is particularly important, because noise cannot be removed by the system calibration which eliminates gain and offset errors); transducer source impedance may affect charge times (as mentioned above); and bias currents flowing in high impedance transducers may cause errors, although these can be removed by system calibration. In general, system calibration can remove most dc errors in systems using the AD771X family.

**TRANSDUCER CONNECTION CONSIDERATIONS**

- **Filter Noisy Signals**
- **Use Shielded, Twisted Pair Cable (Shield Grounded at AGND/DGND Connection Point at ADC, floating at transducer)**
- **DC Leakage (bias) Current = 10pA can cause offset with $R_{source}$**
- **This causes drift over temperature**
- **To Maintain Accuracy:**
  - **Minimize $R_{source}$**
  - **Use Differential inputs and balance $R_{source}$**
  - **Use system calibration techniques**

**Figure 3.34**

Circuitry connected to transducers must generally be protected against over-voltage from ESD, noise pickup, or accidental shorts. If signals are likely to go outside the positive or negative supplies, some form of clamp is necessary to keep them within them. Figure 3.35 shows a suitable circuit for protecting AD771X devices. The AD7710 has internal ESD protection diodes between the input and both supplies which conduct when the input exceeds either supply by more than about 0.6V. Excessive current in these diodes will vaporize metal tracks on the chip and damage the circuit, so an external resistor, $R_p$, is necessary to limit current to a safe 5mA during over-voltage events. $R_p$ may be determined by a simple calculation:

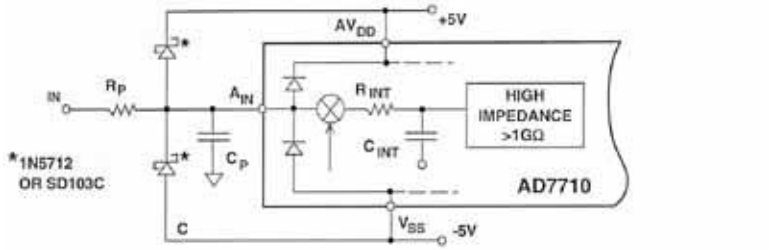
$$R_p = \frac{V_{max} - V_{supply}}{5mA}$$

$R_p$ will contribute noise to the system ( the basic Johnson noise equation applies:

$$e_n = \sqrt{4kTBR_p}$$

where k is Boltzmann's Constant, T is the absolute temperature and B is the bandwidth). If the noise due to $R_p$ is too high, $R_p$ can be reduced if external Schottky diodes are used in addition to the diodes on the chip.

## INPUT OVERVOLTAGE PROTECTION




- Internal ESD protection diodes clamp input to within 0.6V of either supply.
- Limit current due to overvoltage to less than 5mA.

$$R_P = \frac{A_{inmax} - AV_{DD}}{5mA}, \text{ or } \frac{|A_{inmin}| - |V_{SS}|}{5mA}, \text{ whichever is greater.}$$

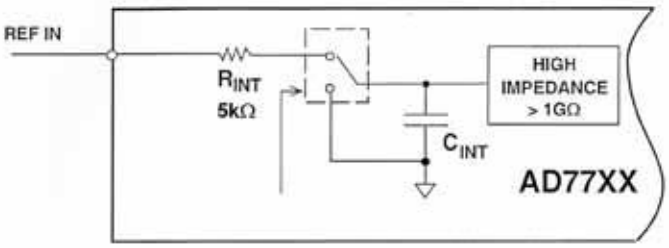
- External Schottkys can be added to reduce the size of $R_p$.
- Include $C_p$ to filter noise due to $R_p$.

**Figure 3.35**

There are no special requirements for these Schottky diodes, as long as they have low leakage current and can handle the necessary fault current levels while maintaining a low turn-on voltage.

As important as the analog signal input is the reference input. Figure 3.36 shows a simplified model of the reference input, which is very similar to that of the analog input (with the exception of the AD7714 operating in the buffered mode). The series resistor is 5kohm, and the value of the capacitor depends on the gain setting and the particular device. For gains of 1-8, the capacitor is approximately 7pF for the AD7714. Above 8, the capacitor's value is halved for each doubling of gain. The value of the capacitor (G = 1-8) for other members of the AD771X series is 20pF.

## REFERENCE VOLTAGE CONSIDERATIONS




| PGA GAIN | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
|---|---|---|---|---|---|---|---|---|
| $C_{INT}$ | C | C | C | C | C/2 | C/4 | C/8 | C/16 |

- C = 20pF for AD7710, AD7711, AD7712, AD7713
- C = 7pF for AD7714
- Heavy decoupling on REF IN required
- Minimal transient loading

**Figure 3.36**

An important consideration in choosing a reference for the AD771X-series is noise. Many references have output noise which exceeds that of the AD771X and cause reduced accuracy. Filtering may help in such cases, but a low noise reference should be selected wherever possible.

Although the AD7710, AD7711, and AD7712 have internal +2.5V references which may be connected to their positive reference input, their use will degrade the effective resolution of the ADCs by approximately 1 bit for filter cut-off frequencies of 60Hz or less. The noise calculations using the AD7710 internal reference are shown in Figure 3.37. For optimum noise performance, a low noise external reference such as the AD780 should be used as shown in Figure 3.38.

**INTERNAL REFERENCE VOLTAGE NOISE CONSIDERATIONS FOR AD7710, AD7711, AD7712 ADCs**

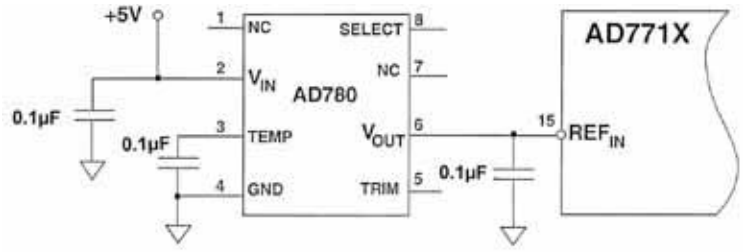
- Specified Output Noise of AD7710, AD7711, AD7712 Internal +2.5V Reference = 8.3μV rms typical (0.1 to 10Hz)
  = 3.4μV rms (0.1 to 2.62Hz, for 10Hz Output Rate)
- Reference Noise adds to intrinsic ADC noise:

  AD7710 Noise = 1.7μV rms (G = +1)

  Total Noise = $\sqrt{(1.7\mu V)^2 + (3.4\mu V)^2} = 3.8\mu V$ rms, or 25μV p – p
- This reduces effective resolution from 21.5 to 20.5 bits
- Use low-noise external reference for highest resolution at low input bandwidths

**Figure 3.37**

**USE A LOW NOISE EXTERNAL REFERENCE FOR OPTIMUM NOISE PERFORMANCE AND RESOLUTION**




- AD780 has 4μV peak-to-peak noise is 0.1 to 10Hz bandwidth.
- In a 2.62Hz bandwidth (notch frequency = 10Hz), the rms value of the noise is 0.31μV rms
- Well below the noise of the AD771X

**Figure 3.38**

The AD780 2.5V reference has noise of 4µV p-p in the range 0.1 to 10Hz. This is equivalent to 0.606µV rms (obtained by dividing the peak-to-peak value by 6.6). This gives 0.31µV rms noise in the 2.62Hz bandwidth associated with a 10Hz update rate. This is negligible compared to the AD7710 inherent noise of 1.7µV rms (G = 1). With output rates of 1kHz or more, and cutoff frequency of 262Hz, the noise of the AD780 may be reduced by 50% if a 0.1µF capacitor is connected to its output (unlike many IC voltage references, the AD780 is stable with all values of capacitive load).

**CALCULATING REFERENCE NOISE CONTRIBUTION**

- If reference noise is given as a spectral density, $V_n$ (nV/√Hz) rms,
  - $V_{refnoise} = V_n\sqrt{BW}$, where BW = 0.262 $f_{notch}$
- If reference noise is given as a peak-to-peak value in the 0.1 to 10Hz bandwidth, $V_{p-p}$, then

$$V_n = \frac{V_{p-p}}{6.6\sqrt{10Hz}}$$

  - $V_{refnoise} = \frac{V_{p-p}}{6.6\sqrt{10Hz}} \bullet \sqrt{BW}$ , BW = 0.262 $f_{notch}$
- Above are approximations, but are sufficiently accurate for estimation of reference noise
- Reference noise should be no greater than 50% of ADC noise

**Figure 3.39**

The AD780 is also a suitable reference for the AD7714 ADC, whose noise with a 10Hz update rate (G = 1, Vsupply = +5V) is 1.0µV rms. When the AD7714 is operating on a +3V supply, it requires a low-noise 1.25V reference, and the AD589 is a suitable choice.

When the AD771X-series ADCs are operated at higher output rates and higher input bandwidths, the ADC noise is significantly higher, and less effective resolution is required. This allows the use of higher noise, lower power references such as the REF192 (25µV p-p noise, 0.1 to 10Hz) which only requires 45µA of quiescent current, compared to 0.75mA for the AD780.

Regardless of the reference selected, it should be properly decoupled in order to act as a charge reservoir to transient load currents as well as a filter for wideband noise. This implies that the reference must be stable under capacitive loads, which is not necessarily the case in all references. In fact, some references actually *require* an external decoupling capacitor in order to maintain stability. Regardless of the reference selected, the data sheet should be carefully examined with respect to output capacitive loading. Further information on applying voltage references can be obtained in References 5, 6, and 7.

**LOW VOLTAGE REFERENCE SUMMARY**

| REFERENCE PART # | OUTPUT (V) | TOLERANCE (mV) (max) | DRIFT ppm/°C (max) | NOISE (μV p-p, typ) 0.1 to 10Hz | SUPPLY CURRENT (mA) typ |
|---|---|---|---|---|---|
| AD780 | +2.5 / +3.0 | 1 - 5 | 3 - 20 | 4 | 0.75 |
| REF43 | +2.5 | 15 - 50 | 10 - 25 | 5 | 0.45 |
| REF192 | +2.5 | 2 - 10 | 5 - 25 | 25 | 0.045 |
| AD589* | +1.235 | 35 | 25 - 100 | 4 | 0.050 - 5 |

* Two Terminal

**Figure 3.40**

DC errors also affect conversion accuracy, but AD771X devices can calibrate themselves to correct dc errors. The AD7710, AD7711, AD7712, and AD7713 have four different calibration modes. These are summarized in Figure 3.41 and comprise Self Calibration, System Calibration, System-Offset Calibration, and Background Calibration. Each calibration cycle contains two conversions, one each for zero-scale and for full-scale calibration. The calibration modes for the AD7714 are similar, except that in the Background-Calibration Mode, only zero-scale is calibrated.

**AD771X OFFERS 4 CALIBRATION OPTIONS**

| | SELF-CALIBRATION | SYSTEM CALIBRATION | SYSTEM OFFSET CALIBRATION | BACKGROUND CALIBRATION* |
|---|---|---|---|---|
| 1st Cycle | Internally Short Inputs to Ground | Externally Short Inputs to Zero-Scale | Externally Short Inputs to Zero-Scale | Internally Short Inputs to Ground* |
| 2nd Cycle | Internally Short Input to $V_{REF}$ | Externally Short Input to Fullscale | Calibrate for Span from $AV_{IN}$ to $V_{REF}$ | Internally Short Inputs to $V_{REF}$* |
| Duration | 9 ÷ Output Rate | 4 ÷ Output Rate Each Step | 9 ÷ Output Rate | 6 ÷ Output Rate* |

* AD7714 Background Calibration consists of zero-scale (Ground) calibration only.

**Figure 3.41**

To initiate a calibration cycle, the appropriate code must be sent to the control register. After the code is sent, the AD771X automatically conducts the entire operation, and clears the control register of the calibration command so that a separate command to stop calibration is not necessary. Since the filter in the sigma-delta converter must purge itself of its previous result for four output update cycles whenever the input sees a full-scale step the total calibration operation takes nine such cycles.

Self Calibration removes errors in an AD771X by connecting the input to ground and performing a conversion, and then connecting the input to $V_{ref}$ and performing another. The results of these conversions are used to calibrate the device.

Background Calibration is a variation of Self Calibration. The only difference is that when an AD771X is placed in Background Calibration mode, it continually calibrates itself at regular intervals without further instructions. This ensures that the AD771X remains calibrated regardless of drift. The Background Calibration cycle alternates calibration conversions with signal conversions: zero calibrate/convert signal/full-scale calibrate/convert signal/zero calibrate/etc. This provides continuous calibration but reduces the output data rate by a factor of six. Background Calibration for the AD7714 only calibrates zero-scale.

System Calibration is intended to calibrate all the elements prior to the ADC which may contribute to system errors, as well as the ADC itself. (For example an instrumentation amplifier introduces errors into a system due to its own offset, drift and gain error. These errors can be removed by System Calibration.) However, System Calibration requires additional analog switches to connect *system* inputs to ground and a reference as well as to the original signal source. The first step in System Calibration requires external grounding of the system input terminal to calibrate out offsets. The second step requires that the input be connected to a reference, which calibrates gain error at full-scale. The System Calibration cycle requires the sending of two separate instructions to the control register as well as control of the analog switches at the system input. It must be repeated regularly to correct for drift with time and temperature.

The final calibration mode is System-Offset Calibration. This calibrates *system* offsets, and *the AD771X* gain. Again, it requires external analog switches at the system input, and separate instructions for zero and gain calibration. For the first cycle, the system input is connected to ground and the AD771X calibrates for system offsets. During the second cycle, the ADC input is connected to the reference for ADC gain calibration.

## CALIBRATION ISSUES

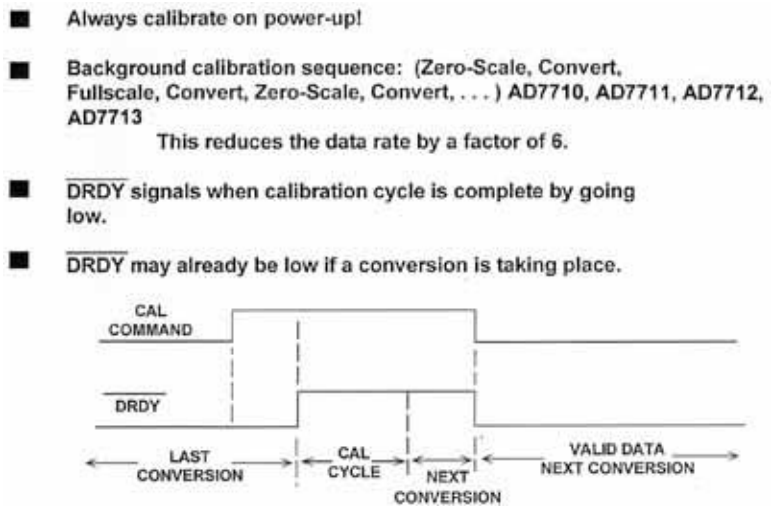



**Figure 3.42**

When calibration is complete, DRDY goes low - but it does not necessarily go high as soon as the calibration command is sent to the ADC, there may be a delay of up to one output data cycle before it does so. Controllers should therefore look for a 0 to 1 transition, rather than the presence of a 0, on DRDY to signal the completion of a calibration after it has been commanded.

Calibration is crucial to achieving the rated accuracy of AD771X devices and should be performed immediately after power-up and repeated regularly. A 1.25µV/°C temperature coefficient of input offset and a 2°C temperature change causes an LSB of error in a 20-bit 2.5V system. Any reference drift adds to the error. Frequent calibration ensures that temperature changes do not degrade the accuracy of conversions.

**CALIBRATE OFTEN TO MAINTAIN ACCURACY**

- **Temperature Drift can cause errors**
  - **Unipolar offset drift of 2.5µV is 1 LSB in a 20 bit system (2.5V full-scale)**
- **Reference voltage drift adds to this error**
- **Calibration can remove gain errors created by input filters**
- **Therefore, to minimize errors, calibrate often.**
- **Always calibrate on power-up!**
- **Calibration coefficients can be manually adjusted**

**Figure 3.43**

When the AD771X executes a calibration cycle, it saves two coefficients in internal registers. One register stores the full scale calibration coefficient, FSC, and the other stores the zero scale calibration coefficient, ZSC. Adjusting the calibration coefficients manually may be useful in some applications. For example, in a weigh scale application it may be necessary to insert an offset to account for a fixed weight. It is possible to read from and write to the calibration registers of members of the AD771X family, making adjustment of calibration coefficients a straightforward task. Details of this procedure are given in References 4 and 8.

A typical application of the AD7710 is in a weigh scale (Figure 3.44). These generally use a resistive bridge as their sensing element and require resolution of at least 16-bits and often more. The AD7710 dramatically simplifies the design of such a system: the bridge is connected directly to its differential inputs, making an external instrumentation amplifier unnecessary. The excitation for the bridge, and the reference for the AD7710, are provided by an AD780, whose low noise helps to preserve the system ENOB. Because the system bandwidth is limited (both by the conversion rate selected and the filter capacitors on the bridge) the ENOB achievable is quite high (approximately 20-bits) but the conversion (and output data) rate is rather low at 10Hz.

**WEIGH SCALE APPLICATION USING THE AD7710**

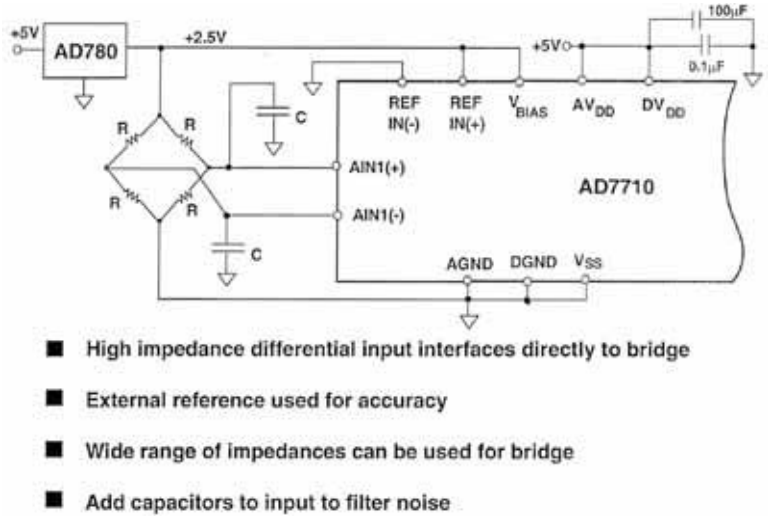



**Figure 3.44**

The converters in the AD771X family all have serial interfaces, which are described in greater detail in the data sheet. They have control registers that control all their operations. Changing the PGA gain, starting a calibration, and changing the filter parameters are all accomplished by writing to the appropriate register. On the other hand, data can be read either as a 16-bit or a 24-bit operation - one of the bits in the control register controls the size of the data word. The DRDY output indicates when a conversion is complete and valid data is available in the output register.

Figure 3.45 shows an isolated 4-wire interface to the AD7713 using common opto-isolators. Over 6kV of isolation is possible. The TFS, A0, and SYNC lines are tied together at the converter to minimize the number of control lines. Tying TFS to AO causes a write to the device to load data to the control register, and any read accesses the data register. The only restrictions of this method of control is that the controller cannot write to the calibration registers and cannot read from the control register. In many applications these capabilities are unnecessary. Four opto-isolators carry data and instructions from the controller to the ADC and a fifth, with a 74HC125 on each side of the isolation barrier, carries data to the controller. The AD7713 is ideal for this particular application because its low supply current minimizes the load on the isolated power supply.

## ISOLATED 4-WIRE INTERFACE USING AD7713

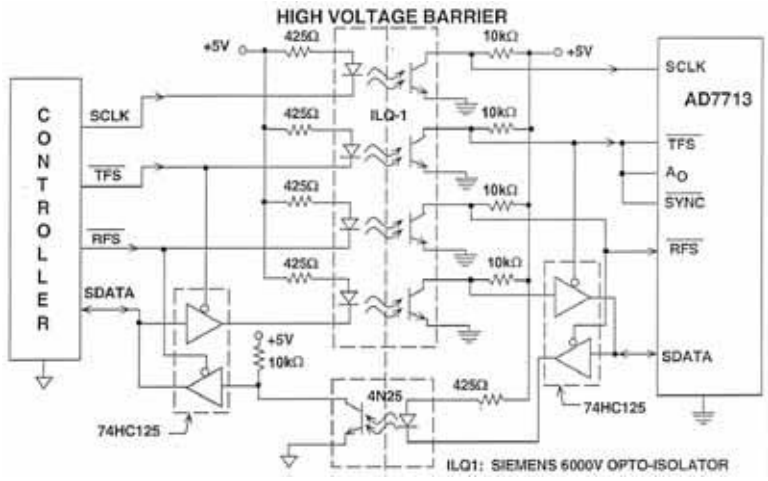



**Figure 3.45**

The AD771X family generally interfaces with some type of microprocessor. Their data sheet includes circuits and micro-code for interfacing to the 8051 and 68HC11 microcontroller and the ADSP-2103/2105 DSP processor. Figure 3.46 shows how the AD7714 may be interfaced to the 68HC11 microcontroller. The diagram shows the minimum (three-wire) interface with CS on the AD7714 hard-wired low. In this scheme, the DRDY bit of the AD7714 Communications Register is monitored to determine when the Data Register is updated. Other schemes are described in the AD7714 data sheet.

**AD7714 TO 68HC11 MICROCONTROLLER INTERFACE**

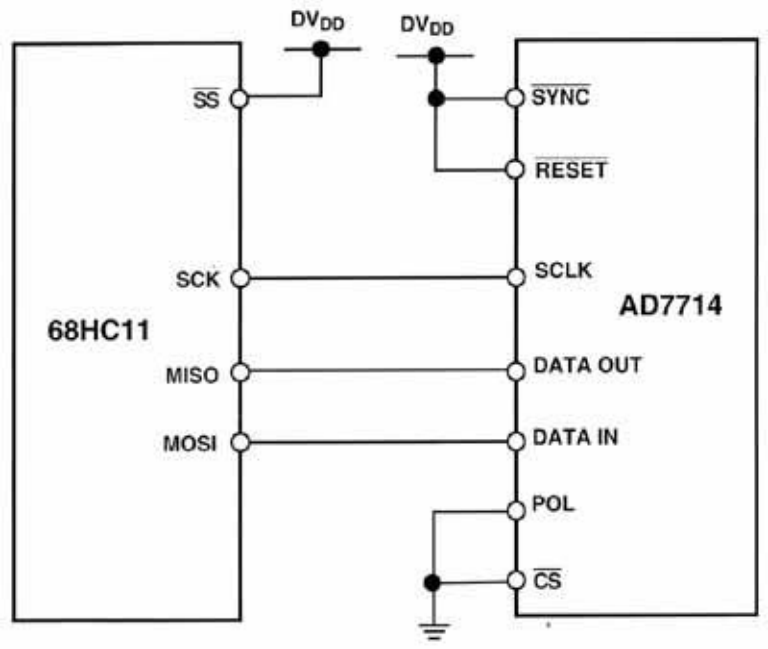



**Figure 3.46**

Interfacing to the ADSP-2103/2105 is also relatively straightforward. The DRDY bit of the Communications Register is again monitored to determine when the Data Register in the AD7714 is updated.

## AD7714 TO ADSP-2103/2105 DSP INTERFACE

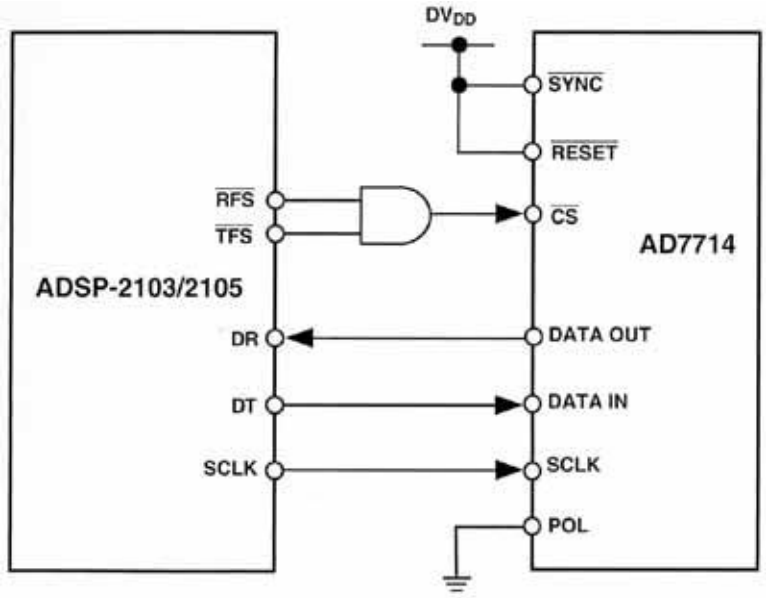



**Figure 3.47**

The AD771X sigma-delta converters are powerful tools for building high accuracy systems. Every one of them combines high resolution, system calibration, a programmable gain amplifier, and high impedance differential inputs with great ease of design. Their adjustable digital filters provides flexibility in the choice of data rates and resolution and their serial interface minimizes their pin count, so that they fit in a 24-pin skinny DIP package, providing a high degree of functionality in a small space.

The AD7714 is especially suitable for low power applications. Figure 3.48 shows the total supply current required as a function of supply voltage for two clock frequencies: 2.4576MHz and 1MHz. These data are for an external clock with the AD7714 operating in the unbuffered mode. Figure 3.48 illustrates an important point which is applicable to a large number of low power data converters - the total power dissipation is a function of the clock frequency! Make sure to check the data sheet carefully for this dependency when estimating the total power requirement. The power dissipation of older, higher-power, bipolar data converters was generally much less sensitive to clock frequency than the modern low-power CMOS designs.

**AD7714 TOTAL SUPPLY CURRENT (EXTERNAL OSCILLATOR)**

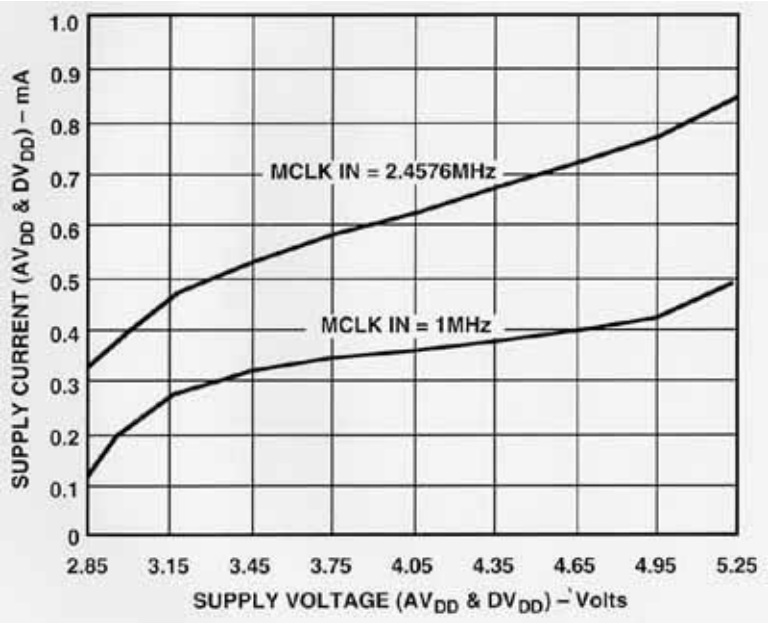



**Figure 3.48**

An area where the low power, single supply, three wire interface capabilities of the AD7714 is of benefit is in smart transmitters (Figure 3.49). The entire smart transmitter must operate from the 4mA to 20mA loop. Tolerances in the loop mean that the amount of current available to power the entire transmitter is as low as 3.5mA. The AD7714 consumes only 500µA, leaving 3mA available for the rest of the transmitter. Not shown in Figure 3.49 is the isolated power source required to power the front end circuits, including the AD7714.

**SMART TRANSMITTER USING AD7714 OPERATES ON 4mA TO 20mA LOOP CURRENT**

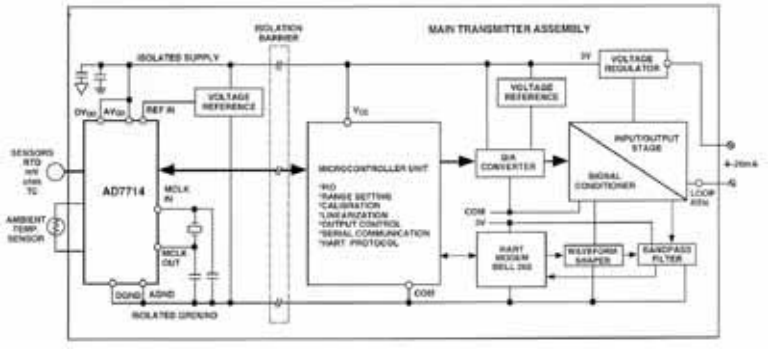



**Figure 3.49**

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