19-3195; Rev 1; 2/05

MAXIM

双通道、低功耗、500Mbps ATE驱动器/比较器，带有35mA负载

概述

MAX9967为双通道、低功耗、高速、引脚电子驱动器/比较器/负载 (DCL) IC，每通道包括三电平引脚驱动器、双路比较器、可调箝位电路和有源负载。驱动器具有较宽的电压范围和高速运行特性，具备高阻和有源端接 (第3级驱动)工作模式，在低电压摆幅下仍可保持高线性。双路比较器在各种输入条件下能够保持很低的偏差 (时序变化)。器件配置为高阻接收器时，箝位电路为高速被测器件 (DUT) 波形提供阻尼衰减。负载可编程，提供最大35mA源出电流和吸入电流。可方便实现接触/连续测试、全速IOH和IOL参数测试，以及对高输出阻抗器件的上拉。

MAX9967A为驱动器提供精确的增益和失调匹配，并为比较器和有源负载提供精确的失调匹配。在成本敏感的系统中，允许多通道共享基准电压。MAX9967B适用于每通道具有独立基准电压的系统设计。

MAX9967提供兼容于ECL、LVPECL、LVDS和GTL的高速差分控制输入，具有可选择的内部端接电阻。比较器提供ECL/LVPECL或具有可选内部上拉电阻的集电极开路输出。这些功能可显著减少电路板分立元件数量。

MAX9967的低泄漏、限摆率和三态/端接工作模式通过3线、低压、CMOS兼容串口编程设置。

MAX9967的工作电压范围为-1.5V至+6.5V，每通道功耗仅为1.15W。器件可提供100引脚、14mm x 14mm面积、0.5mm引脚间距的TQFP封装。封装顶部的8mm x 8mm裸露焊盘可提高散热效率。管芯温度在+70°C至+100°C范围以内时器件可正常工作，具有管芯温度监视输出。

应用

低成本混合信号/片上系统ATE

商用存储器ATE

PCI或VXI可编程数字仪表

特性

- ♦ 低功耗：每通道1.15W (典型值)
- ♦ 高速：3V_{P-P}时，500Mbps
- ♦ 可编程35mA有源负载电流
- ♦ 低时序偏差
- ♦ -1.5V至+6.5V宽工作电压范围
- ♦ 有源端接 (第3级驱动)
- ♦ 低泄漏模式：60nA
- ♦ 集成箝位电路
- ♦ 能够灵活地与多种逻辑电平接口
- ♦ 集成PMU连接
- ♦ 数字设置摆率
- ♦ 内部端接电阻
- ♦ 低增益误差和失调误差

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX9967ADCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967AGCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967ALCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967AMCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967AQCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967ARCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967BDCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967BGCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967BLCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967BMCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9967BQCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9967BRCCQ	0°C to +70°C	100 TQFP-EPR**

** 未来产品——供货信息请与厂商联系。*

*** EPR = 倒置裸露焊盘 (顶部)。*

引脚配置和典型应用电路在数据资料的最后部分给出。

选择指南在数据资料的最后部分给出。

双通道、低功耗、500Mbps ATE 驱动器/比较器，带有35mA负载

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +11.5V
V_{EE} to GND.....-7.0V to +0.3V
V_{CC} - V_{EE}.....-0.3V to +18V
GS to GND .....±1V
DUT_, LDH_, LDL_ to GND .....-2.5V to +7.5V
DATA_, NDATA_, RCV_, NRCV_,
LDEN_, NLDEN_ to GND.....-2.5V to +5.0V
DATA_ to NDATA_, RCV_ to NRCV_,
LDEN_ to NLDEN_.....±1.5V
$V_{CCO\_}$ to GND.....-0.3V to +5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$, TDATA_,
TRCV_, TLDEN_ to GND .....-1.0V to +5V
DHV_, DLV_, DTV_, CHV_, CLV_, COM_,
FORCE_, SENSE_ to GND.....-2.5V to +7.5V
CPHV_ to GND .....-2.5V to +8.5V
CPLV_ to GND.....-3.5V to +7.5V
DHV_ to DLV_.....±10V
DHV_ to DTV_.....±10V
DLV_ to DTV_ .....±10V
CHV_ or CLV_ to DUT_.....±10V
CH_, NCH_, CL_, NCL_ to GND (open collector) ....-2.5V to +5V
CH_, NCH_, CL_, NCL_ to GND (open emitter) ..($V_{CCO\_}$ + 1.0V)
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Current Out of CH_, NCH_, CL_, NCL_ (open emitter) ....+50mA
DHV_, DLV_, DTV_, CHV_, CLV_,
CPHV_, CPLV_ Current.....±10mA
TEMP Current.....-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V.....Continuous
Power Dissipation (T_A = +70°C)
MAX9967_ _CCQ (derate 167mW/°C above +70°C) 13.3W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+125°C
Lead Temperature (soldering, 10s) .....+300°C

**Dissipation wattage values are based on still air with no heat sink. Actual maximum allowable power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		9.5	9.75	10.5	V
Negative Supply	V_{EE}		-6.5	-5.25	-4.5	V
Positive Supply Current (Note 2)	I_{CC}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0		120	155	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, load enabled, driver = high impedance		220	255	
Negative Supply Current (Note 2)	I_{EE}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0		-220	-265	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, load enabled, driver = high impedance		-320	-365	
Power Dissipation	P_D	(Notes 2, 3)		2.3	2.9	W
DUT_ CHARACTERISTICS						
Operating Voltage Range	V_{DUT}	(Note 4)	-1.5		+6.5	V
Leakage Current in High-Impedance Mode	I_{DUT}	LLEAK = 0; 0 ≤ $V_{DUT\_}$ ≤ 3V			±1.5	µA
		LLEAK = 0; $V_{DUT\_}$ = -1.5V, +6.5V			±3	
Leakage Current in Low-Leakage Mode		LLEAK = 1; 0 ≤ $V_{DUT\_}$ ≤ 3V, T_J < +90°C			±60	nA
		LLEAK = 1; $V_{DUT\_}$ = -1.5V, +6.5V; T_J < +90°C			±110	
		LLEAK = 1; 0 ≤ $V_{DUT\_}$ ≤ 3V, $V_{LDL\_}$= $V_{LDH\_}$ = 3.5V; T_J < +90°C			±80	
		LLEAK = 1; $V_{DUT\_}$ = -1.5V, +6.5V; $V_{LDL\_}$ = $V_{LDH\_}$ = 3.5V; T_J < +90°C			±160	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)		4.0		pF
		Driver in high-impedance mode		8.0		
Low-Leakage Enable Time		(Notes 5, 6)		20		µs
Low-Leakage Disable Time		(Notes 6, 7)		20		µs
Low-Leakage Recovery		Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_		4		µs
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_, COM_, LDH_, LDL_)						
Input Bias Current	I_{BIAS}				±25	µA
Settling time		To 0.1% of full-scale change (Note 7)		1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_)						
Input High Voltage	V_{IH}		-1.6		+3.5	V
Input Low Voltage	V_{IL}		-2.0		+3.1	V
Differential Input Voltage	V_{DIFF}		±0.15		±1.0	V
Input Bias Current		MAX9967_DCCQ, MAX9967_MCCQ			±25	µA
Input Termination Voltage	$V_{TDATA\_}$, $V_{TRCV\_}$, $V_{TLDEN\_}$	MAX9967_GCCQ, MAX9967_LCCQ, and MAX9967_QCCQ	-2.1		+3.5	V
Input Termination Resistor		MAX9967_GCCQ, MAX9967_LCCQ, and MAX9967_QCCQ, between signal and corresponding termination voltage input	48		52	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$)						
Internal Threshold Reference	V_{THRINT}		1.05	1.25	1.45	V
Internal Reference Output Resistance	R_O			20		kΩ
External Threshold Reference	V_{THR}		0.43		1.73	V
Input High Voltage	V_{IH}		V_{THR} + 0.2		3.5	V
Input Low Voltage	V_{IL}		-0.1		V_{THR} - 0.2	V
Input Bias Current	I_B				±25	µA
SERIAL INTERFACE TIMING (Figure 6)						
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Pulse-Width High	t_{CH}		8			ns
SCLK Pulse-Width Low	t_{CL}		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}			3.5			ns
DIN to SCLK High Setup	t_{DS}			3.5			ns
DIN to SCLK High Hold	t_{DH}			3.5			ns
$\overline{CS}$ Pulse Width High	t_{CSWH}			20			ns
TEMPERATURE MONITOR (TEMP)							
Nominal Voltage		T_J = +70°C, $R_L \geq 10M\Omega$			3.43		V
Temperature Coefficient					+10		mV/°C
Output Resistance					15		kΩ
DRIVERS (Note 8)							
DC OUTPUT CHARACTERISTICS ($R_L \geq 10M\Omega$)							
DHV_, DLV_, DTV_, Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$, $V_{DTV\_}$, $V_{DLV\_}$ independently tested at +1.5V	MAX9967A			±15	mV
			MAX9967B			±100	
DHV_, DLV_, DTV_, Output Offset Temperature Coefficient					±65		µV/°C
DHV_, DLV_, DTV_, Gain	A_V	Measured with $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ at 0 and 4.5V	MAX9967A (Note 9)	0.999	1.00	1.001	V/V
			MAX9967B	0.96		1.001	
DHV_, DLV_, DTV_, Gain Temperature Coefficient					-35		ppm/°C
Linearity Error		V_{DUT} = 1.5V, 3V (Note 10)				±5	mV
		Full range (Notes 10, 11)				±15	
DHV_ to DLV_ Crosstalk		$V_{DLV\_}$ = 0; $V_{DHV\_}$ = 200mV, 6.5V				±2	mV
DLV_ to DHV_ Crosstalk		$V_{DHV\_}$ = 5V; $V_{DLV\_}$ = -1.5V, +4.8V				±2	mV
DTV_ to DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0; $V_{DTV\_}$ = -1.5V, +6.5V				±2	mV
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DLV\_}$ = 0; $V_{DHV\_}$ = 1.6V, 3V				±3	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0, 1.4V				±3	mV
DHV_, DTV_, DLV_ DC Power-Supply Rejection Ratio	PSRR	(Note 12)		40			dB
Maximum DC Drive Current	$I_{DUT\_}$			±60		±120	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 13)		49	50	51	Ω
DC Output Resistance Variation	$\Delta R_{DUT\_}$	$I_{DUT\_}$ = ±1mA to ±8mA			0.5		Ω
		$I_{DUT\_}$ = ±1mA to ±40mA			1	2.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sense Resistance	R_{SENSE}		7.50	10	13.75	kΩ
Force Resistance	R_{FORCE}		320	400	500	Ω
Force Capacitance	C_{FORCE}			2		pF
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)						
Drive-Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V		30		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		40		
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V		50		
Term-Mode Overshoot		(Note 14)		0		mV
Settling Time to Within 25mV		3V step (Note 15)		10		ns
Settling Time to Within 5mV		3V step (Note 15)		20		ns
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 16)						
Prop Delay, Data to Output	t_{PDD}			2.2		ns
Prop Delay Match, t_{LH} vs. t_{HL}		$3V_{P-P}$		±50		ps
Prop Delay Match, Drivers Within Package		(Note 17)		40		ps
Prop Delay Temperature Coefficient				+3		ps/°C
Prop Delay Change vs. Pulse Width		$3V_{P-P}$, 40MHz, 2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width		±60		ps
Prop Delay Change vs. Common-Mode Voltage		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		85		ps
Prop Delay, Drive to High Impedance	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0		3.2		ns
Prop Delay, High Impedance to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0		3.3		ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V		2.5		ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V		2.2		ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)						
Rise and Fall Time	t_R, t_F	$0.2V_{P-P}$, 20% to 80%		370		ps
		$1V_{P-P}$, 10% to 90%		630		
		$3V_{P-P}$, 10% to 90%	1.0	1.3	1.5	ns
		$5V_{P-P}$, 10% to 90%		2.0		
Rise and Fall Time Match	t_R vs. t_F	$3V_{P-P}$, 10% to 90%		±0.03		ns
SC1 = 0, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		75		%
SC1 = 1, SC0 = 0 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		50		%
SC1 = 1, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%		25		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Pulse Width (Note 18)		$0.2V_{P-P}$			650		ps
		$1V_{P-P}$			1.0		ns
		$3V_{P-P}$			2.0		
		$5V_{P-P}$			2.9		
Data Rate (Note 19)		$0.2V_{P-P}$			1700		Mbps
		$1V_{P-P}$			1000		
		$3V_{P-P}$			500		
		$5V_{P-P}$			350		
Dynamic Crosstalk		(Note 20)			10		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1a (Note 21)			1.6		ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1b (Note 21)			0.7		ns
COMPARATORS (Note 8)							
DC CHARACTERISTICS							
Input Voltage Range	V_{IN}	(Note 4)		-1.5		+6.5	V
Differential Input Voltage	V_{DIFF}			±8			V
Hysteresis	V_{HYST}				0		mV
Input Offset Voltage	V_{OS}	$V_{DUT\_}$ = 1.5V	MAX9967A			±20	mV
			MAX9967B			±100	
Input Offset Voltage Temperature Coefficient					±50		µV/°C
Common-Mode Rejection Ratio (Note 22)	CMRR	$V_{DUT\_}$ = 0, 3V		47	78		dB
		$V_{DUT\_}$ = 0, 6.5V		54	78		
		$V_{DUT\_}$ = -1.5V, +6.5V		44	61		
Linearity Error (Note 10)		$V_{DUT\_}$ = 1.5V, 3V				±3	mV
		$V_{DUT\_}$ = 6.5V				±5	
		$V_{DUT\_}$ = -1.5V				±25	
V_{CC} Power-Supply Rejection Ratio (Note 12)	PSRR	$V_{DUT\_}$ = -1.5V, +6.5V		57	80		dB
V_{EE} Power-Supply Rejection Ratio (Note 12)	PSRR	$V_{DUT\_}$ = 0, 6.5V		44	64		dB
		$V_{DUT\_}$ = -1.5V		33	60		
AC CHARACTERISTICS (Note 23)							
Minimum Pulse Width (Note 24)	$t_{PW(MIN)}$	MAX9967_DCCQ, MAX9967_GCCQ, MAX9967_LCCQ, MAX9967_RCCQ			0.7		ns
		MAX9967_MCCQ, MAX9967_QCCQ			0.85		
Prop Delay	t_{PDL}				2.2		ns
Prop Delay Temperature Coefficient					+6		ps/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Prop Delay Match, High/Low vs. Low/High					±25		ps
Prop Delay Match, Comparators Within Package		(Note 17)			35		ps
Prop Delay Dispersion vs. Common-Mode Input (Note 25)		$V_{CHV\_}$ = $V_{CLV\_}$ = 0, 6.4V			±75		ps
		$V_{CHV\_}$ = $V_{CLV\_}$ = -1.4V			±175		
Prop Delay Dispersion vs. Overdrive		100mV to 1V			220		ps
Prop Delay Dispersion vs. Pulse Width		2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width			±40		ps
Prop Delay Dispersion vs. Slew Rate		0.5V/ns to 2V/ns slew rate			100		ps
Waveform Tracking 10% to 90%		$V_{DUT\_}$ = $1.0V_{P-P}$, t_R = t_F = 1.0ns, 10% to 90% relative to timing at 50% point	Term mode		250		ps
			High-Z mode		500		
OPEN-COLLECTOR LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_: MAX9967_DCCQ, MAX9967_GCCQ, MAX9967_LCCQ, and MAX9967_RCCQ)							
$V_{CCO\_}$ Voltage Range	$V_{VCCO\_}$			0		3.5	V
Output Low-Voltage Compliance		Set by I_{OL}, R_{TERM}, and $V_{CCO\_}$			-0.5		V
Output High Current	I_{OH}	MAX9967_DCCQ, MAX9967_GCCQ		-0.05	0	+0.10	mA
Output Low Current	I_{OL}	MAX9967_DCCQ, MAX9967_GCCQ		7.6	8	8.4	mA
Output High Voltage	V_{OH}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9967_LCCQ, MAX9967_RCCQ		$V_{CCO\_}$ - 0.05	$V_{CCO\_}$ - 0.005		V
Output Low Voltage	V_{OL}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9967_LCCQ, MAX9967_RCCQ			$V_{CCO\_}$ - 0.4		V
Output Voltage Swing		$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9967_LCCQ, MAX9967_RCCQ		360	390	440	mV
Output Termination Resistor	R_{TERM}	Single-ended measurement from $V_{CCO\_}$ to CH_, NCH_, CL_, NCL_, MAX9967_LCCQ, MAX9967_RCCQ		48		52	Ω
Differential Rise Time	t_R	20% to 80%	MAX9967_DCCQ, MAX9967_GCCQ, R_{TERM} = 50Ω at end of line		280		ps
			MAX9967_LCCQ, MAX9967_RCCQ				
Differential Fall Time	t_F	20% to 80%	MAX9967_DCCQ, MAX9967_GCCQ, R_{TERM} = 50Ω at end of line		280		ps
			MAX9967_LCCQ, MAX9967_RCCQ				
OPEN-EMITTER LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_: MAX9967_MCCQ and MAX9967_QCCQ)							
$V_{CCO\_}$ Voltage Range	$V_{VCCO\_}$			-0.1		+3.5	V
$V_{CCO\_}$ Supply Current	$I_{VCCO\_}$	All outputs 50Ω to ($V_{VCCO\_}$ - 2V)			165		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	50Ω to ($V_{VCCO\_}$ - 2V)		$V_{CCO\_}$ - 1.0	$V_{CCO\_}$ - 0.85		V
Output Low Voltage	V_{OL}	50Ω to ($V_{VCCO\_}$ - 2V)			$V_{CCO\_}$ - 1.7	$V_{CCO\_}$ - 1.6	V
Output Voltage Swing		50Ω_to ($V_{VCCO\_}$ - 2V)		800	850	900	mV
Differential Rise Time	t_R	20% to 80%			370		ps
Differential Fall Time	t_F	20% to 80%			370		ps
CLAMPS							
High Clamp Input Voltage Range	$V_{CPH\_}$			-0.3		+7.5	V
Low Clamp Input Voltage Range	$V_{CPL\_}$			-2.5		+5.3	V
Clamp Offset Voltage	V_{OS}	At DUT_ with $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0				±100	mV
		At DUT_ with $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0				±100	
Offset Voltage Temperature Coefficient					±0.5		mV/°C
Clamp Power-Supply Rejection Ratio (Note 12)	PSRR	$I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0			54		dB
		$I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0			54		
Voltage Gain	A_V			0.96		1.00	V/V
Voltage Gain Temperature Coefficient					-100		ppm/°C
Clamp Linearity		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.5V, $V_{CPHV\_}$ = -0.3V to +6.5V			±10		mV
		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = -1.5V to +5.3V			±10		
Short-Circuit Output Current	$I_{SCDUT\_}$	$V_{CPHV\_}$ = 0, $V_{CPLV\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V		50		95	mA
		$V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = 5V, $V_{DUT\_}$ = -1.5V		-95		-50	mA
Clamp DC Impedance	R_{OUT}	$V_{CPHV\_}$ = 3V, $V_{CPLV\_}$ = 0, $I_{DUT\_}$ = ±5mA and ±15mA		50		55	Ω
ACTIVE LOAD ($V_{COM\_}$ = +1.5V, R_L > 1MΩ, driver in high-impedance mode, unless otherwise noted)							
COM_ Voltage Range	$V_{COM\_}$			-1.5		+5.7	V
Differential Voltage Range		$V_{DUT\_}$ - $V_{COM\_}$		-7.2		+8.0	V
COM_ Offset Voltage	Vos	I_{SOURCE} = I_{SINK} = 20mA	MAX9967A			±15	mV
			MAX9967B			±100	
Offset Voltage Temperature Coefficient					50		µV/°C
COM_ Voltage Gain	A_V	$V_{COM\_}$ = 0, 4.5V, I_{SOURCE} = I_{SINK} = 20mA		0.98		1.00	V/V
Voltage Gain Temperature Coefficient					±25		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COM_ Linearity Error		$V_{COM\_}$ = -1.5V, +5.7V; I_{SOURCE} = I_{SINK} = 20mA (Note 10)			±3	±15	mV
COM_ Output-Voltage Power-Supply Rejection Ratio	PSRR	$V_{COM\_}$ = 2.5V, I_{SOURCE} = I_{SINK} = 20mA		40			dB
Output Resistance, Sink or Source	Ro	I_{SOURCE} = I_{SINK} = 35mA; $V_{DUT\_}$ = 3V, 6.5V with $V_{COM\_}$ = -1.5V and $V_{DUT\_}$ = -1.5V, +2V with $V_{COM\_}$ = 5.7V		25			kΩ
		I_{SOURCE} = I_{SINK} = 1mA; $V_{DUT\_}$ = 3V, 6.5V with $V_{COM\_}$ = -1.5V and $V_{DUT\_}$ = -1.5V, +2V with $V_{COM\_}$ = 5.7V		500			kΩ
Output Resistance, Linear Region	Ro	$I_{DUT\_}$ = ±10mA, I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 2.5V			6		Ω
Deadband		$V_{COM\_}$ = 2.5V, 95% I_{SOURCE} to 95% I_{SINK}			400	700	mV
SOURCE CURRENT ($V_{DUT\_}$ = 4.5V)							
Maximum Source Current		$V_{LDL\_}$ = 3.8V		36		40	mA
Source Programming Gain	A_{TC}	$V_{LDL\_}$ = 0.3V, 3V; V_{LDH} = 0.1V		9.9	10	10.1	mA/V
Source Current Offset (Combined Offset of LDL_ and GS)	I_{OS}	$V_{LDL\_}$ = 20mV	MAX9967A (Note 9)	10		50	µA
			MAX9967B	0		200	
Source Current Temperature Coefficient		I_{SOURCE} = 35mA			-6		µA/°C
Source Current Power-Supply Rejection Ratio	PSRR	I_{SOURCE} = 25mA				±70	µA/V
		I_{SOURCE} = 35mA				±84	
Source Current Linearity (Note 26)		$V_{LDL\_}$ = 100mV, 1V, 2.5V				±60	µA
		$V_{LDL\_}$ = 3.5V				±130	
SINK CURRENT ($V_{DUT\_}$ = -1.5V)							
Maximum Sink Current		$V_{LDH\_}$ = 3.8V		-40		-36	mA
Sink Programming Gain	A_{TC}	$V_{LDH\_}$ = 0.3V, 3V; $V_{LDL\_}$ = 0.1V		-10.1	-10	-9.9	mA/V
Sink Current Offset (Combined Offset of LDH_ and GS)	I_{OS}	$V_{LDH\_}$ = 20mV	MAX9967A (Note 9)	-50		-10	µA
			MAX9967B	-200		0	
Sink Current Temperature Coefficient		I_{SINK} = 35mA			+6		µA/°C
Sink Current Power-Supply Rejection Ratio	PSRR	I_{SINK} = 25mA				±70	µA /V
		I_{SINK} = 35mA				±84	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sink Current Linearity (Note 26)		$V_{LDH\_}$ = 100mV, 1V, 2.5V			±60	µA
		$V_{LDH\_}$ = 3.5V			±130	
GROUND SENSE						
GS Voltage Range	V_{GS}	Verified by GS common-mode error test	±250			mV
GS Common-Mode Error		$V_{DUT\_}$ = -1.5V, V_{GS} = ±250mV, $V_{LDH\_}$- V_{GS} = 0.1V			±25	µA
		$V_{DUT\_}$ = +4.5V, V_{GS} = ±250mV, $V_{LDL\_}$ - V_{GS} = 0.1V			±25	
GS Input Bias Current		V_{GS} = 0			±25	µA
AC CHARACTERISTICS (Z_L = 50Ω to GND)						
Enable Time (Note 27)	t_{EN}	I_{SOURCE} = 20mA, $V_{COM\_}$ = -1.5V		2.2		ns
		I_{SINK} = 20mA, $V_{COM\_}$ = +1.5V				
Disable Time (Note 27)	t_{DIS}	I_{SOURCE} = 20mA, $V_{COM\_}$ = -1.5V		1.9		ns
		I_{SINK} = 20mA, $V_{COM\_}$ = +1.5V				
Current Settling Time on Commutation		I_{SOURCE} = I_{SINK} = 1mA and 35mA (Notes 7, 28) To 10%		10		ns
		To 1.5%		50		
Spike During Enable/Disable Transition		I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 0		100		mV

Note 1: All minimum and maximum limits are 100% production tested. Tests are performed at nominal supply voltages unless otherwise noted.

Note 2: Total for dual device at worst-case setting. $R_L \geq 10M\Omega$. The supply currents are measured with typical supply voltages.

Note 3: Does not include internal dissipation of the comparator outputs. With output loads of 50Ω to (V_{VCCO} - 2V), this adds 120mW (typ) to the total device power (MAX9967_MCCQ and MAX9967_QCCQ). For MAX9967_LCCQ, additional power dissipation is typically (32mA x V_{VCCO}).

Note 4: Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.

Note 5: Transition time from LLEAK being asserted to leakage current dropping below specified limits.

Note 6: Based on simulation results only.

Note 7: Transition time from LLEAK being deasserted to output returning to normal operating mode.

Note 8: With the exception of Offset and Gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 9: Measured at V_{CC} = +9.75, V_{EE} = -5.25V, and T_J = +85°C.

Note 10: Relative to straight line between 0 and 4.5V.

Note 11: Specifications measured at the end points of the full range. Full ranges are -1.3V ≤ $V_{DHV\_}$ ≤ 6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ 6.3V, -1.5V ≤ $V_{DTV\_}$ ≤ 6.5V.

Note 12: Change in offset voltage with power supplies independently set to their minimum and maximum values.

Note 13: Nominal target value is 50Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Note 14: $V_{DTV\_}$ = +1.5V, R_S = 50Ω. External signal driven into T-line is a 0 to +3V edge with 1.2ns rise time (10% to 90%). Measurement is made using the comparator.

Note 15: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 16: Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of differential inputs DATA_ and RCV_ is 250ps (10% to 90%).

Note 17: Rising edge to rising edge or falling edge to falling edge.

Note 18: Specified amplitude is programmed. At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

Note 19: Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 95% of its programmed amplitude may be generated at one-half this frequency.

Note 20: Crosstalk from either driver to the other. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channel is in term mode with $V_{DTV\_}$ = +1.5V.

Note 21: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_} < V_{DTV\_} < V_{DHV\_}$. If $V_{DTV\_} < V_{DLV\_}$ or $V_{DTV\_} > V_{DHV\_}$, switching speed is degraded by approximately a factor of 3.

Note 22: Change in offset voltage over the input range.

Note 23: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to +2V, $V_{CHV\_}$ = $V_{CLV\_}$ = +1V, slew rate = 2V/ns, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = 0. Comparator outputs are terminated with 50Ω to GND at scope input with $V_{CCO\_}$ = 2V. Open-collector outputs are also terminated (internally or externally) with R_{TERM} = 50Ω to $V_{CCO\_}$. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.

Note 24: $V_{DUT\_}$ = 0 to +1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V. At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.

Note 25: Relative to propagation delay at $V_{CHV\_}$ = $V_{CLV\_}$ = +1.5V. $V_{DUT\_}$ = $200mV_{P-P}$. Overdrive = 100mV.

Note 26: Relative to segmented interpolations between 20mV, 200mV, 2V, and 3V.

Note 27: Measured from the crossing point of LDEN_ inputs to the 10% point of the output voltage change.

Note 28: $V_{COM\_}$ = 1.5V, R_S = 50Ω, driving voltage = +4V to -1V transition and -1V to +4V transition. Settling time is measured from $V_{DUT\_}$ = 1.5V to I_{SINK}/I_{SOURCE} settling within specified tolerance.

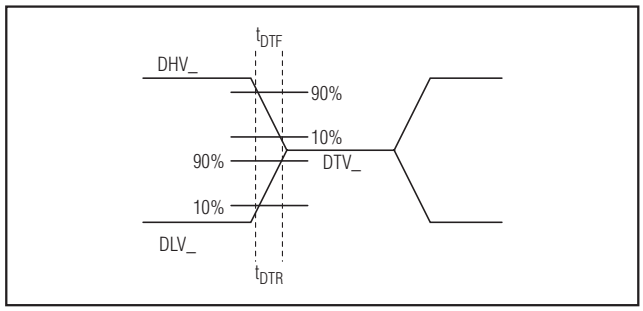


图 1a. 驱动至终端的上升和下降时间

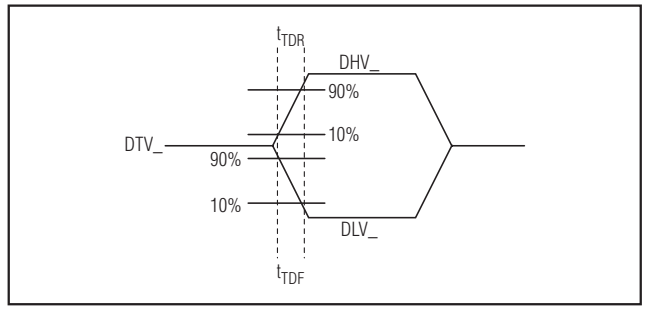
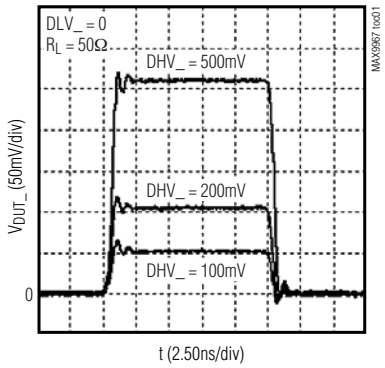


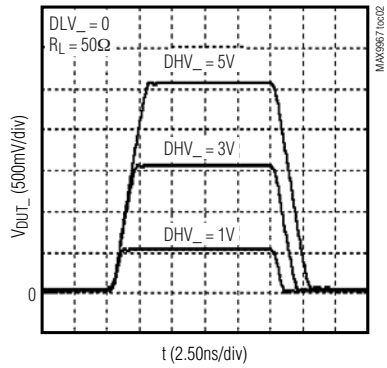
图 1b. 终端至驱动的上升和下降时间

典型工作特性

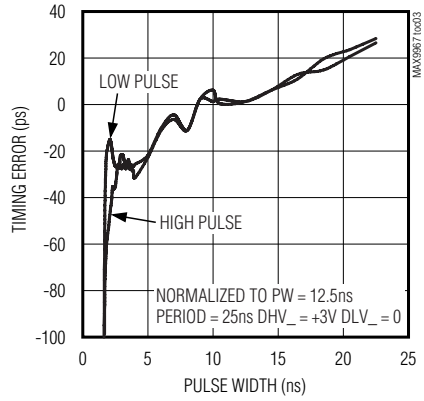
DRIVER SMALL-SIGNAL RESPONSE



DRIVER LARGE-SIGNAL RESPONSE



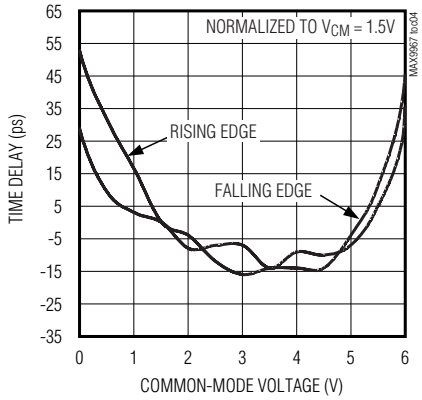
DRIVER TRAILING EDGE TIMING ERROR vs. PULSE WIDTH



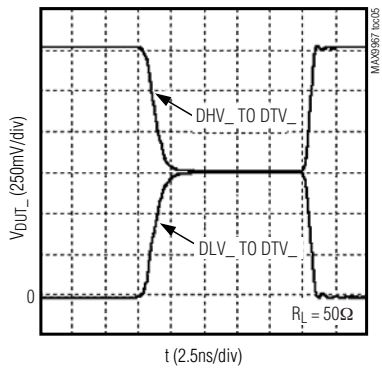
双通道、低功耗、500Mbps ATE驱动器/比较器，带有35mA负载

典型工作特性 (续)

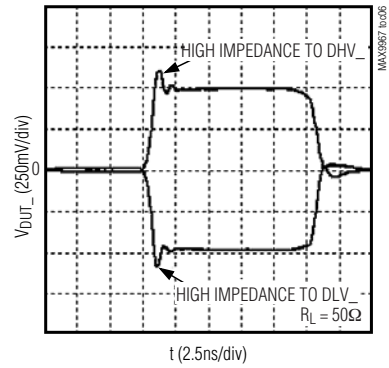
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



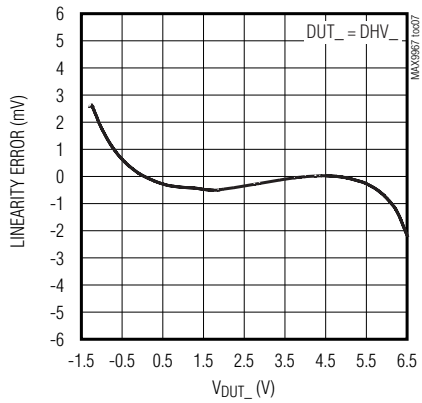
DRIVE-TO-TERM TRANSITION



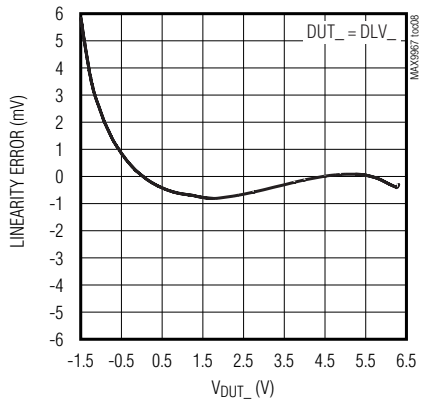
HIGH IMPEDANCE TO DRIVE TRANSITION



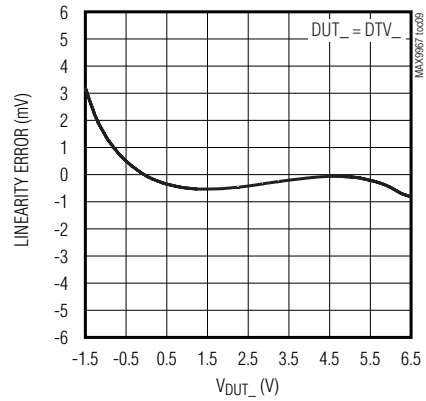
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



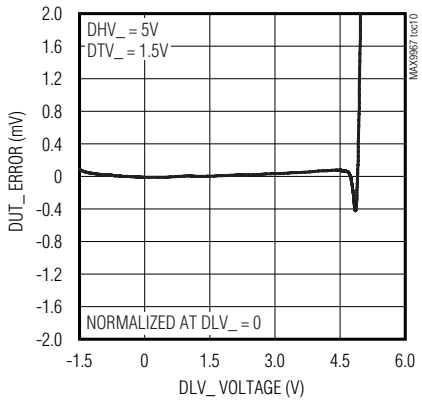
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



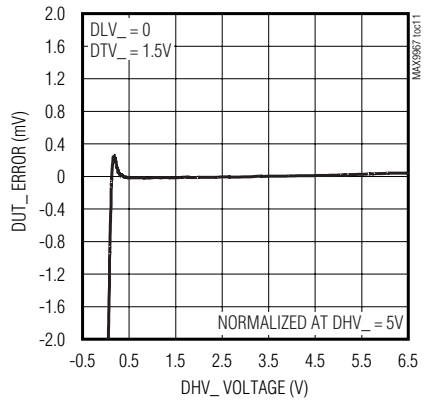
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



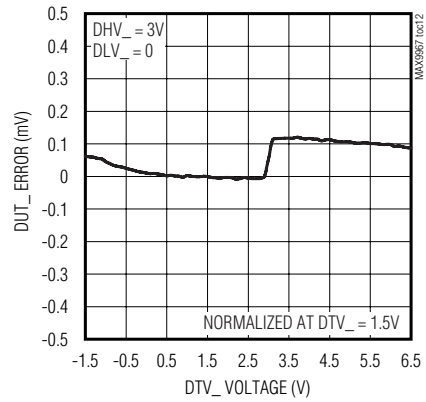
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_

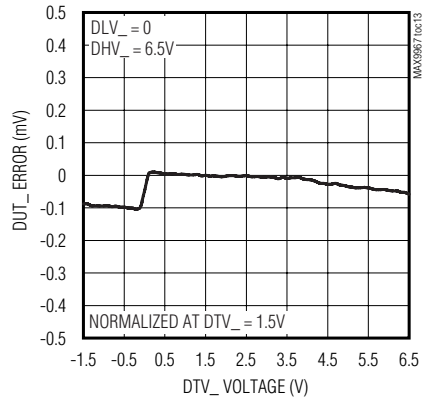


CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_

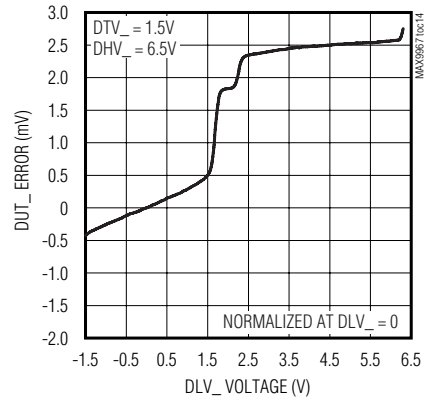


典型工作特性 (续)

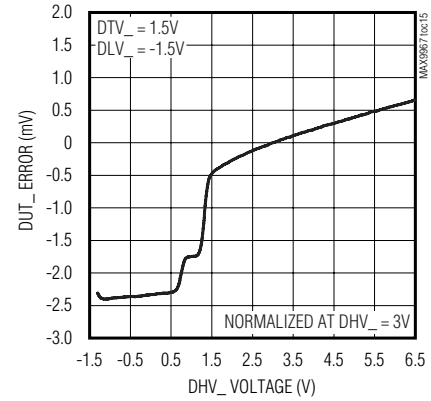
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



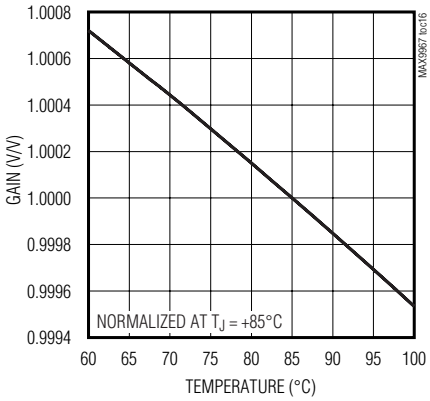
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



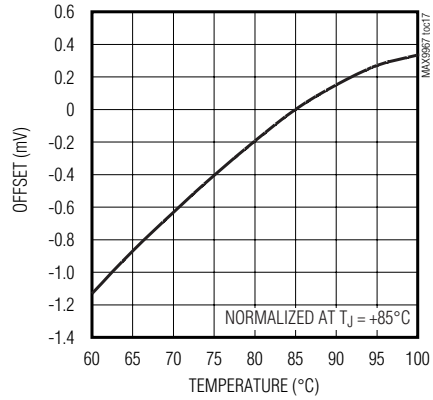
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



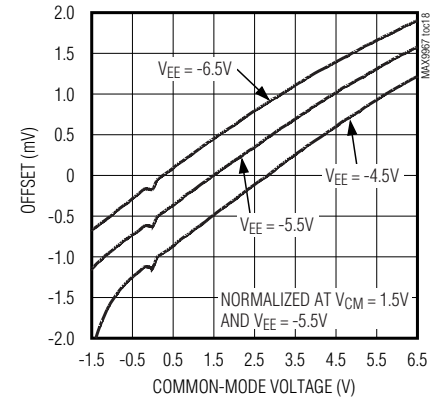
DRIVER GAIN vs. TEMPERATURE



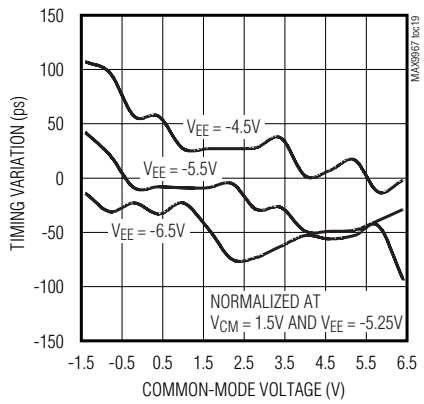
DRIVER OFFSET vs. TEMPERATURE



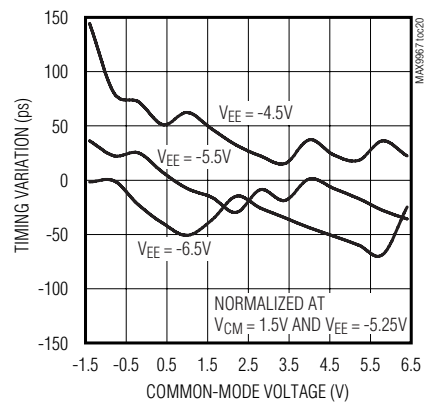
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



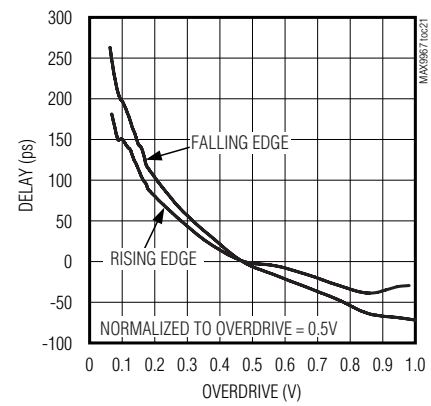
COMPARATOR RISING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE



COMPARATOR FALLING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE

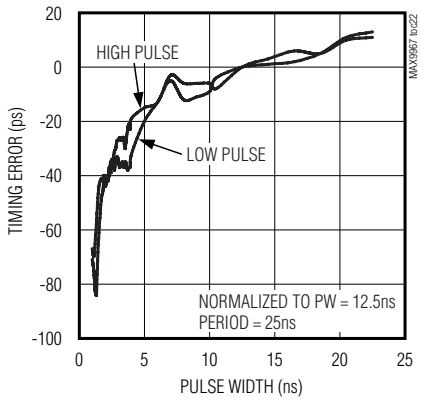


COMPARATOR TIMING VARIATION vs. OVERDRIVE

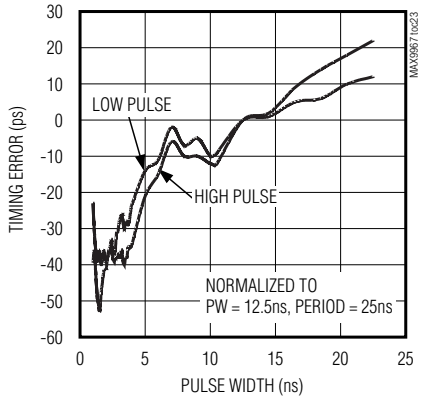


典型工作特性 (续)

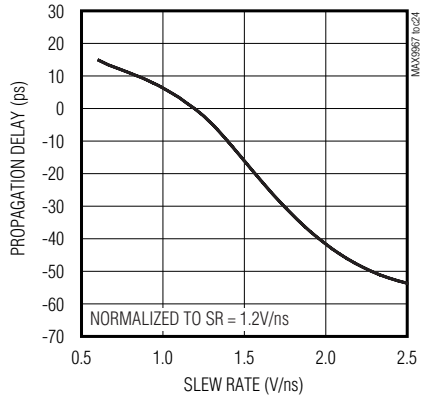
COMPARATOR TRAILING TIMING ERROR vs. PULSE WIDTH, MAX9967_LCCQ



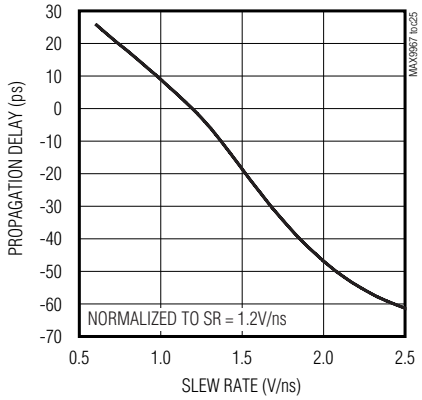
COMPARATOR TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH, MAX9967_MCCQ



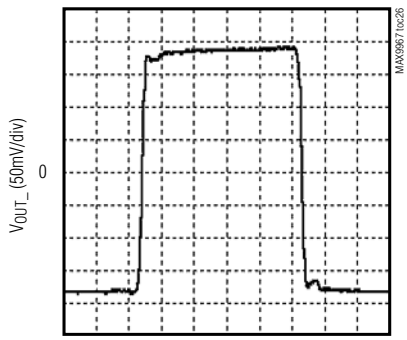
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_ RISING



COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_ FALLING

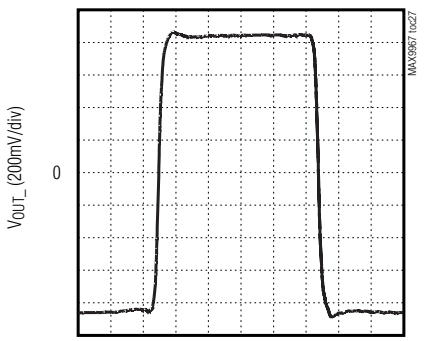


COMPARATOR DIFFERENTIAL OUTPUT RESPONSE (MAX9967_LCCQ)



$V_{DUT\_}$ = 0 TO 3V PULSE, CHV_ = CLV_ = +1.5V, EXTERNAL LOAD = 50Ω

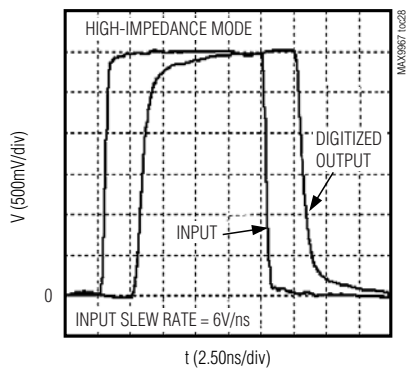
COMPARATOR DIFFERENTIAL OUTPUT RESPONSE (MAX9967_MCCQ)



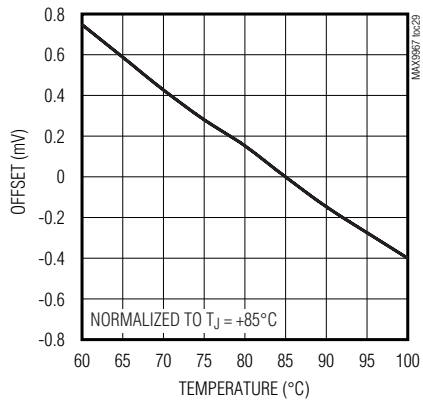
V_{DUT} = 0 TO 3V PULSE, CHV_ = CLV_ = 1.5V, EXTERNAL LOAD = 50Ω

典型工作特性 (续)

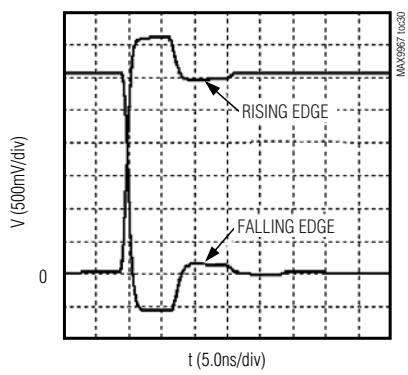
COMPARATOR RESPONSE HIGH SLEW-RATE OVERDRIVE



COMPARATOR OFFSET vs. TEMPERATURE

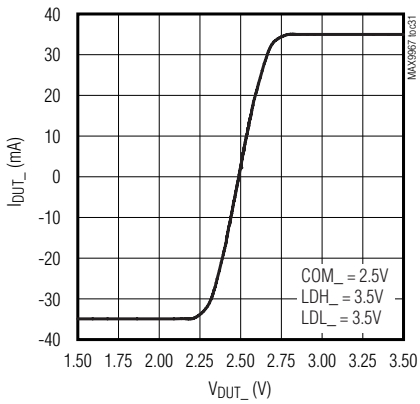


CLAMP RESPONSE

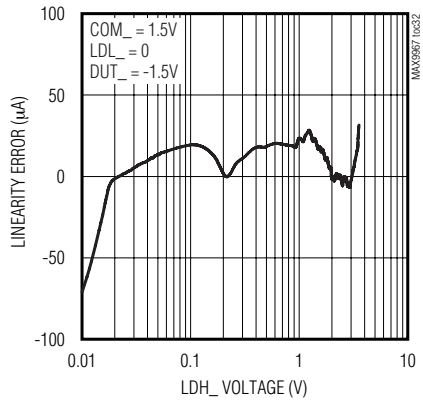


DUT_ = 0 TO 3V SQUARE WAVE
R_S = 25Ω
CPLV_ = -0.1V CPHV_ = +3.1V

ACTIVE-LOAD VOLTAGE vs. CURRENT

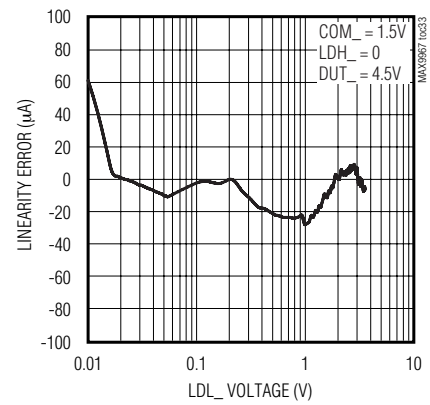


ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. LDH_



CALIBRATION POINTS AT
LDH_ = 20mV, 200mV, 2V, 3V

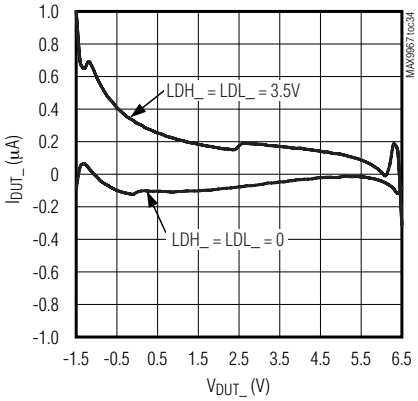
ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. LDL_



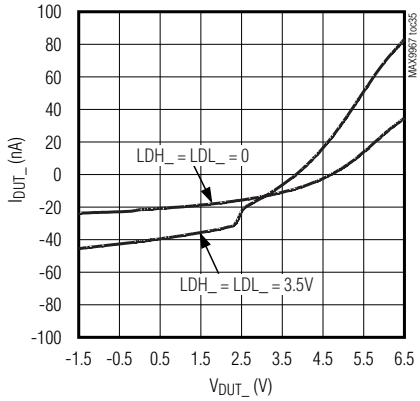
CALIBRATION POINTS AT
LDL_ = 20mV, 200mV, 2V, 3V

典型工作特性 (续)

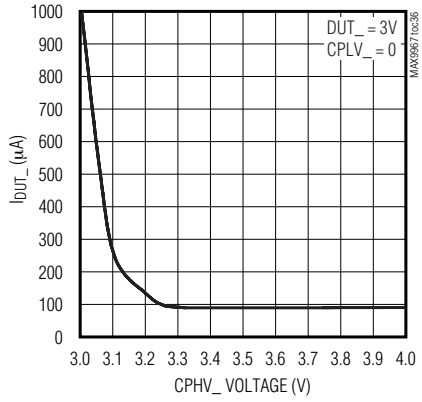
HIGH-IMPEDANCE LEAKAGE CURRENT vs. DUT_ VOLTAGE



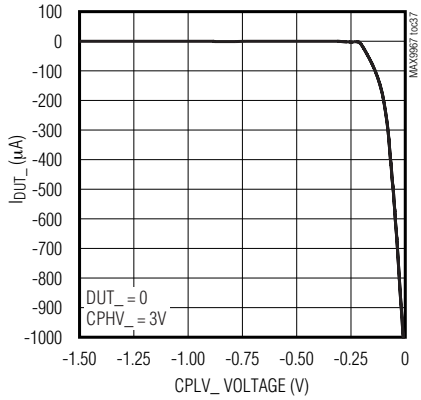
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



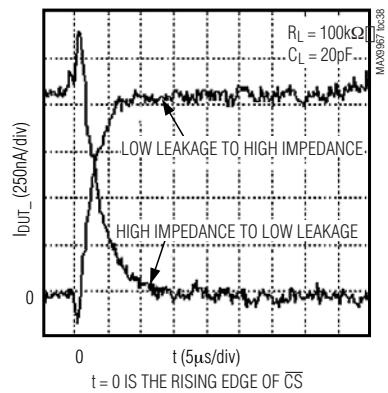
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



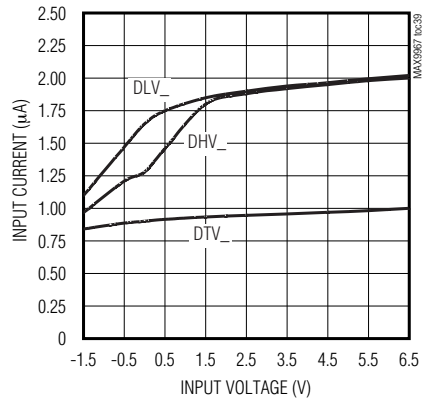
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



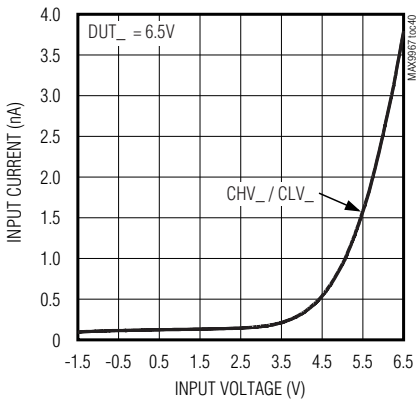
HIGH-IMPEDANCE TO LOW-LEAKAGE TRANSITION



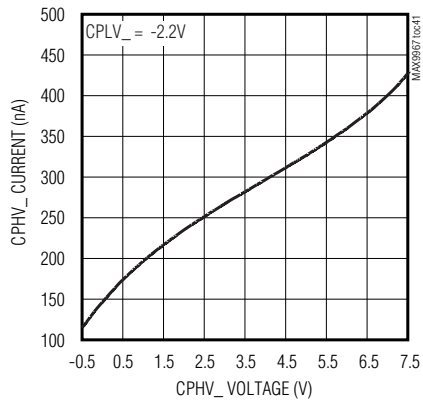
DRIVER REFERENCE CURRENT vs. DRIVER REFERENCE VOLTAGE



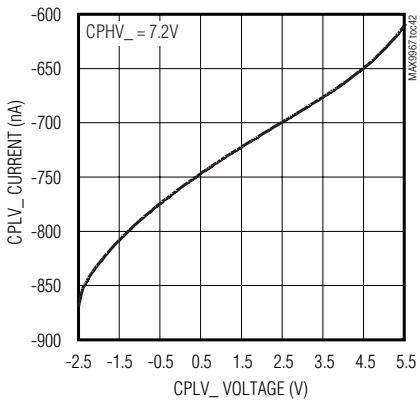
COMPARATOR REFERENCE INPUT CURRENT vs. INPUT VOLTAGE



INPUT CURRENT vs. INPUT VOLTAGE, CPHV_

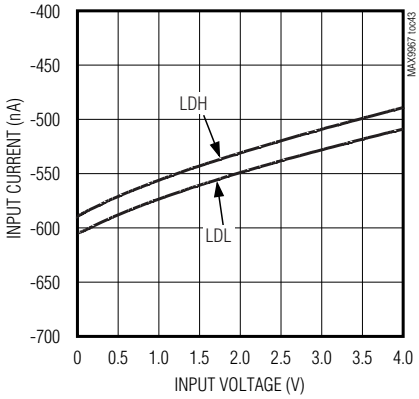


INPUT CURRENT vs. INPUT VOLTAGE, CPLV_

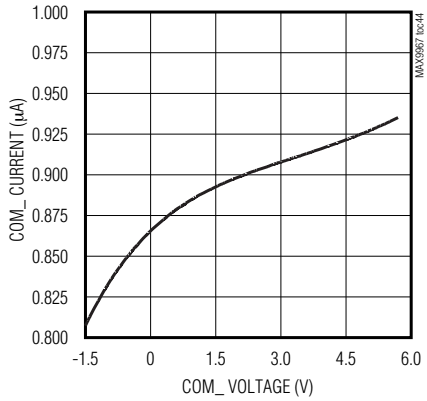


典型工作特性 (续)

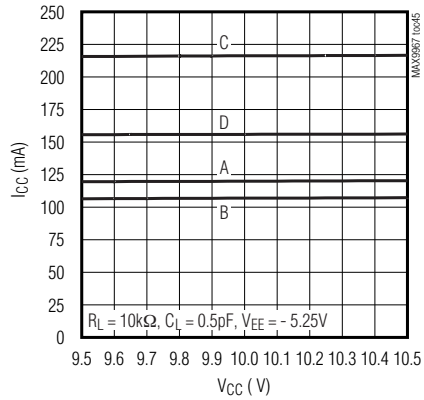
LOAD REFERENCES INPUT CURRENTS vs. INPUT VOLTAGE



INPUT CURRENTS vs. INPUT VOLTAGE, COM_

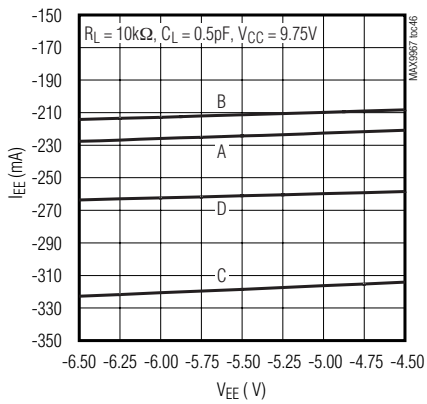


SUPPLY CURRENT, I_{CC} vs. V_{CC}



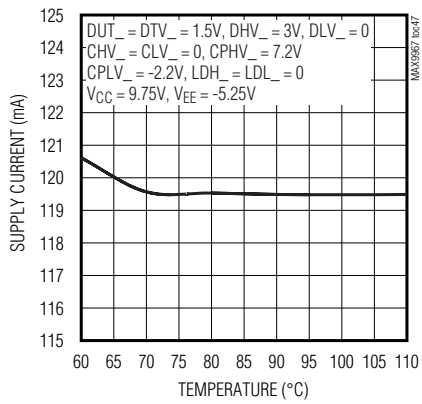
A: DUT_ = DTV_ = 1.5V, DHV_ = 3V, DLV_ = 0, CHV_ = CLV_ = 0, CPHV_ = 7.2V, CPLV_ = -2.2V, LDH_ = LDL_ = 0
$I_{SOURCE} = I_{SINK} = 0$
B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED
C: SAME AS B EXCEPT $I_{SOURCE} = I_{SINK} = 35mA$
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

SUPPLY CURRENT, I_{EE} vs. V_{EE}

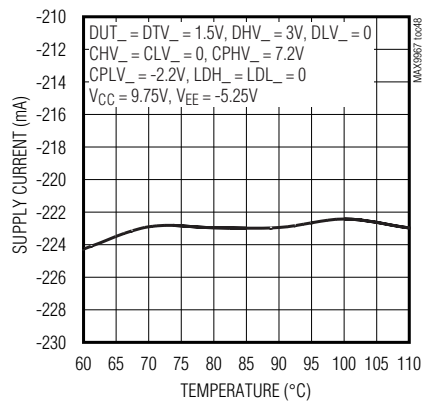


A: DUT_ = DTV_ = 1.5V, DHV_ = 3V, DLV_ = 0, CHV_ = CLV_ = 0, CPHV_ = 7.2V, CPLV_ = -2.2V, LDH_ = LDL_ = 0
$I_{SOURCE} = I_{SINK} = 0$
B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED
C: SAME AS B EXCEPT $I_{SOURCE} = I_{SINK} = 35mA$
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

I_{CC} vs. TEMPERATURE



I_{EE} vs. TEMPERATURE



双通道、低功耗、500Mbps ATE驱动器/比较器，带有35mA负载

引脚说明

引脚	名称	功能
1	TEMP	温度监视输出。
2, 9, 12, 14, 17, 24, 35, 45, 46, 60, 80, 81, 91	V_{EE}	负电源输入。
3, 5, 10, 16, 21, 23, 25, 34, 43, 44, 82, 83, 92	GND	接地端。
4, 11, 15, 22, 33, 41, 42, 66, 84, 85, 93	V_{CC}	正电源输入。
6	FORCE1	通道1来自外部PMU的加载输入。
7	DUT1	通道1被测器件输入/输出。多功能组合I/O用于驱动器、比较器、箝位电路和负载。
8	SENSE1	通道1至外部PMU的检测输出。
13	GS	地检测端。GS是LDH_和LDL_的地参考端。
18	SENSE2	通道2至外部PMU的检测输出
19	DUT2	通道2被测器件输入/输出。多功能组合I/O用于驱动器、比较器、箝位电路和负载。
20	FORCE2	通道2来自外部PMU的加载输入。
26	CLV2	通道2低端比较器基准输入。
27	CHV2	通道2高端比较器基准输入。
28	DLV2	通道2驱动器低端基准输入。
29	DTV2	通道2驱动器端接基准输入。
30	DHV2	通道2驱动器高端基准输入。
31	CPLV2	通道2低端箝位基准输入。
32	CPHV2	通道2高端箝位基准输入。
36	NCH2	通道2比较器高端输出。通道2高端比较器差分输出。
37	CH2	
38	V_{CCO2}	通道2集电极电压输入。通道2比较器输出上拉电阻的加载电压。对于集电极开路输出，这是内部端接电阻的上拉电压。对于射级开路输出，这是输出晶体管的集电极电压。对于内部没有端接电阻的集电极开路版本，内部未连接。
39	NCL2	通道2比较器低端输出。通道2低端比较器差分输出。
40	CL2	
47	COM2	通道2有源负载换流电压基准输入。
48	LDL2	通道2有源负载源出电流基准输入。
49	LDH2	通道2有源负载吸入电流基准输入。
50, 76	N.C.	无连接。不要连接。
51	TDATA2	通道2数据端接电压输入。DATA2和NDATA2差分输入的端接电压输入。对于没有内部端接电阻的器件，内部未连接。
52	NDATA2	通道2多路复用器控制输入。通过差分控制输入DATA2和NDATA2选择DHV2或DLV2作为驱动器2的输入。DATA2高于NDATA2时选择DHV2；NDATA2高于DATA2时选择DLV2。
53	DATA2	

引脚说明 (续)

引脚	名称	功能
54	TRCV2	通道2 RCV端接电压输入。RCV2和NRCV2差分输入的端接电压输入。对于没有内部端接电阻的器件，内部未连接。
55	NRCV2	通道2多路复用器控制输入。差分控制输入RCV2和NRCV2可将通道2置为接收模式。RCV2高于NRCV2时，通道2进入接收模式；NRCV2高于RCV2时，通道2进入驱动模式。
56	RCV2	
57	TLDEN2	通道2负载使能端接电压输入。LDEN2和NLDEN2差分输入的端接电压输入。对于没有内部端接电阻的版本，内部未连接。
58	NLDEN2	通道2多路复用器控制输入。差分控制输入LDEN2和NLDEN2用来使能/禁用有源负载。LDEN2高于NLDEN2时，使能通道2有源负载；NLDEN2高于LDEN2时，禁用通道2有源负载。
59	LDEN2	
61	$\overline{RST}$	复位输入。串行寄存器异步复位输入。$\overline{RST}$低电平有效，有效时启动低泄漏模式。上电时，在V_{CC}和V_{EE}稳定之前，需保持$\overline{RST}$为低电平。
62	$\overline{CS}$	片选输入。串行端口使能输入。$\overline{CS}$低电平有效。
63	THR	单端逻辑门限。THR开路时，门限设置为+1.25V，也可将THR加载到所需的门限电压。
64	SCLK	串行时钟输入。串行端口时钟。
65	DIN	数据输入。串行端口数据输入。
67	LDEN1	通道1多路复用器控制输入。差分控制输入LDEN1和NLDEN1用于使能/禁用有源负载。LDEN1高于NLDEN1时，使能通道1有源负载。NLDEN1高于LDEN1时，禁用通道1有源负载。
68	NLDEN1	
69	TLDEN1	通道1负载使能端接电压输入。LDEN1和NLDEN1差分输入的端接电压输入。对于没有内部端接电阻的版本，内部未连接。
70	RCV1	通道1多路复用器控制输入。差分控制输入RCV1和NRCV1，可将通道1置为接收模式。RCV1高于NRCV1时，通道1进入接收模式；NRCV1高于RCV1时，通道1进入驱动模式。
71	NRCV1	
72	TRCV1	通道1 RCV端接电压输入。RCV1和NRCV1差分输入的端接电压输入。对于没有内部端接电阻的版本，内部未连接。
73	DATA1	通道1多路复用器控制输入。通过差分控制输入DATA1和NDATA1选择DHV1或者DLV1作为驱动器1的输入。DATA1高于NDATA1时选择DHV1；NDATA1高于DATA1时选择DLV1。
74	NDATA1	
75	TDATA1	通道1数据端接电压输入。DATA1和NDATA1差分输入的端接电压输入。对于没有内部端接电阻的版本，内部未连接。
77	LDH1	通道1有源负载吸入电流基准输入。
78	LDL1	通道1有源负载源出电流基准输入。
79	COM1	通道1有源负载换流电压基准输入。
86	CL1	通道1低端比较器输出。通道1低端比较器差分输出。
87	NCL1	

双通道、低功耗、500Mbps ATE驱动器/比较器，带有35mA负载

引脚说明 (续)

引脚	名称	功能
88	V_{CCO1}	通道1集电极电压输入。通道1比较器输出上拉电阻的加载电压。对于集电极开路输出，这是内部端接电阻的上拉电压。对于射极开路输出，这是输出晶体管的集电极电压。对于没有内部端接电阻的集电极开路器件，内部未连接。
89	CH1	通道1比较器高端输出。通道1高端比较器差分输出。
90	NCH1	
94	CPHV1	通道1高端箝位基准输入。
95	CPLV1	通道1低端箝位基准输入。
96	DHV1	通道1驱动器高端基准输入。
97	DTV1	通道1驱动器端接基准输入。
98	DLV1	通道1驱动器低端基准输入。
99	CHV1	通道1高端比较器基准输入。
100	CLV1	通道1低端比较器基准输入。

详细说明

MAX9967为双通道、低功耗、高速、引脚电子DCL IC，每个通道都包括三电平引脚驱动器、双路比较器、可调箝位电路和有源负载。驱动器可工作在-1.5V至+6.5V范围内，具有高速工作特性，它包括高阻和有源端接 (第3级驱动) 模式，在低电压摆幅下仍可保持高线性。双路比较器在各种输入条件下具有较低的偏差 (时序变化)。器件配置为高阻接收器时，箝位电路为高速DUT_波形提供阻尼衰减。负载可编程，提供最大35mA源出电流和吸入电流。可方便实现接触/连续测试、全速IOH和IOL参数测试、以及对高输出阻抗器件的上拉。

MAX9967A为驱动器提供精确的增益和失调匹配，为比较器和有源负载提供精确的失调匹配，在成本敏感的系统中，允许多通道共用基准。MAX9967B适用于每通道具有独立基准的系统设计。

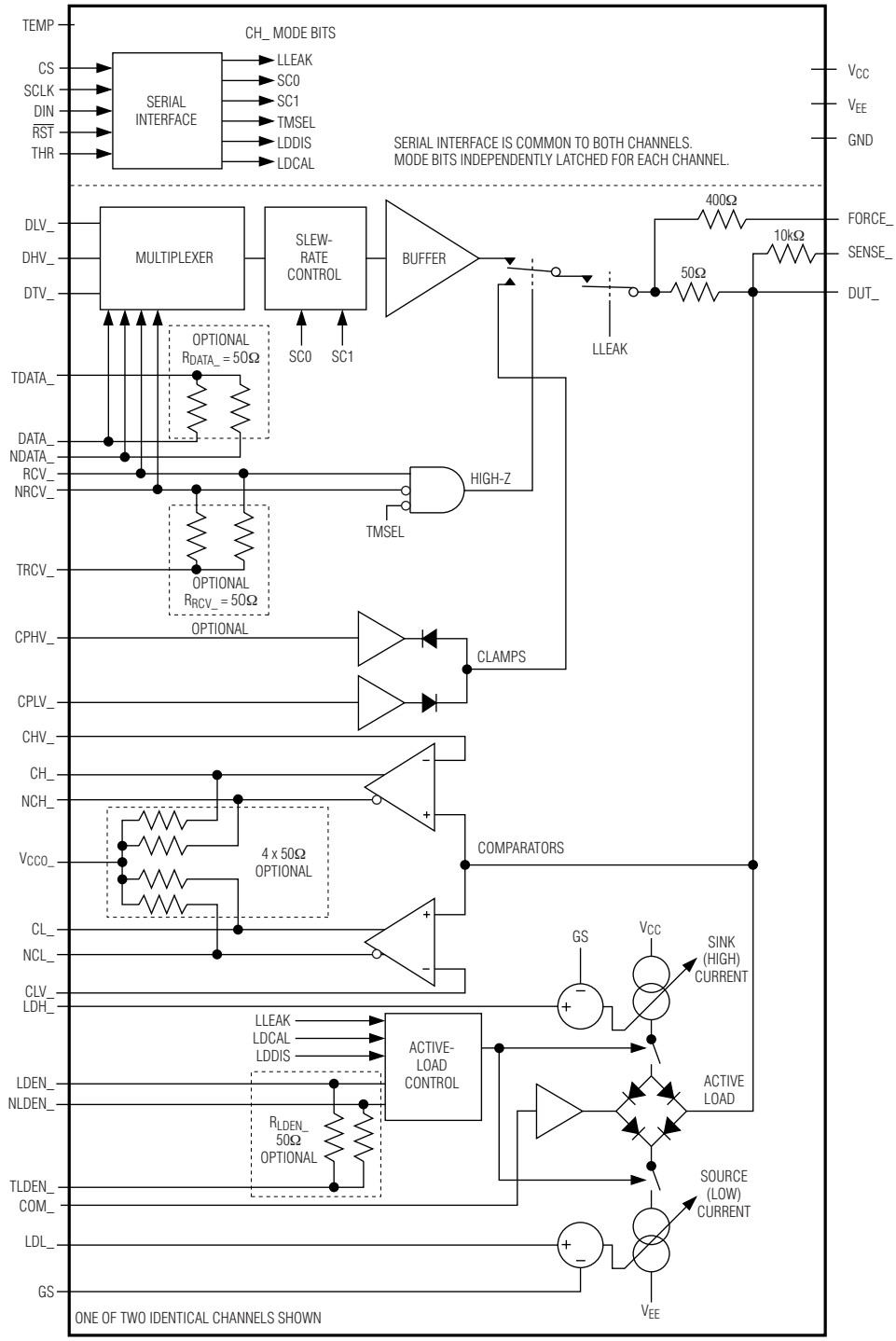
高速输入端口的可选内部电阻使器件能够兼容于ECL、LVPECL、LVDS和GTL接口。连接端接电压输入 (TDATA_、TRCV_、TLDEN_) 至合适的电压，以实现与ECL、LVPECL、GTL或其它逻辑电平的匹配连接。对于100Ω差分LVDS终端电阻，则保持输入悬空。另外，比较器提供ECL/LVPECL或者具有可选内部上拉电阻的集电极开路输出。这些功能可显著减少电路板分立元件数量。

由3线、低压、CMOS兼容串口编程设置MAX9967的低泄漏、负载禁用、摆率和三态/端接运行模式。

输出驱动器

驱动器输入是一个高速多路复用器，可选择DHV_、DLV_或DTV_三个电压之一作为输入。该选择切换由高速输入DATA_、RCV_以及模式控制位TMSEL (表1) 进行控制。摆率电路控制缓冲器输入的摆率。可根据表2在四种摆率中进行选择。内部多路复用器速率设置为100%驱动器摆率 (*参考典型工作特性*中的Driver Large-Signal Response曲线)。

功能框图


TEMP
CH_ MODE BITS
CS
SCLK
DIN
RST
THR
SERIAL INTERFACE
LLEAK
SC0
SC1
TMSEL
LDDIS
LDCAL
SERIAL INTERFACE IS COMMON TO BOTH CHANNELS.
MODE BITS INDEPENDENTLY LATCHED FOR EACH CHANNEL.
VCC
VEE
GND
DLV_
DHV_
DTV_
MULTIPLEXER
SLEW-RATE CONTROL
BUFFER
400Ω
10kΩ
50Ω
FORCE_
SENSE_
DUT_
LLEAK
SC0
SC1
OPTIONAL RDATA_ = 50Ω
TDATA_
DATA_
NDATA_
RCV_
NRCV_
HIGH-Z
TMSEL
TRCV_
OPTIONAL RRCV_ = 50Ω
OPTIONAL
CPHV_
CPLV_
CLAMPS
CHV_
CH_
NCH_
VCCO_
4 x 50Ω OPTIONAL
COMPARATORS
CL_
NCL_
CLV_
LDH_
GS
VCC
SINK (HIGH) CURRENT
LLEAK
LDCAL
LDDIS
ACTIVE-LOAD CONTROL
ACTIVE LOAD
LDEN_
NLDEN_
RLDEN_ 50Ω OPTIONAL
TLDEN_
COM_
SOURCE (LOW) CURRENT
LDL_
GS
VEE
ONE OF TWO IDENTICAL CHANNELS SHOWN

双通道、低功耗、500Mbps ATE驱动器/比较器，带有35mA负载

DUT_可在缓冲器输出和高阻模式之间高速转换，也可置为低泄漏模式 (见图2和表1)。高阻模式下，接入了箝位电路。高速输入RCV_和模式控制位TMSEL、LLEAK控制该切换。高阻模式下，DUT_的偏置电流在0至3V电压范围内小于1.5µA，而节点仍然能够跟踪高速信号。低泄漏模式下，DUT_的偏置电流进一步降至50nA以下，信号跟踪能力变慢。更多细节请参考*低泄漏模式，LLEAK*部分。

驱动器输出阻抗标称值为50Ω。若需45Ω至51Ω范围内的不同电阻值，请与厂商联系。

箝位电路

当通道配置为高阻接收器时，应设置电压箝位 (高电平和低电平) 以限制DUT_上的电压并抑制反射。箝位电路如同连接至大电流缓冲器输出的二极管。内部电路对1mA箝位电流时的二极管压降进行补偿。使用外部连接端CPHV_和CPLV_设置箝位电压。箝位电路仅在驱动器处于高阻模式时有效 (图2)。为实现瞬态抑制，需设置箝位电压近似等于所需的最小和最大DUT_电压。最佳箝位电压取决于应用情况，需要根据经验确定。如果不需要箝位，应将箝位电压设置在超出所需DUT_电压范围的0.7V以外；没有加载DUT_时，过压保护电路仍然保持工作状态。

比较器

MAX9967的每一个通道都含有两个独立的高速比较器。每个比较器的一个输入内部连接至DUT_，另一个输入连接至CHV_或者CLV_ (*参考功能框图*)。如表3所示，比较器输出为输入条件的逻辑运算结果。

比较器差分输出提供三种配置结构，很容易与多种逻辑电平接口。集电极开路输出结构在两个输出之间切换一个8mA电流源。该结构提供或不提供连接至$V_{CCO_}$的内部端接电阻 (图3)。对于没有内部端接的集电极开路版本，则不要连接$V_{CCO_}$，并加入所需的外部电阻。这些典型值为50Ω的电阻连接至输出走线接收端的上拉电压。在不超过*Absolute Maximum Ratings*的条件下，也可以使用不同的配置。对于具有内部端接的集电极开路版本，连接$V_{CCO_}$至所需的V_{OH}电压。每路输出提供标称值为400mV_{P-P}的摆幅和50Ω源终端匹配电阻。

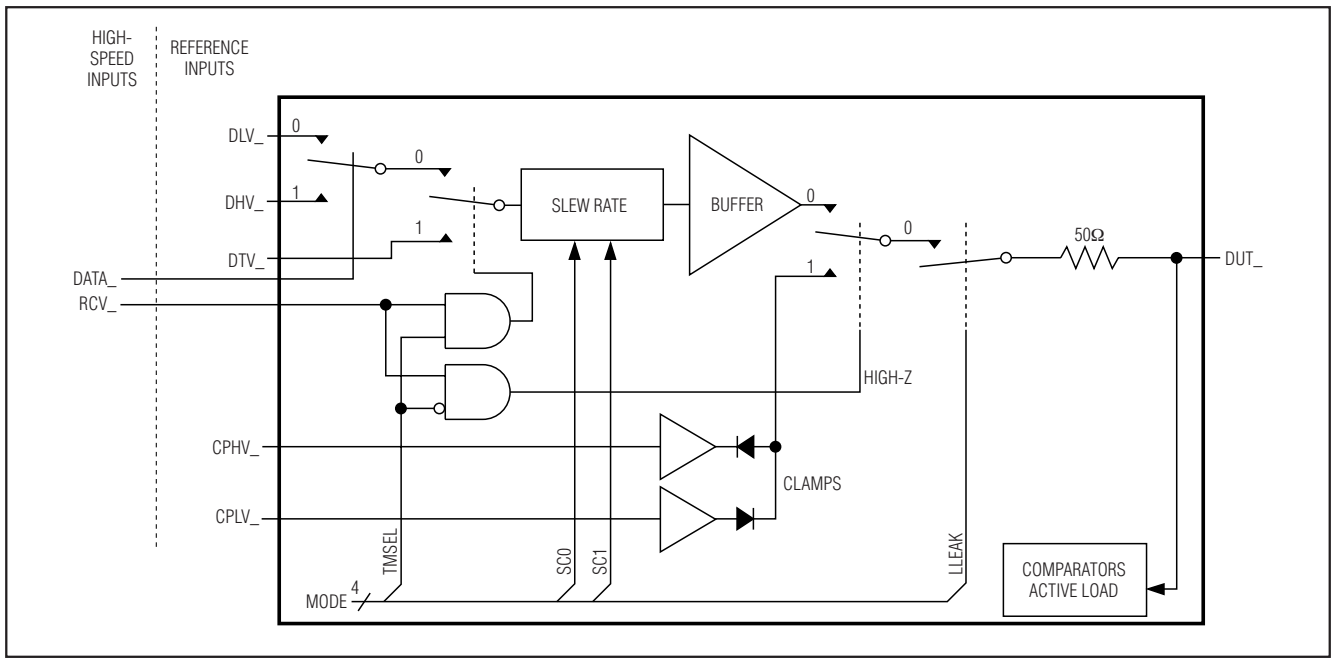


图2. 简化驱动器通道

表1. 驱动器逻辑

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA_	RCV_	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance (high-z) mode
X	X	X	1	Low-leakage mode

表2. 摆率逻辑

SC1	SC0	DRIVER SLEW RATE (%)
0	0	100
0	1	75
1	0	50
1	1	25

输出级还提供射极开路结构(图4)。连接外部集电极电压至$V_{CCO_}$，并加入外部下拉电阻。这些典型值为50Ω的电阻连接至输出走线接收端，加载电压为$V_{CCO_}$ - 2V。在不超过*Absolute Maximum Ratings*的条件下，也可以使用不同配置。

有源负载

有源负载由线性可编程的源出和吸入电流源、一个换流缓冲器和一个二极管桥 (*参考功能框图*) 组成。模拟控制输入LDH_和LDL_，分别在0至35mA范围内编程设置吸入和源出电流。模拟基准输入COM_设置换流缓冲器的输出电压。源出和吸入相对被测器件而言。流出MAX9967的电流称为吸入电流，而流入MAX9967的电流称为源出电流。

可编程源出 (低) 电流在$V_{DUT_} > V_{COM_}$时，加载被测器件。可编程吸入 (高) 电流在$V_{DUT_} < V_{COM_}$时，加载被测器件。

GS输入允许使用MAX5631或MAX5734等电平设置DAC对MAX9967的有源负载、驱动器、比较器和箝位电路进行编程设置。尽管所有DAC电平通常由V_{GS}进行偏置，相对于有源负载电流而言，MAX9967的地检测输入消除了这种偏置影响。连接GS至DAC所使用的地参考端。($V_{LDL\_}$ - V_{GS}) 以+10mA/V的比率设置源出电流。($V_{LDH\_}$ - V_{GS}) 以-10mA/V的比率设置吸入电流。

高速差分输入LDEN_以及控制字的3位 (LDCAL、LDDIS和LLEAK) 对负载进行控制 (表4)。当负载使能后，内部源出和吸入电流源连接至二极管桥。负载禁用后，内部电流源旁路至地，二极管桥的两端浮空 (*参考功能框图*)。LLEAK将负载置为低泄漏模式。LLEAK优先级高于LDEN_、LDDIS和LDCAL。更多详细信息请参考*低泄漏模式，LLEAK*部分。

LDDIS和LDCAL

在一些测试仪配置中，负载使能由驱动器高阻信号 (RCV_) 的置反信号驱动，因此禁用驱动器将会使能负载，反之亦然。无论LDEN_为何状态，LDDIS和LDCAL信号都可以禁用和使能负载。这允许同时使能和禁用负载与驱动器，从而实现诊断功能 (表4)。

低泄漏模式，LLEAK

通过串行端口将LLEAK置位，或者利用$\overline{RST}$可使MAX9967进入低泄漏状态 (*参考Electrical Characteristics*)。此时，比较器全速工作，而禁用驱动器、箝位电路和有源负载。该模式不需要输出断开继电器，即可方便进行IDDQ和PMU测量。对于每个通道，LLEAK可独立编程设置。

当DUT_以高速信号驱动，而LLEAK置位时，泄漏电流瞬间增加并超过正常工作所规定的限制值。*Electrical Characteristics*表中的低泄漏恢复指标给出了器件在这种条件下的运行状态。

表3. 比较器逻辑

DUT_ > CHV_	DUT_ > CLV_	CH_	CL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

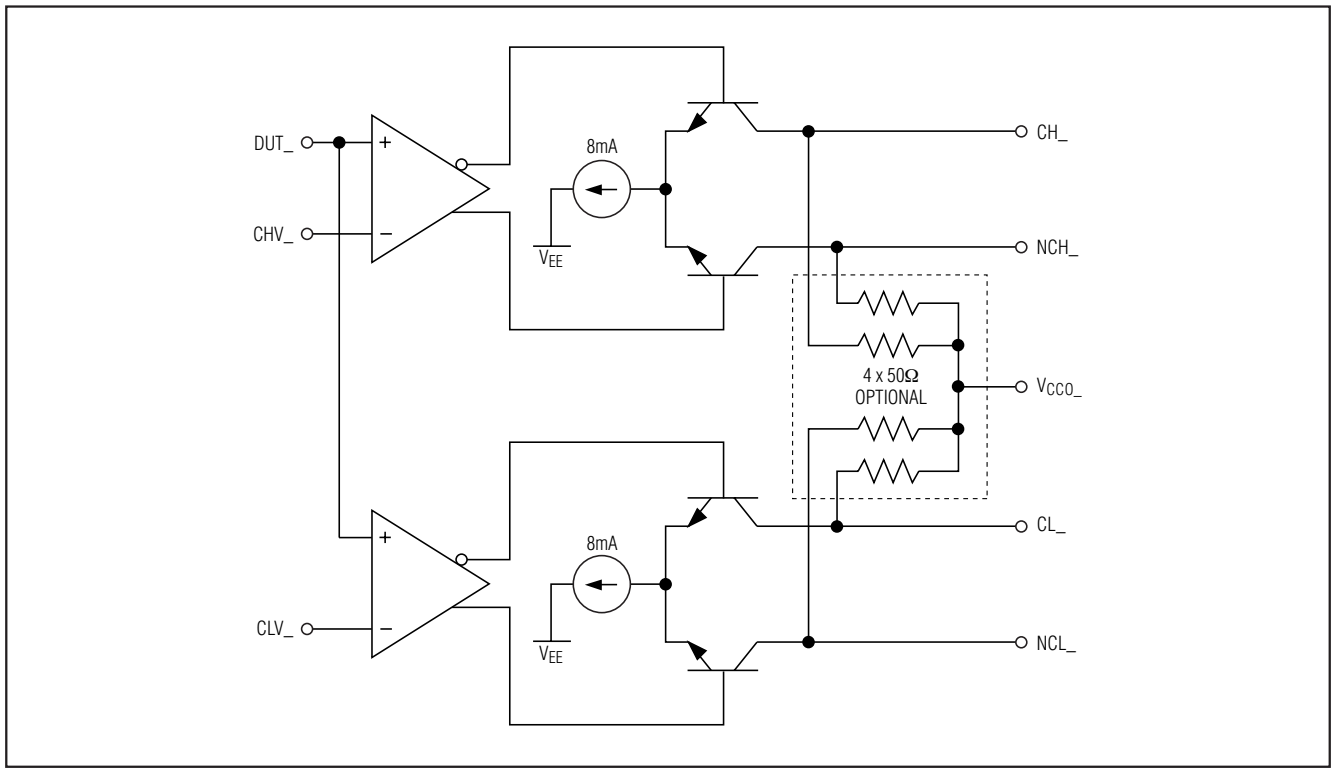


图3. 比较器集电极开路输出

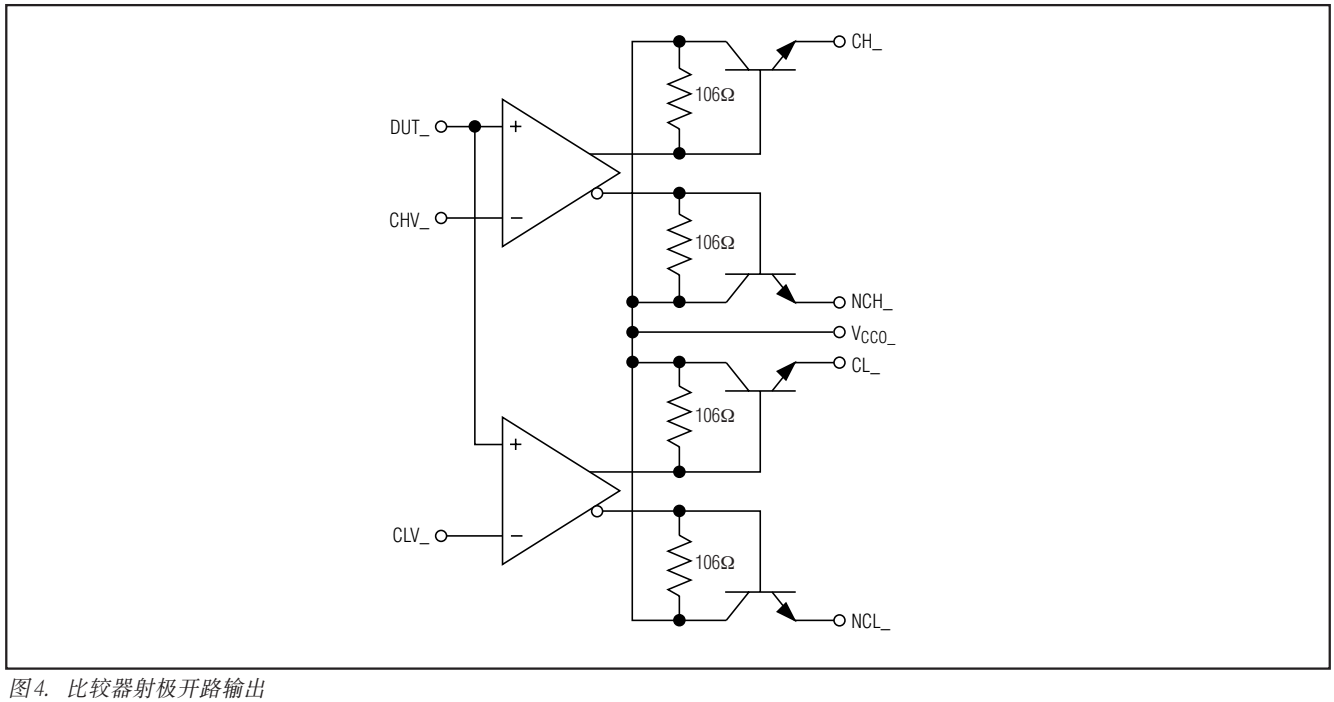


图4. 比较器射极开路输出

表4. 有源负载编程

EXTERNAL CONNECTIONS	INTERNAL CONTROL REGISTER			MODE
LDEN_	LDCAL	LDDIS	LLEAK	
0	0	0	0	Normal operating mode, load disabled
1	0	0	0	Normal operating mode, load enabled
X	1	0	0	Load enabled for diagnostics
X	X	1	0	Load disabled
X	X	X	1	Low-leakage mode

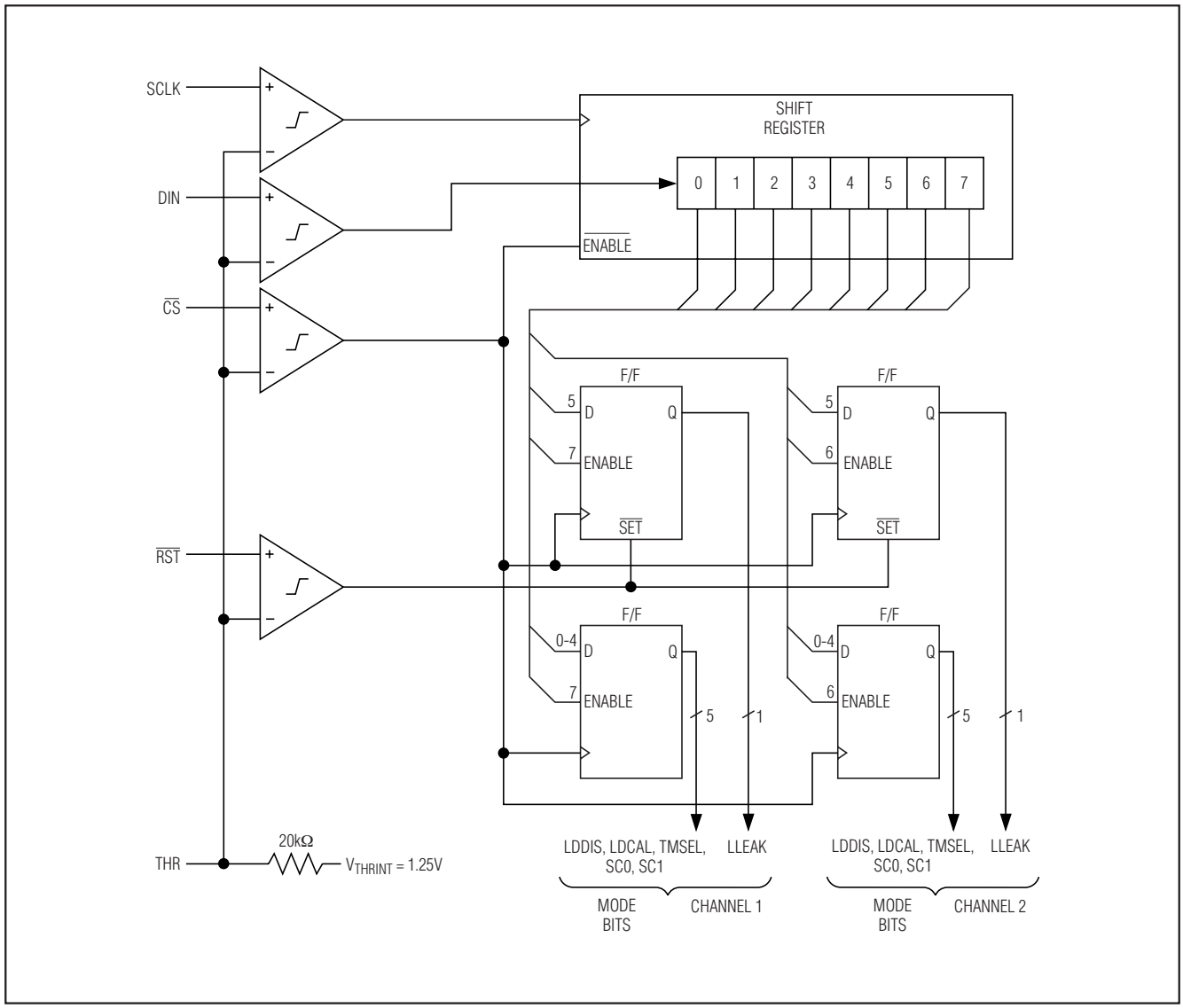


图5. 串行接口

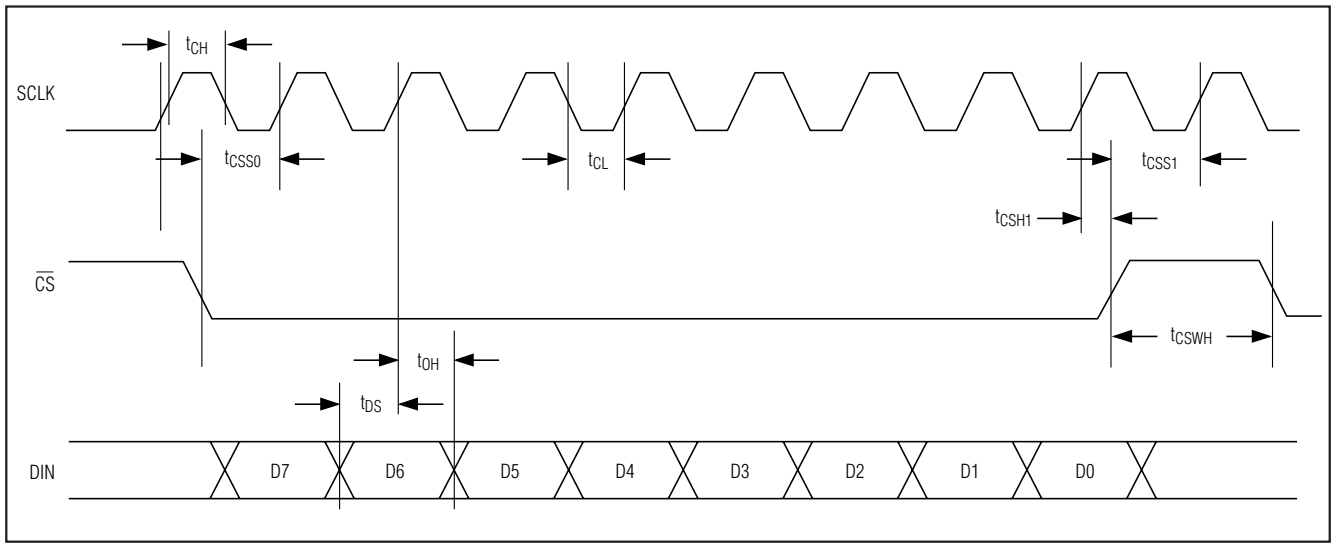


图6. 串口时序

串口和器件控制

CMOS兼容串行接口控制MAX9967的工作模式 (图5)。如图6所示，控制数据进入一个8位移位寄存器 (MSB在前)，并在$\overline{CS}$变为高电平时锁存该数据。锁存器为双引脚驱动器的每个通道提供6个控制位。如图5和表5所示，来自移位寄存器的数据装入其中一个或所有两个锁存器，具体由D6和D7决定。控制位同外部输入DATA_和RCV_一起管理每个通道的功能，如表1和表2所示。$\overline{RST}$将所有两个通道设置为LLEAK = 1，强制它们进入低泄漏模式。其它所有位不受影响。上电时，在V_{CC}和V_{EE}稳定之前，$\overline{RST}$需保持低电平。

模拟控制输入THR用于设置输入逻辑电平的门限，允许与低至0.9V的CMOS逻辑电平接口。THR悬空时，会产生来自内部基准的1.25V门限电压，并与2.5V至3.3V逻辑电平兼容。

表5. 移位寄存器功能

BIT	NAME	DESCRIPTION
D7	CH1	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.
D6	CH2	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.
D5	LLEAK	Low-Leakage Select. Set to 1 to put driver, load, and clamps into low-leakage mode. Comparators remain active in low-leakage mode. Set to 0 for normal operation.
D4	TMSEL	Driver Termination Select. Set to 1 to force the driver output to the DTV_ voltage when RCV_ = 1 (term). Set to 0 to place the driver into high-impedance mode when RCV_ = 1 (high-Z). See Table 1.
D3	SC1	Driver Slew-Rate Select. SC1 and SC0 set the driver slew rate. See Table 2.
D2	SC0	
D1	LDDIS	Load Disable. Set LDDIS to 1 to disable the load. Set to 0 for normal operation. See Table 4.
D0	LDCAL	Load Calibrate. Overrides LDEN to enable load. Set LDCAL to 1 to enable load. Set LDCAL to 0 for normal operation. See Table 4.

温度监视

MAX9967提供温度输出信号TEMP，在管芯温度为+70°C (343K) 时输出标称值为3.43V的电压。此输出电压随温度升高而成比例增大。

散热

在正常环境下，MAX9967需要采用外部散热器并通过裸露焊盘进行散热。裸露焊盘与V_{EE}等电势，必需连接至V_{EE}或者进行隔离处理。

功耗与具体应用密切相关。*Electrical Characteristics*表给出了源出电流和吸入电流设置为0mA时器件的功耗情况。当源出和吸入电流都达到35mA，$V_{DUT_}$处于电压范围(-1.5V或+6.5V) 的极限值，并且二极管桥换流达到满摆幅时，功耗最大。在这些条件下，增加的功耗 (每个通道) 为：

如果DUT源出电流，则有$\Delta P_D = (V_{DUT_} - V_{EE}) \times I_{SOURCE} + (V_{CC} - V_{EE}) \times I_{SINK}$。

如果DUT吸入电流，则有$\Delta P_D = (V_{CC} - V_{DUT_}) \times I_{SINK} + (V_{CC} - V_{EE}) \times I_{SOURCE}$。

当$V_{DUT_} > V_{COM_}$时，DUT源出 (低) 所设置的电流。电流路径为从DUT开始，流经二极管桥的外侧、源出 (低) 电流源，到达V_{EE}。所设置的吸入电流由V_{CC}流出，经过吸电流 (高) 电流源、二极管桥内侧以及换流缓冲器，到达V_{EE}。

当$V_{DUT_} < V_{COM_}$时，DUT吸入(高) 所设置的电流。电流路径从V_{CC}开始，流经吸电流 (高) 电流源、二极管桥外侧，到达DUT。所设置的源出电流从V_{CC}流出，流经换流缓冲器、二极管桥内侧、源出 (低) 电流源，到达V_{EE}。

带裸露焊盘的封装J-C热阻很低，大约为3°C/W至4°C/W。因此管芯温度很大程度上取决于应用中使用的散热方案。

在以下条件下产生最大总功耗：

- V_{CC} = +10.5V
- V_{EE} = -6.5V
- 所有两个通道：$I_{SOURCE} = I_{SINK}$ = 35mA
- 负载使能
- $V_{DUT\_}$ = +6.5V
- $V_{COM\_}$ < +5.5V

在这些极限条件下，总功耗大约为6W。如果在这些条件下管芯温度不能维持在可以接受的水平，使用软件箝位限制负载输出电流至较低值和/或降低电源电压。

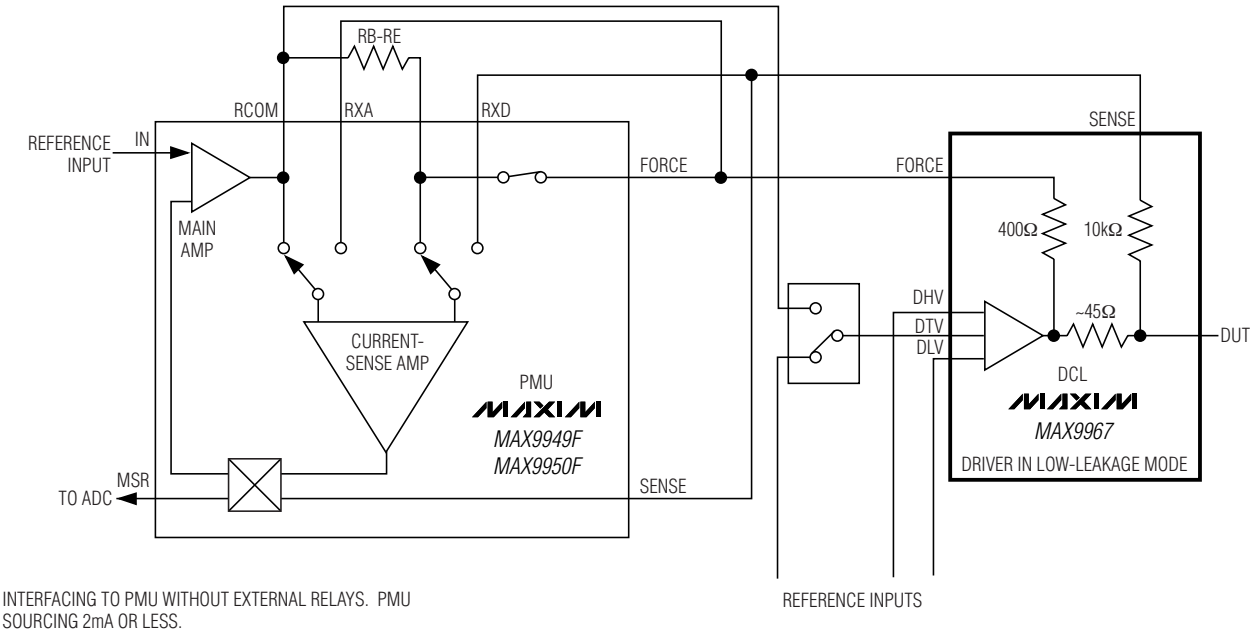
芯片信息

TRANSISTOR COUNT: 5656

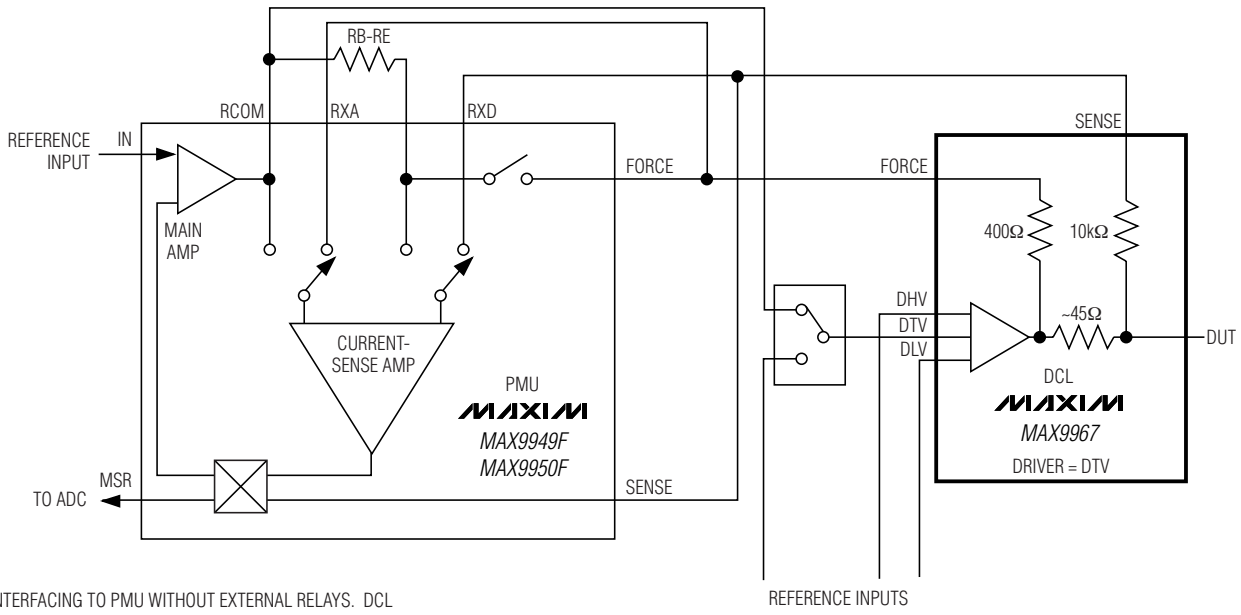
PROCESS: Bipolar

双通道、低功耗、500Mbps ATE驱动器/比较器，带有35mA负载

典型应用电路 (简图)



INTERFACING TO PMU WITHOUT EXTERNAL RELAYS. PMU SOURCING 2mA OR LESS.

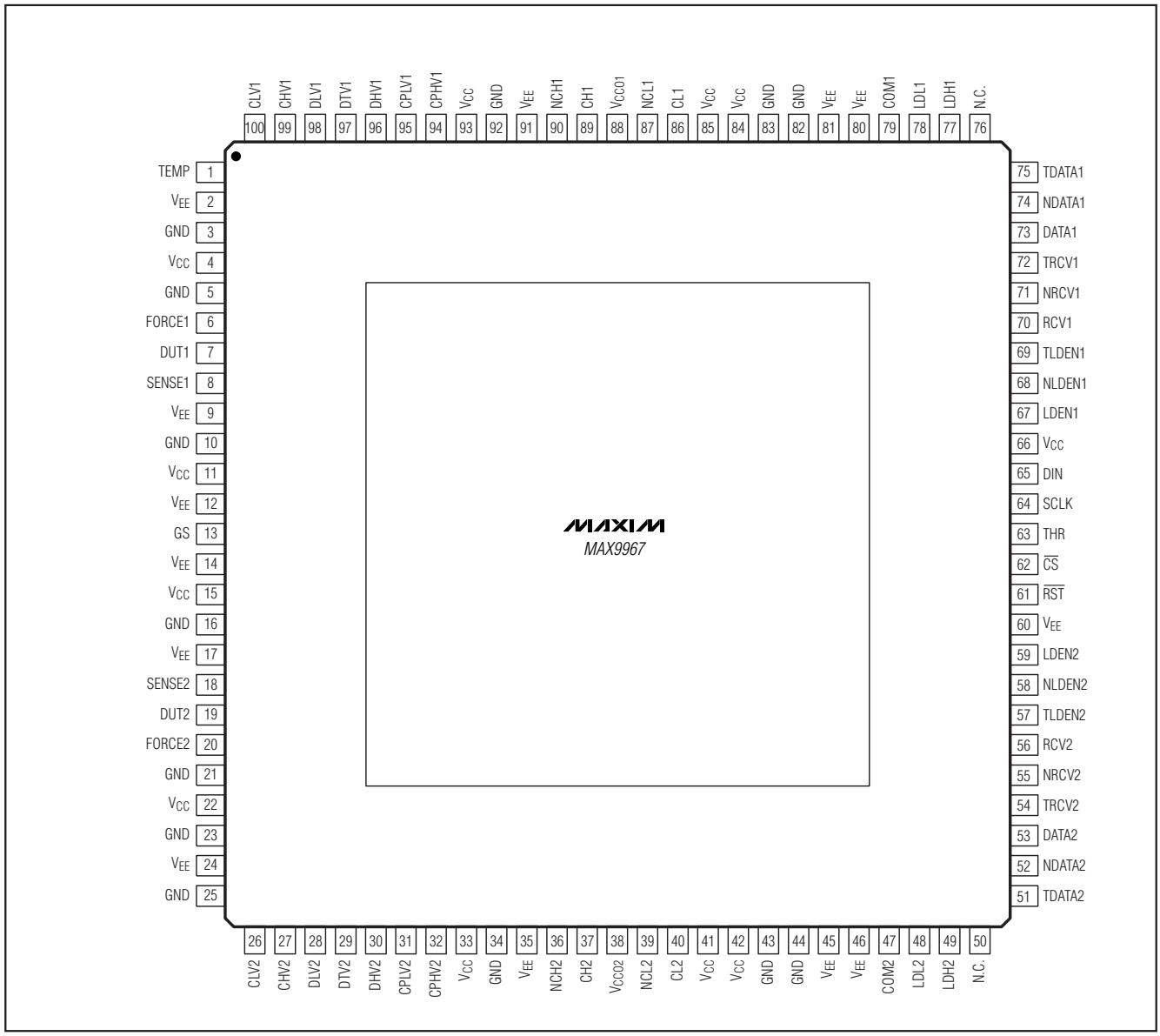


INTERFACING TO PMU WITHOUT EXTERNAL RELAYS. DCL SOURCING UP TO 60mA.

PART	ACCURACY GRADE	COMPARATOR OUTPUT TYPE	COMPARATOR OUTPUT TERMINATION	HIGH-SPEED DIGITAL INPUT TERMINATION			HEAT EXTRACTION
				RCV_	DATA_	LDEN_	
MAX9967ADCCQ	A	Open collector	None	None	None	None	Top
MAX9967AGCCQ	A	Open collector	None	100	100	100	Top
MAX9967ALCCQ	A	Open collector	50Ω to $V_{CCO\_}$	100	100	100	Top
MAX9967AMCCQ	A	Open emitter	ECL/LVPECL	None	None	None	Top
MAX9967AQCCQ	A	Open emitter	ECL/LVPECL	100	100	100	Top
MAX967ARCCQ	A	Open collector	50Ω to $V_{CCO\_}$	None	100	100	Top
MAX9967BDCCQ	B	Open collector	None	None	None	None	Top
MAX9967BGCCQ	B	Open collector	None	100	100	100	Top
MAX9967BLCCQ	B	Open collector	50Ω to $V_{CCO\_}$	100	100	100	Top
MAX9967BMCCQ	B	Open emitter	ECL/LVPECL	None	None	None	Top
MAX9967BQCCQ	B	Open emitter	ECL/LVPECL	100	100	100	Top
MAX9967BRCCQ	B	Open collector	50Ω to $V_{CCO\_}$	None	100	100	Top

双通道、低功耗、500Mbps ATE驱动器/比较器，带有35mA负载

引脚配置



封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 **www.maxim-ic.com.cn/packages**。)